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A 1.0-V 10-b 30-MS/s 3.4-mW rail-to-rail pipelined ADC using a new front-end MDAC

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Abstract: This paper describes a low-voltage design for a pipelined ADC that can operate in a 2.0-V_{pp} full-swing input range at a 1.0-V supply. To enlarge the input range of an ADC and maintain the output range of its op-amps, we propose a new front-end 2b-MDAC with S/H that can reduce the output ranges of all MDACs by 50% compared to the ADC's input. We designed a 10-b pipelined ADC with the proposed front-end MDAC using a 90-nm CMOS process. The ADC achieved 2.0-V_{pp} rail-to-rail operation at only a 1-V supply and a 57.5-dB SNDR with only 3.4 mW at 30 MS/s despite using conventional folded-cascode op-amps.

Keywords: pipeline ADC, MDAC, op-amp, low-voltage, low-power

Classification: Integrated circuits

References

[1] K. Gotoh, H. Ando, and A. Iwata, "A 10-b 30-MS/s 3.4-mW Pipelined ADC with 2.0-V_{pp} Full-swing Input at a 1.0-V Supply," *ASSCC Dig. Tech. Papers*, pp. 57–60, Nov. 2008.

[2] K. Gotoh and O. Kobayashi, "3 States Logic Controlled CMOS Cyclic A/D Converter," *Proc. CICC*, pp. 366–369, May 1986.

[3] M. Yoshioka, M. Kudo, T. Mori, and S. Tsukamoto, "A 0.8 V 10b 80 MS/s 6.5 mW Pipelined ADC with Regulated Overdrive Voltage Biasing," *ISSCC Dig. Tech. Papers*, pp. 452–453, Feb. 2007.

[4] O. Stroeble, V. Dias, and C. Schwoerer; "An 80 MHz 10b pipeline ADC with Dynamic Range Doubling and Dynamic Reference Selection," *ISSCC Dig. Tech. Papers*, pp. 462–463, Feb. 2004.

[5] M. Yoshioka, M. Kudo, K. Gotoh, and Y. Watanabe, "A 10b 125 MS/s 40 mW Pipelined ADC in 0.18 μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 282–283, Feb. 2005.

[6] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[7] S.-T. Ryu, B.-S. Song, and B. K, "A 10b 50 MS/s Pipelined ADC with Opamp Current Reuse," *ISSCC Dig. Tech. Papers*, pp. 216–217, Feb. 2006.

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1 Introduction

The demand for high-speed ($\geq 30\,\mathrm{MS/s}$) and high-resolution ($\geq 10\,\mathrm{bit}$) analog-to-digital converters (ADC) is increasing because of the rapid growth in digital consumer applications and wireless communications. The analog circuits included in these applications have recently been developed with system on a chip (SoC) devices using scaled CMOS processes. A low-voltage operation ($\leq 1.2\,\mathrm{V}$) is required for an ADC that is highly-accurate, with low-power, and has a small die-size when using these processes.

Although a pipelined ADC is popular and suitable circuit architecture for use in these applications, it is challenging to operate under a 1.2-V supply while satisfying the mentioned requirements because of the headroom voltage range of an operational amplifier (op-amp). To reduce the analog signal range, the sampling-capacitor for a pipelined ADC must increase to obtain the same accuracy, because the thermal noise (kT/C) must be reduced to correspond with the input signal power. This means that the analog power consumption and die-size of the ADC increases despite a low supply voltage. Therefore, how to handle a large input range under a 1.2-V supply has been an important concern.

This paper describes a new front-end 2b-MDAC with S/H that can enlarge the ADC's input range twice the op-amp's output range [1]. The fabricated ADC using the proposed front-end MDAC achieved a full-swing input operation for a 1-V supply without using rail-to-rail op-amps. Improvement of figure of merit (FOM) is also discussed.

2 Proposed new Front-end 2b-MDAC with S/H

2.1 Issues with conventional S/H and 1.5b-MDAC

The transfer functions of a conventional S/H and 1.5b-MDAC [2] are shown in Fig. 1 (a). These output ranges are limited by the output range of the following op-amp (VO_{AMP_FS}).

$$VO_{AMP\_FS} = V_{DD} - (N_p + N_n) * V_{OD} \tag{1}$$

where the $(N_p+N_n)*V_{OD}$ is the headroom voltage (VO_{AMP_HR}) that consists of the over-drive voltage (V_{OD}) and the number of the cascode transistors ($N_p + N_n$).

If a folded-cascode op-amp (OPA-I) is used for MDAC where the N_p+N_n is 4 to obtain a high DC gain, and V_{OD} is set to 0.125 V, the differential input range VIN_{diff_FS} of a 1.5b-MDAC would become:

$$VIN_{diff\_FS} = 2 * (V_{DD} - (N_p + N_n) * V_{OD}) \tag{2}$$

$$= 2 * (V_{DD} - 0.5) \tag{3}$$

This means that VIN_{diff_FS} for a 1.0-V supply becomes $1.0\,\mathrm{V_{pp}}$ that is only half the ideal full-swing input, see Fig. 1 (b).

The conventional approach is to find out how to reduce the headroom voltage of an op-amp. By using multi-stage and a regulated low V_{OD} control

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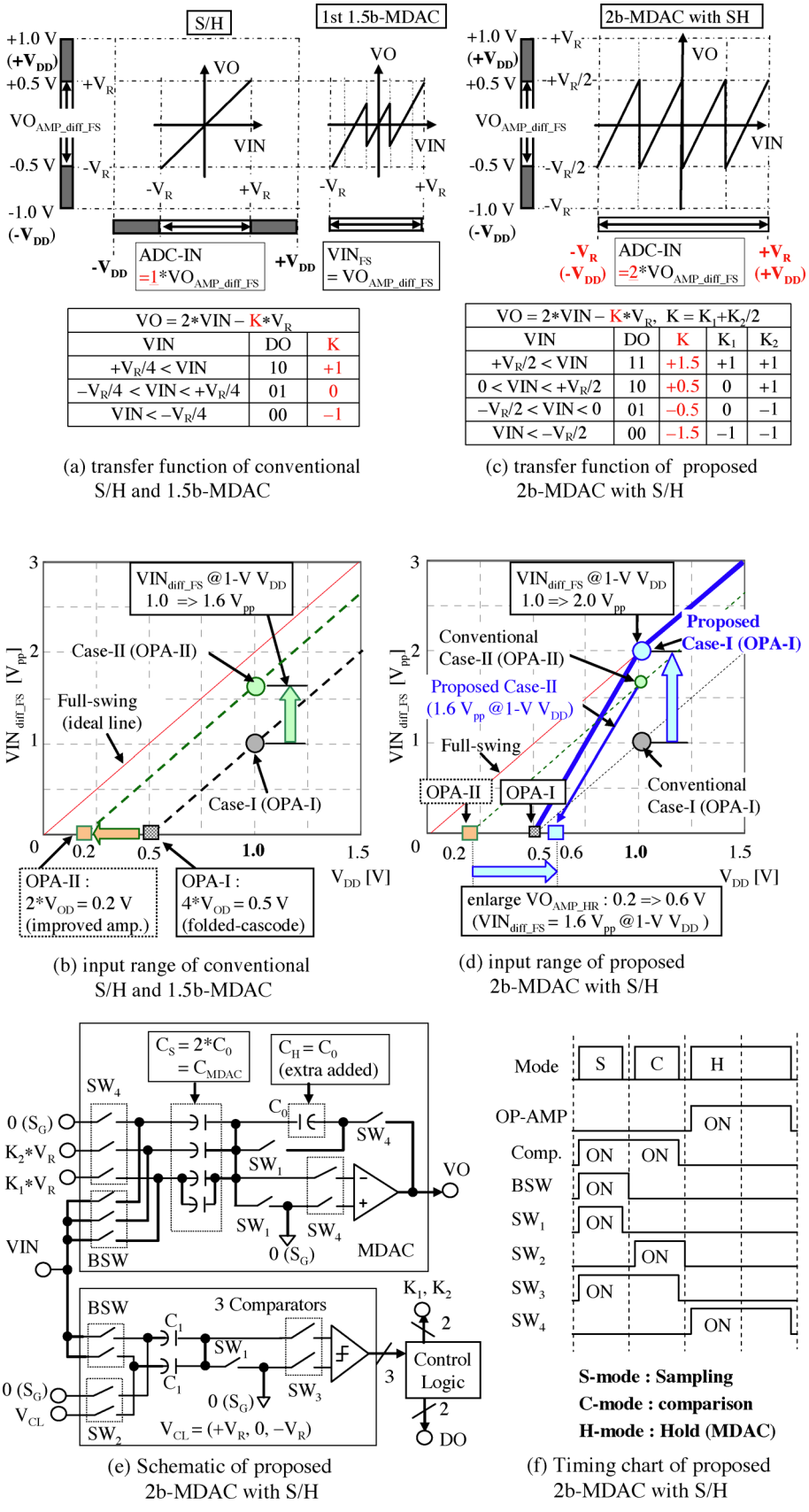

VO = 2*VIN – K*V_R		
VIN	DO	K
+V_R/4 < VIN	10	+1
–V_R/4 < VIN < +V_R/4	01	0
VIN < –V_R/4	00	–1

(a) transfer function of conventional S/H and 1.5b-MDAC

VO = 2*VIN – K*V_R, K = K_1+K_2/2				
VIN	DO	K	K_1	K_2
+V_R/2 < VIN	11	+1.5	+1	+1
0 < VIN < +V_R/2	10	+0.5	0	+1
–V_R/2 < VIN < 0	01	–0.5	0	–1
VIN < –V_R/2	00	–1.5	–1	–1

(c) transfer function of proposed 2b-MDAC with S/H

(b) input range of conventional S/H and 1.5b-MDAC

(d) input range of proposed 2b-MDAC with S/H

(e) Schematic of proposed 2b-MDAC with S/H

(f) Timing chart of proposed 2b-MDAC with S/H

Fig. 1. Proposed Front-end 2b-MDAC with S/H

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technique [3], the VO_{AMP_HR} for the improved op-amp (OPA-II) is reduced to 0.2 V with $N_p + N_n = 2$ and $V_{OD} = 0.1$ V. The VIN_{diff_FS} for this op-amp is:

$$VIN_{diff\_FS} = 2 * (V_{DD} - 0.2) \tag{4}$$

In this case, the VIN_{diff_FS}can be increased up to 1.6 V_{pp} at a 1.0-V supply. However, by improving only an op-amp, a full-swing input operation cannot be achieved.

2.2 Architecture of Proposed 2b-MDAC with S/H

To enlarge the ADC's input range to twice all its op-amp's output ranges including S/H, we propose a new front-end 2b-MDAC with S/H, as shown in Fig. 1 (c). The output voltage VO of an MDAC is determined as:

$$VO = 2 * VIN - K * V_R \tag{5}$$

where K is set to the value decided by the comparator levels shown in the tables in Figs. 1 (a) and (c), and $\pm V_R$ is the reference voltages for an ADC. To modify the transfer function, the number of segments is increased from 3 to 4, and the value of maximum K ($= K_{max}$) is enhanced from 1 to 1.5. By using these modifications, VO_{FS} of the 2b-MDAC can be reduced to half the input range.

Reducing only the output range of an MDAC to half the input range has already been reported [4], but the input range of the ADC has not been enhanced because a remained S/H op-amp cannot reduce its output range. To solve this issue, the proposed 2b-MDAC adopted the circuit technique for implementing a sample-hold function without the S/H op-amp [5]. By setting the 2b-MDAC with S/H to the 1st-stage of an ADC, the ADC's input range can be enhanced twice all its op-amp's output ranges. In the case of using the op-amp OPA-I, the VIN_{diff_FS} of the proposed 2b-MDAC becomes:

$$VIN_{diff\_FS} = 4 * (V_{DD} - (N_p + N_n) * V_{OD}) \tag{6}$$

$$= 4 * (V_{DD} - 0.5) \tag{7}$$

This means that the proposed 2b-MDAC with S/H can handle 2.0-V_{pp} full-swing input at the 1.0-V supply, see Fig. 1 (d). In this case, the op-amps for the reference voltages can be removed by using V_{DD} and GND, as supplies.

2.3 Circuit Design

A schematic and timing chart of the proposed 2b-MDAC with S/H are shown in Figs. 1 (e) and (f). To obtain a sample-hold function without an extra op-amp and capacitance, the 2b-MDAC has three operational modes and an op-amp is used for only the hold-mode, see Fig. 1 (f). In the 1st quarter period (Sampling), the input signal VIN is sampled to capacitors C_S and C_1 by using the switches SW_1 and the bootstrap switches BSW [6]. In the 2nd quarter period (Comparison), the VIN is compared with three levels (0, $\pm V_R/2$) and digital output data (DO, K_1, K_2) is obtained by using the switched-capacitor comparators, see Fig. 1 (e). In the last half period (Hold),

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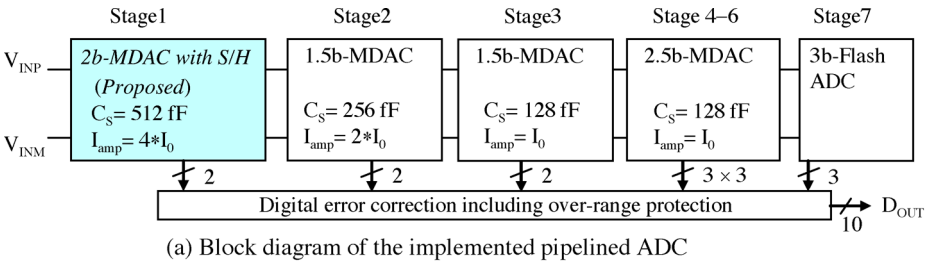
the output voltage of the MDAC (VO) is calculated by using an op-amp and an extra C_H to deal with a K_{max} of up to 1.5, see Figs. 1 (c) and (e).

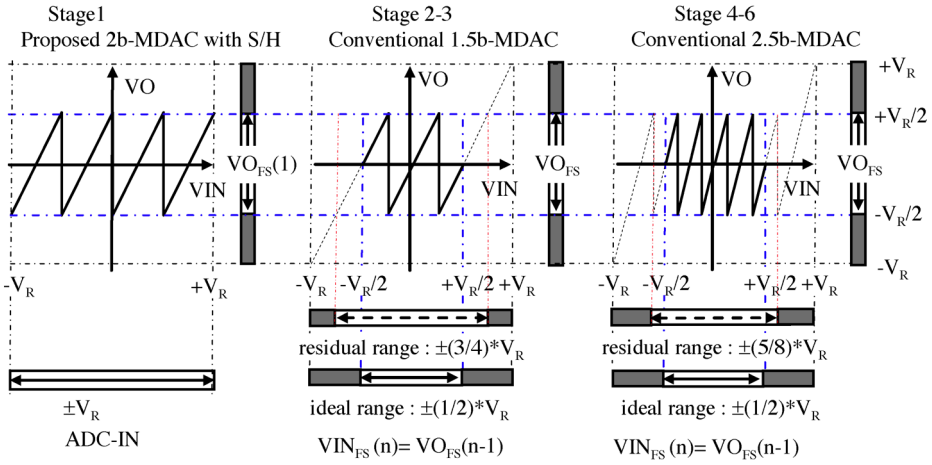
2.4 Merits of using the proposed 2b-MDAC with S/H

The merits of the proposed 2b-MDAC with S/H will be discussed by comparing a 1.5b-MDAC under the same conditions, using the op-amp OPA-I and a 1.0-V supply. The input range of the 2b-MDAC is double that of the 1.5b-MDAC. So, the value of the unit capacitor C_0 can be decreased to 1/4 compared with the one for the 1.5b-MDAC. The number of C_0 increases from 2 to 3 and the gain-factor β of an op-amp becomes 1/3 from 1/2. As a result, the total capacitance and the current of op-amp can be decreased to 3/8 ($= (3/2) * (1/4)$). Another merit is that the op-amps for the reference voltages and S/H can be removed. These features are a very effective way to ensure low-power consumption and small die-size.

In another point of view to design a low-voltage op-amp, a conventional 1.5b-MDAC needs the improved multi-stage op-amp OPA-II with VO_{AMP_HR} = 0.2 V to obtain 1.6-V_{pp} input range at a 1.0-V supply, in Fig. 1 (b). By using the 2b-MDAC with S/H for the same input condition, the headroom voltage for its op-amp can be enlarged to 0.6 V from 0.2 V, see Fig. 1 (d). This feature is very effective when design a low voltage op-amp because the headroom issue can almost be ignored.



(a) Block diagram of the implemented pipelined ADC



(b) transfer function of MDACs of the implemented ADC

Fig. 2. Implemented ADC architecture

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3 Implemented ADC Architecture using the 2b-MDAC with S/H

A block diagram of our implemented ADC is shown in Fig. 2 (a). The 1st-stage of the ADC is the proposed 2b-MDAC with S/H. The following stages consist of conventional circuits that are two 1.5b-MDACs, three 2.5b-MDACs and a 3b-flash ADC. Stages 4–6 are using multi-bits MDACs to reduce the die-size.

The transfer functions of MDACs are shown in Fig. 2 (b). By setting the 2b-MDAC to the 1st-stage, all input and output ranges of other stages can be reduced to half the ADC's input range, see Fig. 2 (b).

Next, I will discuss the effect of the comparator's offset voltage (V_{CMP_offset}) that is within ±10 mV by using the switched-capacitor comparators. The output range for a 2.5b-MDAC is increased to $4 * V_{CMP\_offset}$ ($= \pm 40$ mV) from the ideal input range $\pm V_R/2$, so the headroom voltage $4 * V_{OD}$ of the folded-cascode op-amps for the ADC is adjusted to 0.44 V from 0.5 V. The input residual range for the 2.5b-MDAC is $\pm(5/8) * V_R$ that covers the increased input range by the V_{CMP_offset}, so the $\pm(5/8) * V_R$ comparators can be removed, see Fig. 2 (b).

4 Measured Results

A prototype ADC was fabricated using a 90-nm CMOS technology. The ADC achieved 2.0-V_{PP} input range at a 1.0-V supply. With the measured condition of the full-swing input level and a 30-MS/s conversion rate (F_s), a 57.5-dB SNDR at only 3.4 mW was obtained for a 4.89 MHz of input signal. The INL and DNL are $-0.9/+1.1$ LSB and $5/+0.5$ LSB, respectively. The active area of the ADC is 1.12 mm^2.

Table I shows a comparison of the reported 10-bit pipelined ADCs. Here, a figure of merit is represented as:

$$FOM = Power/(F_s * 2^{ENOB}) \tag{8}$$

The proposed ADC shows the lowest FOM and the largest input range.

Table I. 10-bit ADC performance comparison

Reference	OP-AMP Type	V_{DD} [V]	VIN_{FS} [V_{pp}]	F_S [MS/s]	SNDR [dB]	Power [mW]	FOM [pJ/step]
[7]	folded-cascode	1.8	1.0	50	56.9	18	0.61
[6]	multi-stage	1.5	0.8	14.3	58.5	36	3.72
[3]	multi-stage	1.2	1.2	80	56.9	13.3	0.28
[3]	multi-stage	0.8	1.2	80	55.0	6.5	0.18
This work	folded-cascode	1.0	2.0	30	57.5	3.4	0.18

5 Conclusion

This paper described new pipelined ADC architecture that can almost ignore the headroom voltage issue of an op-amp. To solve this issue, we proposed

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a new front-end 2b-MDAC with S/H that can enhance the ADC's input range twice to the all its op-amp's output ranges. By measurements of the fabricated ADC, a 2.0-V_{PP} full-swing input operation and a 57.5-dB SNDR with a 0.18-pJ/step FOM were obtained at a 1-V supply.

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