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Multi-Level Pulse Width Modulation to Boost the Power Efficiency of Switching Amplifiers for Analog Signals with Very High Crest Factor

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***Abstract*—**The main goal of this paper is to develop a switching amplifier with optimized power efficiency for analog signals with a very high crest factor such as audio or DSL signals. Theoretical calculations show that a switching amplifier architecture based on multi-level pulse width modulation outperforms all other types of linear or switching amplifiers in that respect. Simulations on a 2 W multi-level switching audio amplifier, designed in a 50 V 0.35 μm IC technology, confirm its superior performance in terms of power efficiency. A real silicon implementation of this audio amplifier design is currently underway to provide experimental validation.

***Keywords*—**Audio amplifier, multi-level switching amplifier, power efficiency, pulse width modulation, PWM, self-oscillating amplifier.

I. Introduction

THE traditional approach to amplify analog signals is by using class-A or class-AB amplifiers. Their excellent linearity is beyond any doubt a major advantage, but they exhibit an extremely poor power efficiency when it comes to amplify analog signals with a high crest factor, which is defined as the ratio of the signal's peak value to its effective or root mean square (RMS) value. Interesting examples are audio signals or Discrete Multi-Tone (DMT) signals used in Digital Subscriber Line (DSL) equipment for high-speed internet communication. Those signals have most of the time a low-amplitude noisy behaviour, while peaks or bursts of high amplitude only occur sporadically. In order to guarantee distortion-free amplification of those signals, the supply voltage of the amplifier must be chosen sufficiently high according to the highest amplitudes occurring in the signal. The average power efficiency, however, will predominantly be determined by the low-amplitude section of the signal. As a linear class-A or class-AB amplifier exhibits a very low power efficiency when the signal amplitude is much smaller than the supply voltage, it is not surprising that the average power efficiency of these types of linear amplifiers for analog signals with high crest factor is disappointingly low, typically well below 15%.

A lot of effort has been spent to remedy this problem and the most effective solution is to use switching amplifiers rather than linear amplifiers. As the output transistors in a switching amplifier behave like almost ideal solid-state switches instead of linear amplifying devices, the power efficiency gets a significant boost. This paper explains the operation and shows simulation results of a multi-level switching amplifier that outperforms other types of linear and switching amplifiers in terms of power efficiency, especially for analog signals that suffer from a high crest factor.

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II. Amplifier Architecture

The most widely employed switching amplifier type is the class-D amplifier, also known as a class-S amplifier. It contains a binary high-voltage switching output stage, in single-ended or balanced configuration, that produces an amplified 2-level Pulse-Width-Modulated (PWM) approximation of the original analog signal by means of proper feedback, filtering and control. The switching frequency can be set to a fixed value or can be generated automatically in a self-oscillating loop configuration. A low-loss passive LC low-pass filter then eliminates the switching frequency and its harmonics from the output signal, thereby delivering the desired amplified analog signal to the load. This type of class-D switching amplifier has been successfully demonstrated in various applications, such as audio and DSL equipment [1]-[3].

Although the power efficiency of class-D amplifiers can theoretically be very high, the large switching amplitude of the 2-level PWM output voltage can cause considerable dynamic switching losses, especially at high oscillation frequency, and the associated high-frequency currents, whose amplitude is determined by the LC low-pass filter's input impedance, also induce additional conduction losses in the non-zero on-state resistance of the output transistors. In case the analog signal has a very high crest factor, these extra sources of heat dissipation can exceed the average signal power in the load, hence yielding an unsatisfactory overall power efficiency.

It is clear that the power efficiency could significantly be improved by reducing the switching amplitude of the amplifier's PWM output voltage. But, in order to maintain the required dynamic range for analog signals with high crest factor, somehow the discrete switching levels of the PWM output voltage should become adaptable to the instantaneous analog signal strength. By this way, a multi-level switching amplifier is obtained.

Just a limited number of multi-level switching amplifier designs are discussed in literature. Some of them are based on a sophisticated architecture wherein super-capacitors or even rechargeable batteries are used as "flying batteries" to power

multiple series-connected switching cells [4]. A less complex alternative architecture, where the "flying batteries" are being replaced by a set of fixed supply voltages, is shown in Fig. 1 and is based on a high-voltage multiple-input single-output analog multiplexer [5].

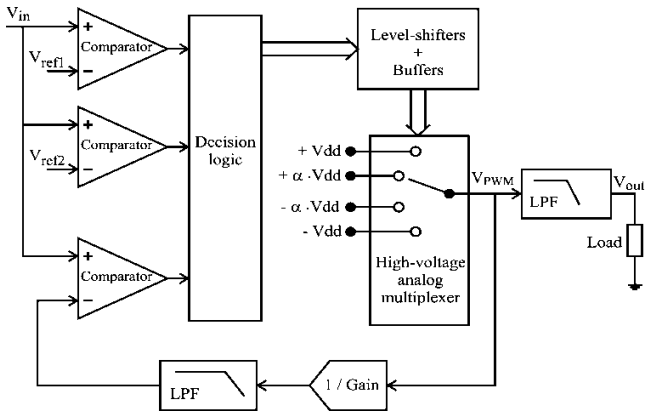

Fig. 1 Block diagram of a multi-level switching amplifier

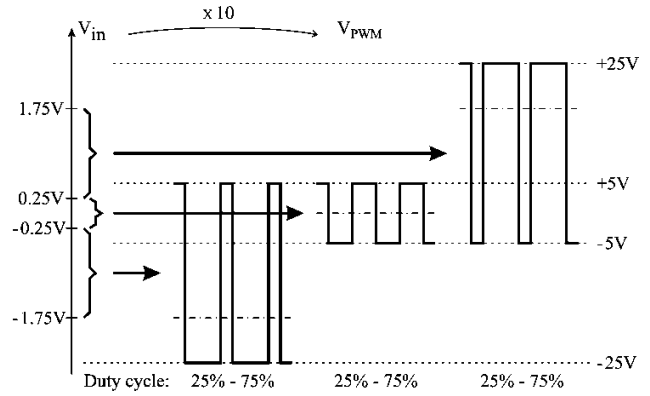

Fig. 2 Optimal switching strategy for a multi-level switching amplifier

In this particular example, the multiplexer consists of four bidirectional high-voltage solid-state switches, normally implemented as symmetrical Double-diffused or Drain-extended MOS (DMOS) transistors and generates by means of a self-oscillating feedback loop an amplified 4-level PWM approximation of the original analog input signal. The decision logic, in combination with two comparators that continuously monitor the instantaneous strength of the input signal (by comparing it to two reference voltages), decides between which of the four discrete supply voltage levels the analog multiplexer should switch in order to achieve minimal power losses in the output transistors. In case where the signal amplitude is low, the supply voltages $-\alpha \cdot Vdd$ and $+\alpha \cdot Vdd$ will be selected, wherein α represents a fraction much smaller than 1. This produces minimal switching losses and minimal conduction losses due to the high-frequency switching currents during most of the time. Only when the comparators detect increased signal strength at the input, the decision logic will activate one of the supply voltages –Vdd or +Vdd, depending on the signal polarity. Several switching strategies are still possible, but the one depicted in Fig. 2 offers the best trade-off between overall power efficiency and linearity [5]. The PWM waveforms in Fig. 2 correspond to the specific case where Vdd = 25 V, α = 0.2, amplifier gain = 10, and a 25% - 75% duty cycle range.

It should also be noted that this type of multi-level switching amplifier can easily be seen as a discrete version of the so-called linear class-G amplifier, being essentially a standard linear class-AB amplifier, whose output stage will be powered by a significantly reduced supply voltage as soon as the input signal amplitude drops below a certain predefined limit.

III. Power Efficiency Calculation

When comparing the performance of the multi-level switching amplifier to other types of switching or linear amplifiers, the power efficiency will obviously be the most important figure-of-merit. In previous work [5], the following equation was derived for the power efficiency η of the multi-level switching amplifier according to Fig. 1 under DC excitation at the amplifier input:

$$\eta = \frac{1}{1 + \frac{r}{R} + \frac{r \cdot R}{2V_{DC}^2} \cdot \sum_{n=1}^{\infty} \frac{a_n^2}{|Z_{in}(nf_S)|^2}}$$

V_{DC} is the amplified DC voltage across the load resistance R, while r represents the equivalent on-state resistance of the DMOS transistors used as bidirectional solid-state switches in the multiplexer. Each coefficient a_n is the amplitude of the n^{th} harmonic in the Fourier series expansion of the multiplexer's PWM output voltage (before the LC low-pass filter), $Z_{in}(f)$ is the frequency-dependent input impedance of the LC low-pass filter, and f_s is the switching frequency. It is clear that the values of the Fourier coefficients a_n will depend on the DC output voltage V_{DC} as well as on the two selected multiplexer supply voltages according to the switching strategy of Fig. 2. Also note that this formula takes all the conduction losses into account (caused by the DC load current and the high-frequency switching currents in the multiplexer transistors), while the switching power losses (due to the fact that parasitic capacitances have to be charged and discharged continuously at high speed) are neglected.

Where the calculations in previous work [5] focused entirely on pure DC excitation of the multi-level switching amplifier, this paper extends the analysis towards other types of analog input signals (sine wave, audio, DSL, …). In such cases the overall power efficiency can be estimated by doing the mathematics all over, using the probability density function of the analog signal under consideration. This is a kind of quasi-static approximation, which implies that the switching frequency of the amplifier should be much higher than the signal bandwidth, which is a valid assumption in most switching amplifier applications. As an example, this analysis was performed for sinusoidal excitation of the amplifier. Fig. 3 shows the calculated power efficiency of the multi-level switching amplifier as a function of the amplitude of the sinusoidal output voltage and compares it to other relevant amplifier types (switching class-D, linear class-AB and linear

class-G). The following parameter values were used in the power efficiency calculations of Fig. 3: Vdd = 25V, α = 0.2, gain = 10, R = 10·r, and $f_s = 5 \cdot f_c$ where f_c represents the 3dB cut-off frequency of the LC low-pass filter having a third-order Butterworth characteristic.

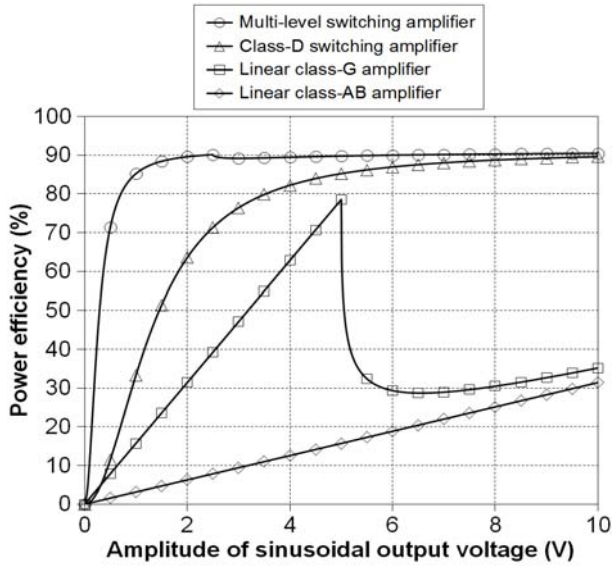

Fig. 3 Calculated power efficiency: comparison between different types of switching and linear amplifiers under sinusoidal excitation

From Fig. 3, we learn that the performance of the multi-level switching amplifier is by far superior compared to all other amplifier types. Especially at low signal amplitudes, where it really matters when it comes down to amplifying analog signals with very high crest factor, the supremacy of the multi-level switching amplifier is overwhelming. At a sinusoidal amplitude of 2V, it still has a power efficiency of 90%, very similar to the values at higher signal strength, whereas the efficiency of the class-D switching amplifier has already dropped to 64%, and the efficiency of the linear class-G and class-AB amplifiers has collapsed to extremely low levels of 31% and 6%, respectively.

It was already mentioned that the switching power losses (also called dynamic power losses), attributed to the continuous charging and discharging of parasitic capacitances at the switching frequency, have been neglected so far. To assess their impact on the multi-level switching amplifier performance, the calculation of the power efficiency should be modified. Under DC excitation at the amplifier input the resulting formula for the power efficiency becomes:

$$\eta = \frac{1}{1+\frac{r}{R}+\frac{r \cdot R}{2{V_{DC}}^2}\cdot\sum_{n=1}^{\infty}\frac{{a_n}^2}{|Z_{in}(nf_S)|^2}+\frac{4 f_S \cdot R \cdot C}{{V_{DC}}^2}\cdot(V_B - V_A)^2}$$

In this equation, the last term in the denominator represents the impact of the switching power losses, wherein C is the parasitic capacitance of a single multiplexer switch in the off-state, while V_A and V_B are the two switching voltage levels for a given DC output voltage V_{DC} across the load according to the optimal switching strategy of Fig. 2.

To evaluate the impact of the switching power losses, we introduce a new parameter, the "relative switching loss factor" λ, defined as the ratio of the switching power losses in the multiplexer switches to the total (i.e. switching + conduction) power losses in the multiplexer switches. Due to the presence of the off-state parasitic capacitance C and the switching frequency f_s in the expression for the switching power losses, it is clear that the relative switching loss factor λ will be highly technology- and application-dependent. Let us consider one specific practical case, corresponding to the 2 W audio amplifier application that will be discussed in the next section. It concerns a multi-level switching amplifier design in the 50 V 0.35 µm I3T50 technology of ON Semiconductor, wherein a symmetrical p-channel DMOS switch with an on-state resistance of r = 10 Ω possesses an off-state parasitic capacitance of C = 1.78 pF. When operating at a switching frequency of f_s = 100 kHz, the graph of the relative switching loss factor λ in Fig. 4 is obtained under DC excitation (while maintaining the parameters from Fig. 3: Vdd = 25V, α = 0.2, gain = 10, R = 10·r, and $f_s = 5 \cdot f_c$).

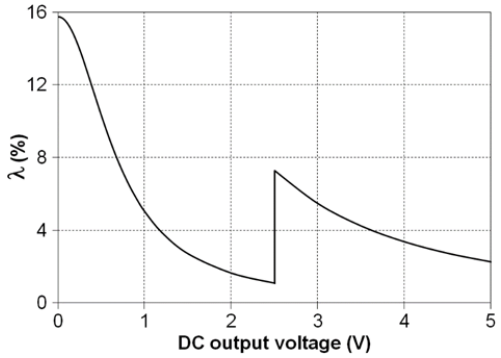

Fig. 4 Calculated relative switching loss factor λ in a multi-level switching amplifier under DC excitation

Fig. 4 proves that the relative contribution of the switching power losses in the total amount of power losses is reasonably small for this particular technology and application, even at low signal levels. This analysis was performed under DC excitation but remains equally valid for sinusoidal excitation. As a consequence, the impact of the switching power losses on the power efficiency calculations in Fig. 3 can be considered as being negligible. But, be aware of the fact that the impact of the switching power losses may be more important when other IC technologies are employed, and/or other applications are targeted.

IV. Initial Circuit Simulations

In order to get a reliable confirmation of the discussed theoretical calculations, a prototype version of a multi-level switching amplifier was designed, in which the optimal switching strategy of Fig. 2 was adopted to drive the amplifier architecture of Fig. 1. The targeted application was a 2 W audio amplifier with a useful signal bandwidth of 20 kHz, monolithically integrated in the 50 V 0.35 µm I3T50 smart

power IC technology of ON Semiconductor.

For the integration of the bidirectional switches in the 4-level high-voltage analog multiplexer, the circuit schematic of Fig. 5 has been used. The switch actually consists of two p-channel DMOS transistors, symmetrically coupled one to the other, between the switch nodes V_a and V_b. The gate electrodes of these two p-channel DMOS devices are driven by an ultra-low-power level-shifter, based on a dynamic charge control principle [6], in order to minimize the extra power consumption in the driving circuitry. Originally these ultra-low-power dynamically controlled level-shifters were developed for driving high-voltage bistable LC-based flat-panel displays [6], [7], but they are also perfectly suitable for the design of this 2 W switching audio amplifier.

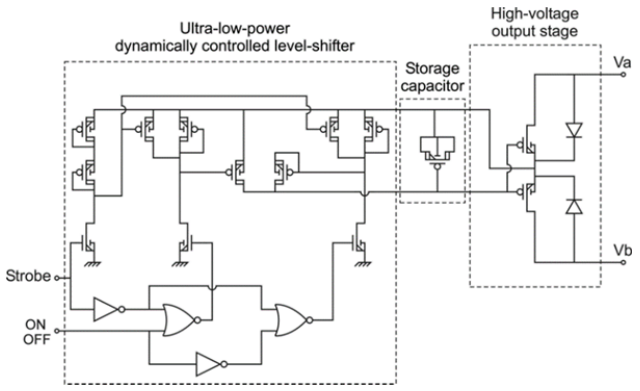

Fig. 5 Bidirectional high-voltage analog switch driven by a dynamically controlled level-shifter

A simulated current-versus-voltage characteristic of such a bidirectional high-voltage analog switch in the on-state, having an equivalent on-state resistance of r = 10 Ω, is shown in Fig. 6. The two p-channel DMOS transistors in the output stage each have an effective channel width of 16.8 mm with a multi-finger-shaped physical layout. Fig. 6 evidences that the activated switch indeed resembles a 10 Ω resistor at voltages below 5 V but behaves rather like a constant current source at higher voltage levels, which is due to saturated operation of the p-channel DMOS devices at high source-drain voltages. Fig. 6 also illustrates the perfectly symmetrical behaviour of the switch, which is quite logical in view of the symmetrical structure of the output stage between the switch nodes V_a and V_b in Fig. 5.

During the design of the 2 W multi-level switching audio amplifier the following system parameter values were specified: Vdd = 25 V, $\alpha = 0.2$, gain = 10, R = 100 Ω, r = 10 Ω, f_s = 100 kHz, f_c = 20 kHz, in accordance with the values used in the power efficiency calculations. The operation of the designed amplifier was thoroughly verified by means of Spectre simulations, and the obtained simulated power efficiency under 1 kHz sinusoidal excitation is depicted in Fig. 7 as a function of the sinusoidal output amplitude. It should be noted that all power losses, including the power dissipation in the dynamically controlled level-shifters that drive the bidirectional high-voltage analog switches as well as the power consumption in all other feedback and control circuitry, were taken into account during these Spectre circuit simulations.

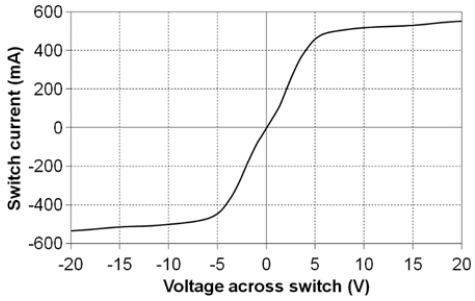

Fig. 6 Simulated current-versus-voltage characteristic of a dynamically controlled bidirectional high-voltage analog switch in the on-state

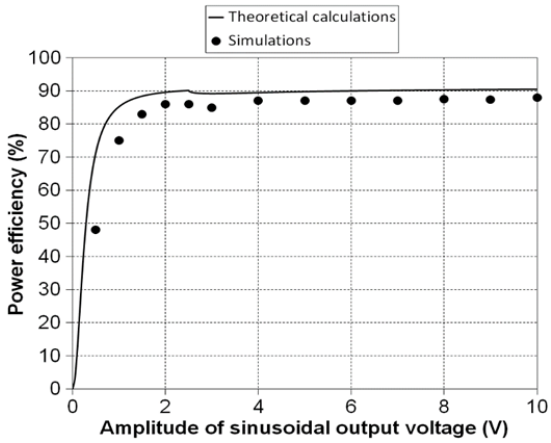

Fig. 7 Comparison between the simulated and theoretically calculated power efficiency of the 2 W multi-level switching audio amplifier under 1 kHz sinusoidal excitation

From a comparison between the simulated power efficiency and the previously discussed theoretically calculated values (both are plotted in Fig. 7), we learn that the simulated power efficiency of the multi-level switching amplifier is somewhat lower than what was theoretically predicted, especially in the range of low signal amplitudes. From the analysis of the relative switching loss factor λ in Fig. 4, we know that the impact of the switching power losses is practically negligible, even at low signal levels, and hence, switching power losses cannot be held responsible for the mismatch between simulations and theoretical calculations in Fig. 7. Consequently, the most probable causes of the mismatch are the additional power dissipation in the dynamically controlled level-shifters that drive the multiplexer switches and the power consumption in the feedback loop (including the low-pass loop filter, the comparators and the decision logic from Fig. 1) that is responsible for generating the multi-level PWM approximation of the analog input signal. But, even if the simulated efficiency is somewhat lower than theoretically predicted, the simulation data from Fig. 7 reveal excellent performance of the designed 2 W multi-level switching audio amplifier as far as power efficiency is concerned.

V. Real Silicon Implementation

To validate the very promising initial circuit simulation results, the designed 2W multi-level switching audio amplifier will soon be integrated in real silicon. To that purpose, this IC design in the 50 V 0.35 μm I3T50 technology of ON Semiconductor will be submitted to the Multi-Project-Wafer (MPW) IC service of Europractice for low-cost fabrication of prototype samples. As soon as the chip samples return to the laboratory, they will be extensively tested, and the experimental data will be compared to the simulation results.

VI. Conclusion

Theoretical calculations have proven that a multiplexer-based switching amplifier architecture employing multi-level pulse width modulation exhibits a much higher power efficiency than the conventional linear class-AB or class-G amplifiers as well as the standard class-D switching amplifier, especially at low signal amplitudes. This superior performance in terms of power efficiency is particularly striking when it comes to amplifying analog signals with a very high crest factor, such as audio or DMT-modulated DSL signals. Circuit simulations on a 2 W audio amplifier, designed according to this multi-level switching amplifier architecture in the 50 V 0.35 μm I3T50 smart power technology of ON Semiconductor, confirm the superior power efficiency of this new type of amplifier. A real silicon implementation of this 2 W multi-level switching audio amplifier is currently underway.

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