The 4th International Symposium on More Electric Aircraft Technology (MEA 2017)

8–9 November 2017

CMV reduction for five-level ANPC converter by PS-PWM strategy

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Published in *The Journal of Engineering*; Received on 10th January 2018; Accepted on 17th January 2018

Abstract: Five-level active neutral point clamped (ANPC) converter has become one of the most attractive topologies in industry applications, especially in the field of the motor drive. A novel common-mode voltage (CMV) reduction strategy for five-level ANPC is presented, which is based on the phase-shifted pulse-width modulation (PS-PWM). A basic PS-PWM method is presented, which can realise the NP voltage and the flying capacitor (FC) voltages balance. Moreover, a general CMV reduction method is summarised. The proposed CMV reduction strategy can minimise the CMV by injecting zero-sequence voltage to the modulation wave and it does not affect the ability of NP voltage and FC voltages balance. The validity of the proposed CMV reduction method based on PS-PWM strategy is verified by simulation.

1 Introduction

Multilevel converters have been widely used in industry applications, especially in the field of energy, transportation etc. Compared to the traditional two-level converters, multilevel converters have so many advantages such as lower current harmonics, lower dv/dt and so on. Three-level neutral point clamped (NPC) [1, 2], flying capacitor (FC), cascaded H-bridge (CHB) [3, 4] and modular multilevel converter (MMC) [5] are mature topologies that have been used in industry applications. However, in the medium-voltage motor drives such as more electric aircraft's 540 V high-voltage DC system, NPC and FC need more diodes or capacitors which will increase the number of devices enormously. So, NPC or FC converters are hard to be applied in medium-voltage or high-voltage motor drives. CHB converters need an isolated transformer to supply DC power, the weight and volume of which are greatly increased. MMC is widely applied in high-voltage DC system, but when it is used to drive motor, there will be low-frequency fluctuation in the capacitors [6].

Five-level active NP clamped (ANPC) converter is one of the most attractive topologies that can be used in medium-voltage or high-voltage motor drives, because of its lower costs, lower volume and the simplicity of control. NP voltage balance, FCs voltages balance and common-mode voltage (CMV) reduction are three key concerns that need to be considered in five-level ANPC converter. NP voltage balance and FC voltages are related to the nominal operation of the converter, while the CMV can cause the leakage current and voltage stresses in the machine, which will reduce the life of the machine bearing [7]. So it is very important to reduce or eliminate the effect of the CMV on the machine.

Five-level ANPC converter has been extensively researched and the research hotpots include the NP voltage balance, the FC voltage balance, the CMV reduction etc. An space vector pulse-width modulation (SVPWM) method based on the line voltage coordinate system can achieve the balance of NP voltage and FC voltages by selecting a proper switching sequence. However, the SVPWM method is too complicated to achieve and the CMV is only limited to one-quarter of the DC bus voltage [8, 9]. In addition, a phase-shifted PWM (PS-PWM) method is proposed to control the NP voltage by injecting the zero-sequence voltage (ZSV) and to control the FC voltages by adjusting the duty of different switches. The CMV is still too high [10, 11]. To suppress the CMV, some researches focusing on the CMV have been developed. An SVPWM method that utilises only 55 voltage vectors to reduce the CMV to $u_{dc}/12$ has been proposed, where u_{dc} is the DC bus voltage. However by this strategy, the NP voltage cannot be controlled and it can bring potential threats to the safe operation of the whole system [12]. On the basis of that an SVPWM method that utilises 55 vectors to suppress CMV is proposed in [13], but it increases two cases that will increase the number of vectors up to 79 actually. This method is so difficult to realise compared with the sinusoidal PWM (SPWM) method. As for the method that is based on SPWM to reduce the CMV, it has not been researched fully yet because it is so vague by injecting the ZSV.

This paper proposes a novel CMV suppression method based on PS-PWM strategy for five-level ANPC converter. The basic principle of PS-PWM is introduced and a general CMV reduction method is proposed in this paper. By injecting the limited ZSV, the CMV can be suppressed to 1/12 of the DC bus voltage. It can also realise the balance control of the NP voltage and the balance control of the FC voltages, while the minimum value of CMV will be $u_{dc}/6$.

This paper is organised as follows. Section 2 will present the structure of five-level ANPC converter and describe the principle control strategies based on PS-PWM, which includes the NP voltage control and the FC voltages control. The general CMV reduction method is discussed in Section 3. A novel and simple PS-PWM method for reducing the CMV is developed and it can achieve the NP voltage control and FC voltages control. Section 4 shows the simulation results of the proposed method. Finally, the conclusions are drawn in Section 5.

2 Five-level ANPC converter

2.1 Structure of five-level ANPC converter

A phase-leg structure of five-level ANPC converter is shown in Fig. 1, which consists of 11 switches and five capacitors (assuming that each switch and capacitor bears a voltage of $u_{dc}/4$). In Fig. 1, C_1 and C_2 represent the upper and lower DC bus capacitors, respectively, and C_{fx} is the FC of this phase-leg, where x represents phase sign

doi: 10.1049/joe.2018.0020

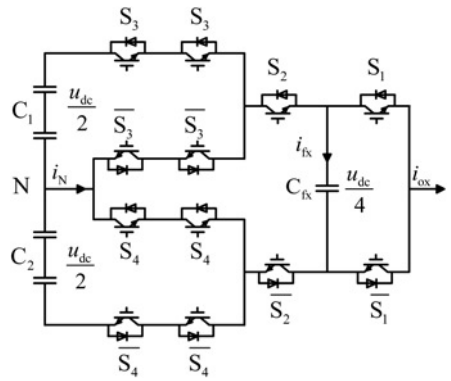

Fig. 1 *Phase-leg structure of five-level ANPC converter*

Table 1 Switching states of five-level ANPC converter

S_{1x}	S_{2x}	S_{3x}	S_{4x}	i_{Nx}	I_{fx}	u_{ox}	Switching state
0	0	0	0	0	0	$-u_{dc}/2$	V0
1	0	0	0	0	$-i_o$	$-u_{dc}/4$	V1
0	1	0	0	i_o	i_o	$-u_{dc}/4$	V2
1	1	0	0	i_o	0	0	V3
0	0	1	1	i_o	0	0	V4
1	0	1	1	i_o	$-i_o$	$u_{dc}/4$	V5
0	1	1	1	0	i_o	$u_{dc}/4$	V6
1	1	1	1	0	0	$u_{dc}/2$	V7

(a, b or c). i_{Nx} and i_{fx} represent the NP current and FC current separately, and in this paper the current direction is defined in Fig. 1.

As shown in Fig. 1, five-level ANPC converter can be considered as a two-level converter plus a three-level FC clamped converter. In this topology, S_1 and S_2 operate at high frequency, whereas S_3 and S_4 operate at a fundamental frequency, which can reduce the switching loss. In addition, there are four complementary switch pairs that include (S_1, $\overline{S}_1$), (S_2, $\overline{S}_2$), (S_3, $\overline{S}_3$), and (S_4, $\overline{S}_4$). Table 1 lists all the possible switching states of a single-phase, which includes five different voltage levels: $u_{dc}/2$, $u_{dc}/4$, 0, $-u_{dc}/4$ and $-u_{dc}/2$.

As we can see from Table 1, S_3 and S_4 require the same switching signal, so there are only three switching signals that can be controlled. Moreover, the switching states V1 and V2, V3 and V4, V5 and V6 have the same output voltage, which will be discussed later.

2.2 PS-PWM strategy for five-level ANPC

The PS-PWM strategy is adopted to generate PWM signals for five-level ANPC converter. The real output voltage U_{ox} can be described by the switching signals by (1), and we can get the average model as expressed in (2)

$$U_{ox} = \frac{u_{dc}}{4}\left[2\left(S_{3x}-1\right)+S_{1x}+S_{1x}\right] \tag{1}$$

$$U_{ox} = \begin{cases} d_{1x}+d_{2x} & S_{3x}=1 \\ d_{1x}+d_{2x}-2 & S_{3x}=0 \end{cases} \tag{2}$$

where d_{1x} and d_{2x} represent the switching duty of S_{1x} and S_{2x}, respectively, and u_{ox} is the per-unit output voltage whose value is between −2 and 2. The switching state of S_{3x} depends on the polarity of u_{ox}, so it can be described as below:

$$S_{3x} = \begin{cases} 0 & u_{ox}<0 \\ 1 & u_{ox}>0 \end{cases} \tag{3}$$

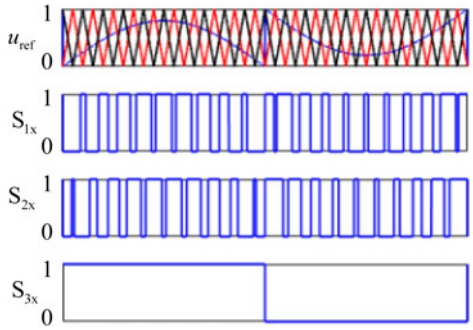

Fig. 2 *PS-PWM for five-level ANPC*

Since the PS-PWM is chosen to generate the switch signals of S_{1x} and S_{2x}, d_{1x} is equal to d_{2x}, and the reference modulation wave is described as (4) according to (2)

$$u_{\mathrm{ref}x} = \begin{cases} \dfrac{u_{ox}}{2} & S_{3x}=0 \\ \dfrac{u_{ox}}{2}+1 & S_{3x}=1 \end{cases} \tag{4}$$

where $u_{\mathrm{ref}x}$ represents the reference modulation wave, whose value is between 0 and 1. The principle of PS-PWM for five-level ANPC converter is depicted by Fig. 2. The modulation wave is compared with the carrier wave, which decides the switching states of S_{1x} and S_{2x}.

2.3 Control of the NP voltage

From Table 1, it is obvious that only V2, V3, V4 and V5 have an influence on the NP current. So, the relationship between the NP current of the single-phase i_{Nx} and the switching state is described by switching mode as below:

$$i_{Nx} = \begin{cases} (1-S_{2x})\,i_{ox} & S_{3x}=1 \\ S_{2x}\,i_{ox} & S_{3x}=0 \end{cases} \tag{5}$$

When it comes to the average model, (5) can be changed as below:

$$i_{Nx} = \begin{cases} (1-d_{2x})\,i_{ox} & S_{3x}=1 \\ d_{2x}\,i_{ox} & S_{3x}=0 \end{cases} \tag{6}$$

The relationship between i_{Nx} and u_{ox} can be described as (7) according to (1), (3) and (6)

$$i_{Nx} = (1-|u_{ox}|/2)\,i_{ox} \tag{7}$$

In a typical three-phase system, the NP current can be summarised as below:

$$\begin{aligned} i_N &= (1-|u_{oa}|/2)i_{oa}+(1-|u_{ob}|/2)i_{ob}+(1-|u_{oc}|/2)i_{oc} \\ &= -(|u_{oa}|i_{oa}+|u_{ob}|i_{ob}+|u_{oc}|i_{oc})/2 \end{aligned} \tag{8}$$

where i_N are the sum of i_{Na}, i_{Nb} and i_{Nc}. After the injection of ZSV, the NP current must be changed and it can be described and

simplified as below:

$$\begin{aligned} i_N{}' &= -\left(|u_{oa}{}'|i_{oa} + |u_{ob}{}'|i_{ob} + |u_{oc}{}'|i_{oc}\right)/2 \\ &= \begin{cases} -\left(u_{omax}{}'i_{omax} + u_{omid}{}'i_{omid} - u_{omin}{}'i_{omin}\right)/2, & u_{omid}{}' > 0 \\ -\left(u_{omax}{}'i_{omax} - u_{omid}{}'i_{omid} - u_{omin}{}'i_{omin}\right)/2, & u_{omid}{}' < 0 \end{cases} \\ &= \begin{cases} i_N - u_z\left(i_{omax} + i_{omid} - i_{omin}\right)/2, & u_{omid}{}' > 0 \\ i_N - u_z\left(i_{omax} - i_{omid} - i_{omin}\right)/2, & u_{omid}{}' < 0 \end{cases} \end{aligned} \tag{9}$$

where $u_{omax}{}'$, $u_{omid}{}'$ and $u_{omin}{}'$ represent the maximum value, middle value and minimum value of the $u_{ox}{}'$, respectively, and i_{omax}, i_{omid} and i_{omin} correspond to the $u_{omax}{}'$, $u_{omid}{}'$ and $u_{omin}{}'$. It is obvious that the NP current $i_N{}'$ is linearised to the ZSV u_z according to (9). To ensure that S_{3x} operates at a fundamental frequency, the ZSV must be limited by

$$-u_{\text{refmin}} \le \frac{u_z}{2} \le 1 - u_{\text{refmax}} \tag{10}$$

where u_{refmax} and u_{refmin} represent the maximum value and minimum value of the u_{refx}. Then, the maximum and minimum values of u_z can be calculated by (10)

$$\begin{cases} u_{z\text{max}} = 2(1 - u_{\text{refmax}}) \\ u_{z\text{min}} = -2\,u_{\text{refmin}} \end{cases} \tag{11}$$

Assuming that the upper DC bus capacitor's voltage is u_{dc1} and the lower is u_{dc2}, the needed NP current can be calculated by (12) if we want to balance the NP voltage to the normal value in a control period T_s

$$i_{\text{NP\_ref}} = (C_1 + C_2)\frac{u_{\text{dc2}} - u_{\text{dc1}}}{T_s} \tag{12}$$

According to (9) and (12), the optimal ZSV can be calculated by linear interpolation by (13), which means the ZSV is non-key ZSV. There is another method to calculate the ZSV by (14), which will make $u_{ox}{}'$ an integer

$$u_{z\text{ref}} = \frac{u_{z\text{max}} - u_{z\text{min}}}{I_{\text{NPmax}} - I_{\text{NPmin}}} I_{\text{NPref}} + \frac{u_{z\text{min}} I_{\text{NPmax}} - u_{z\text{max}} I_{\text{NPmin}}}{I_{\text{NPmax}} - I_{\text{NPmin}}} \tag{13}$$

$$u_{z\text{ref}} = \begin{cases} u_{z\text{max}} & |i_{\text{NPmax}} - i_{\text{NPref}}| < |i_{\text{NPmin}} - i_{\text{NPref}}| \\ u_{z\text{min}} & |i_{\text{NPmax}} - i_{\text{NPref}}| > |i_{\text{NPmin}} - i_{\text{NPref}} \end{cases} \tag{14}$$

where i_{NPmax} and i_{NPmin} are calculated by (9) using $u_{z\text{max}}$ and $u_{z\text{min}}$, respectively.

2.4 Control of the FC voltages

From Table 1, we can find that the switching states (V1, V2) and (V5, V6) have an opposite influence on the FC voltages, though they output the same voltage. The relationship between the i_{fx} and the switching state is given by the equation below:

$$i_{fx} = (S_{1x} - S_{2x})\,i_{ox} \tag{15}$$

Equation (15) can be changed to the average model as (16) which consists of the duties of S_{1x} and S_{2x}

$$i_{fx} = (d_{1x} - d_{2x}) \cdot i_{ox} \tag{16}$$

Therefore, the FC voltages can be balanced by adjusting the duties of S_{1x} and S_{2x} according to the output current's polarity. Balance factor k is introduced to achieve this function and the modified duty can be calculated by

$$\begin{cases} d_{1x\_\text{real}} = (1 - k)\,d_{1x} \\ d_{2x\_\text{real}} = (1 - k)\,d_{2x} \end{cases} \tag{17}$$

3 CMV reduction strategy

3.1 General method for CM reduction

CMV is the voltage between the midpoint O of the three phases and the midpoint N of the DC bus. It can be defined as u_{cm} which is depicted in Fig. 3 and defined as below:

$$u_{\text{cm}} = \frac{u_{\text{AN}} + u_{\text{BN}} + u_{\text{CN}}}{3} \tag{18}$$

It is easy to analyse the CMV by SVPWM strategy because the CMV can be controlled by selecting the specific switching states which will produce lower CMV. However, when it comes to PS-PWM method, the CMV is not easy to analyse by the modulation wave.

To get the general method for CMV reduction, three reference voltages (after the ZSV is injected) can be described as the sum of an integer and a positive decimal by the equation below:

$$u_{ox}{}' = \left[u_{ox}{}'\right] + \left\{\left[u_{ox}{}'\right]\right\} \tag{19}$$

For PS-PWM, the output phase voltage alters between two adjacent voltage levels in a switching period and the instantaneous value of phase voltage can only be $u_{\text{dc}}[u_{ox}']/4$ or $u_{\text{dc}}([u_{ox}']+1)/4$. If the injected ZSV makes the value of reference modulation wave exactly an integer, the ZSV at this point is the key ZSV. Otherwise, it is the non-key ZSV. Fig. 4 shows the generation of

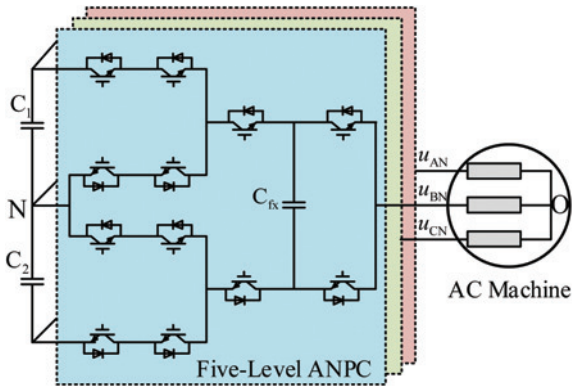

Fig. 3 *CMV of five-level ANPC converter*

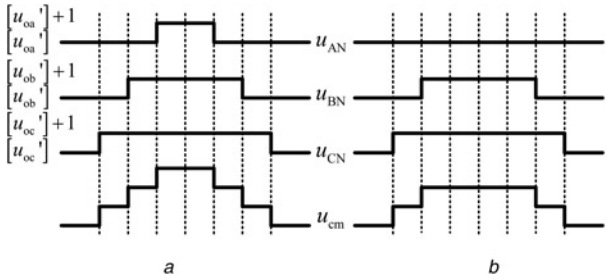

Fig. 4 *Generation of CMV by SPWM strategy*

Table 2 CMV values of five-level ANPC converter

$[u_{oa}']+[u_{ob}']+[u_{oc}']$	CMV values	
	Key ZSV	Non-key ZSV
−6	$-u_{dc}/2$, $-5u_{dc}/12$, $-u_{dc}/3$	$-u_{dc}/2$, $-5u_{dc}/12$, $-u_{dc}/3$, $-u_{dc}/4$
−5	$-5u_{dc}/12$, $-u_{dc}/3$, $-u_{dc}/4$	$5u_{dc}/12$, $-u_{dc}/3$, $-u_{dc}/4$, $-u_{dc}/6$
−4	$-u_{dc}/3$, $-u_{dc}/4$, $-u_{dc}/6$	$-u_{dc}/3$, $-u_{dc}/4$, $-u_{dc}/6$, $-u_{dc}/12$
−3	$-u_{dc}/4$, $-u_{dc}/6$, $-u_{dc}/12$	$-u_{dc}/4$, $-u_{dc}/6$, $-u_{dc}/12$, 0
−2	$-u_{dc}/6$, $-u_{dc}/12$, 0	$-u_{dc}/6$, $-u_{dc}/12$, 0, $u_{dc}/12$
−1	$-u_{dc}/12$, 0, $u_{dc}/12$	$-u_{dc}/12$, 0, $u_{dc}/12$, $u_{dc}/6$
0	0, $u_{dc}/12$, $u_{dc}/6$	0, $u_{dc}/12$, $u_{dc}/6$, $u_{dc}/4$
1	$u_{dc}/12$, $u_{dc}/6$, $u_{dc}/4$	$u_{dc}/12$, $u_{dc}/6$, $u_{dc}/4$, $u_{dc}/3$
2	$u_{dc}/6$, $u_{dc}/4$, $u_{dc}/3$	$u_{dc}/6$, $u_{dc}/4$, $u_{dc}/3$, $5u_{dc}/12$
3	$u_{dc}/4$, $u_{dc}/3$, $5u_{dc}/12$	$u_{dc}/4$, $u_{dc}/3$, $5u_{dc}/12$, $u_{dc}/2$
4	$u_{dc}/3$, $5u_{dc}/12$, $u_{dc}/2$	$u_{dc}/3$, $5u_{dc}/12$, $u_{dc}/2$

CMV in a switching period by SPWM strategy in two different ways.

(i) If the voltage is key ZSV, CMV will have three values: $u_{dc}([u_{oa}']+[u_{ob}']+[u_{oc}'])/12$, $u_{dc}([u_{oa}']+[u_{ob}']+[u_{oc}']+1)/12$ and $u_{dc}([u_{oa}']+[u_{ob}']+[u_{oc}']+2)/12$. If the voltage is non-key zero-sequence voltage (ZVS), CMV will have four values: $u_{dc}([u_{oa}']+[u_{ob}']+[u_{oc}'])/12$, $u_{dc}([u_{oa}']+[u_{ob}']+[u_{oc}']+1)/12$, $u_{dc}([u_{oa}']+[u_{ob}']+[u_{oc}']+2)/12$ and $u_{dc}([u_{oa}']+[u_{ob}']+[u_{oc}']+3)/1$.

(ii) Owing to $-2 \le u_{ox}' \le 2$, the value of $[u_{oa}']+[u_{ob}']+[u_{oc}']$ after the ZSV injected will be limited between −6 and 4.

The possible CMV values can be summarised in Table 2.

If there is no ZSV injected, the values of $[u_{oa}']+[u_{ob}']+[u_{oc}']$ are −1 or −2. So according to Table 2, the CMV value will be $\pm u_{dc}/6, \pm u_{dc}/12$ and 0. In this paper, the key ZVS is selected to balance the NP voltage and to reduce the CMV.

3.2 Restrictions of ZVS injection for CMV reduction

If ZSV is limited by (11), the value of $[u_{oa}']+[u_{ob}']+[u_{oc}']$ will be limited between −4 and 2. We defined this situation as case 1. In this situation, the value of CMV is limited to $\pm u_{dc}/3$, which is larger than the situation when there is no ZVS injection.

Assuming that the CMV value needs to be limited between $\pm u_{dc}/6$ if the ZVS is injected, the value of $[u_{oa}']+[u_{ob}']+[u_{oc}']$ must be valued as 0, −1 and −2. In other words, after the injection of ZVS, there must be the relationship

$$[u_{ao}] = [u_{ao}'],\ [u_{bo}] = [u_{bo}'],\ [u_{co}] = [u_{co}'] \tag{20}$$

To satisfy (20), the value of ZVS must be limited by another limiting condition as below:

$$\begin{cases} u_z \le \min(1+[u_{ao}]-u_{ao},\ 1+[u_{bo}]-u_{bo},\ 1+[u_{co}]-u_{co}) \\ u_z \ge -\min(u_{ao}-[u_{ao}],\ u_{bo}-[u_{bo}],\ u_c-[u_{co}]) \end{cases} \tag{21}$$

For instance, three-phase reference phase voltages are normalised, as $u_{ao}=0.6$, $u_{bo}=-0.9$ and $u_{co}=0.3$, the value of ZSV is limited to $-0.1 \le u_z \le 0.4$ by (19), while the value of ZSV ranges from −0.3 to 0.9 by (11). It is obvious that the value range of the ZSV is smaller, so the ability of NP voltage control will be weakened. This situation is defined as case 2.

Furthermore, if the magnitude of CMV needs to be limited to $\pm u_{dc}/12$, the value of $[u_{oa}']+[u_{ob}']+[u_{oc}']$ should be −1 by the injection of key ZSV according to Table 2. Moreover, this situation is defined as case 3.

On the basis of case 2, when the value of $[u_{oa}']+[u_{ob}']+[u_{oc}']$ is −2, it needs to take proper methods to convert −2 to −1. By further restricting the range of the ZSV, the limitation is described as equation below:

$$\begin{cases} u_z \le \min(1+[u_{ao}]-u_{ao},\ 1+[u_{bo}]-u_{bo},\ 1+[u_{co}]-u_{co}) \\ u_z \ge \min(1+[u_{ao}]-[u_{ao}],\ 1+[u_{bo}]-u_{bo},\ 1+[u_{co}]-u_{co}) \end{cases} \tag{22}$$

Combined to the previous limitation (19), the final limitation condition can be described as (21). For instance, if the three-phase reference voltage value is assumed as $u_{ao}=-0.6$, $u_{bo}=0.9$ and $u_{co}=-0.3$, there is only one value, $u_z=0.1$, that we can choose to satisfy the below equation:

$$u_z = \min(1+[u_{ao}]-u_{ao},\ 1+[u_{bo}]-u_{bo},\ 1+[u_{co}]-u_{co}) \tag{23}$$

When the value of $[u_{oa}']+[u_{ob}']+[u_{oc}']$ is zero, it needs to take proper methods to convert 0 to −1. The limitation equation is described as below:

$$\begin{cases} u_z < \min(1+[u_{ao}]-u_{ao},\ 1+[u_{bo}]-u_{bo},\ 1+[u_{co}]-u_{co}) \\ u_z \ge -\min(u_{ao}-[u_{ao}],\ u_{bo}-[u_{bo}],\ u_{co}-[u_{co}]) \end{cases} \tag{24}$$

Consider (19), the limitation condition is $u_z \ne \min(1+[u_{ao}]-u_{ao},\ 1+[u_{bo}]-u_{bo},\ 1+[u_{co}]-u_{co})$, but what we need is a key ZSV, so the final ZSV limitation can also be described as (23).

3.3 Novel method for CM reduction

According to the previous analysis, if the magnitude of CMV is desired to be suppressed to $u_{dc}/12$, the value of the ZSV will be limited to one value, resulting in the loss of ability to balance the NP voltage. So in this paper, a threshold NP voltage Δu_{NP_th} is set to switch the control strategy. The NP voltage u_{NP} is defined as below:

$$u_{NP} = \frac{u_{dc2} - u_{dc1}}{2}$$

Under the normal condition, the NP voltage can be automatically balanced in five-level ANPC converter. So if the NP voltage is less than the threshold voltage, case 3 strategy is chosen to minimise the CMV to $\pm u_{dc}/12$. When it is found that the absolute value of NP voltage exceeds the threshold voltage, case 2 strategy is utilised to suppress the CMV to $\pm u_{dc}/6$, and in this case the NP voltage can be a balance to the normal value. When case 2 strategy is used, the NP voltage will quickly come back to the normal and the NP voltage value will be less than threshold voltage again. So when it comes back to the normal situation, case 3 strategy will be used again to minimise the CMV. Fig. 5 shows the flowchart of how the novel method for CMV reduction operates.

4 Simulation verification

The proposed CMV strategy is verified in MATLAB/Simulink environment and the simulation parameters are summarised in Table 3. To simplify the simulation system, three-phase RL load is used in this simulation.

First of all, when there is no ZSV injected into the modulation wave, the simulation results are shown in Fig. 6.

doi: 10.1049/joe.2018.0020

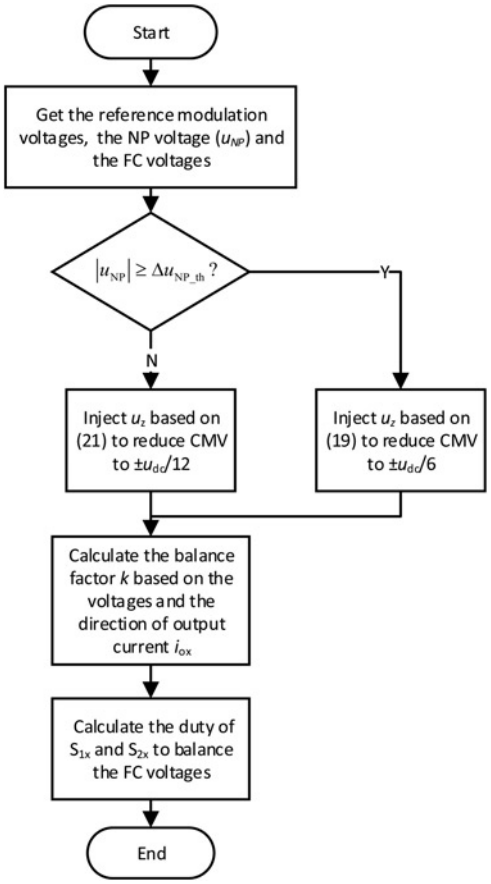

Fig. 5 *Flowchart of the novel CMV reduction strategy*

Table 3 Simulation parameters

Parameters	Values
DC input voltage	$u_{dc} = 540$ V
DC-link capacitor	$C_1 = C_2 = 4700$ μF
flying capacitance	$C_f = 1100$ μF
carrier frequency	$f_c = 2$ kHz
fundamental frequency	$f = 50$ Hz
modulation radio	$m = 0.8$
threshold voltage difference	$\Delta u_{NP\_th} = 2$ V
load	$R = 20$ Ω and $L = 10$ mH

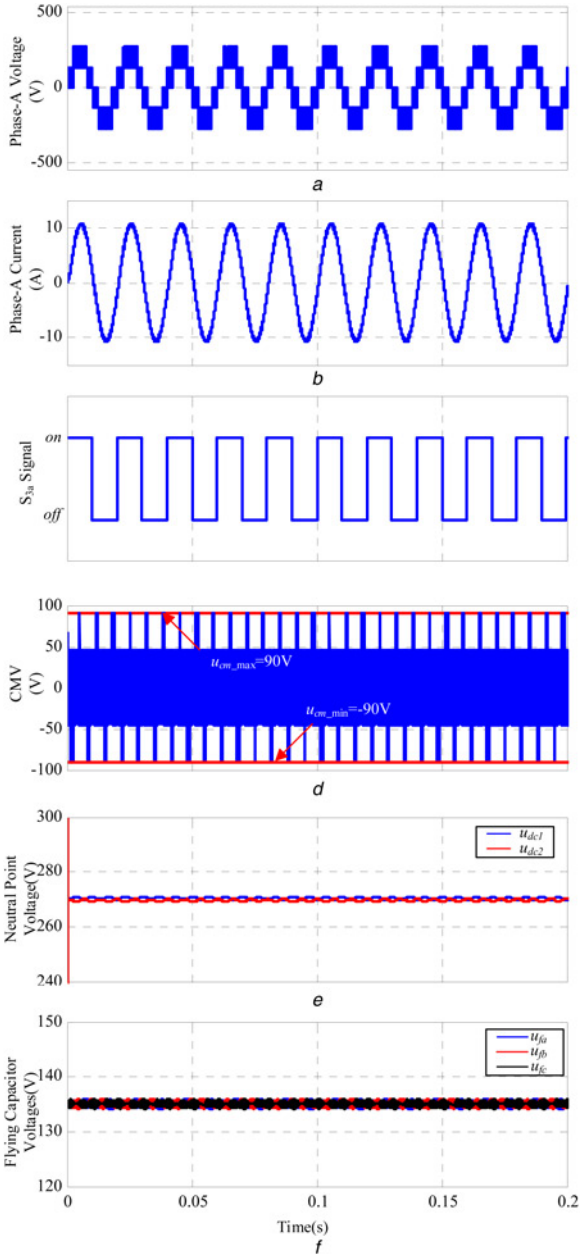

Fig. 6 *Simulation results of PS-PWM strategy without ZVS injection*
a Phase-A voltage
b Phase-A current
c S_{3x} signal
d CMV
e NP voltage
f FC voltages

Fig. 6*a* shows the phase-A voltage with the magnitude of $u_{dc}/2$. The phase-A current is illustrated in Fig. 6*b* whose total harmonic distortion is about 2.25%, which proves that five-level ANPC converter has the lower harmonic characteristic. Fig. 6*c* shows the S_{3a} signal and it is obvious that S_{3a} operates at the fundamental frequency. The CMV simulation wave is shown in Fig. 6*d* and the magnitude of CMV is about ±90 V when the ZSV is zero. Figs. 6*e* and *f* show that the NP voltage and FC voltages can be balanced automatically when the condition is ideal.

The five-level ANPC converter has the ability to balance the NP voltage and the FC voltages automatically, and the rated voltage of the upper and lower capacitors' voltage is 270 V according to the simulation parameters, whereas the FC voltage is 135 V. To verify the basic PS-PWM strategies which include the NP voltage balance method and FC voltages balance method, a voltage command is given at $t = 0.2$ s and 0.8 s to create unbalanced condition. At $t = 0.2$ s, the upper- and lower-voltage commands of the DC bus is given as 275 and 265 V separately, while the phase-A FC voltage is set to 145 V and phase-B FC voltage is set to 125 V. At $t = 0.8$ s, the voltage command comes back to normal. When the ZSV is limited by (11) and the injected voltage is key ZSV, the simulation results are shown in Fig. 7. Fig. 7*a* shows that the value of CMV, which is limited to seven levels: $u_{dc}/3$, $u_{dc}/6$, $u_{dc}/12$, 0, $-u_{dc}/12$, $-u_{dc}/6$ and $-u_{dc}/3$. The minimum value is larger than the condition that there is no ZSV injected. From Fig. 7*b*, we can find that the NP voltage can be controlled without error and it is worth noting that the steady time after the voltage command is about 9.66 ms in the simulation. Fig. 7*c* shows that the FC voltages are controlled quickly after the voltage command is given.

Fig. 8 shows the simulation results of case 2. The voltage command is given as before. Fig. 8*a* shows the CMV is reduced

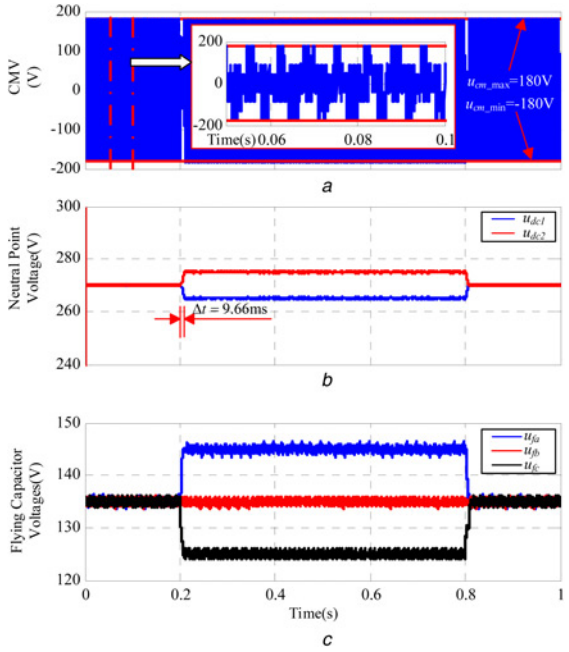

Fig. 7 *Simulation results of traditional PS-PWM strategy*
a CMV
b NP voltage
c FC voltages

by the proposed method and there are five values in the CMV. The magnitude of the CMV is about 90 V, which is $u_{dc}/6$. The mean value of CMV is reduced significantly. Fig. 8*b* shows that the NP voltage can be controlled to the given voltage by injecting the ZSV. Moreover, the steady time is about 27.72 ms, which is longer than Fig. 7*b*. So, the reduction of CMV sacrifices the ability of NP voltage balance. Fig. 8*c* shows the wave of three-phase FC voltages. They can be quickly controlled to the given values and the response time is not influenced.

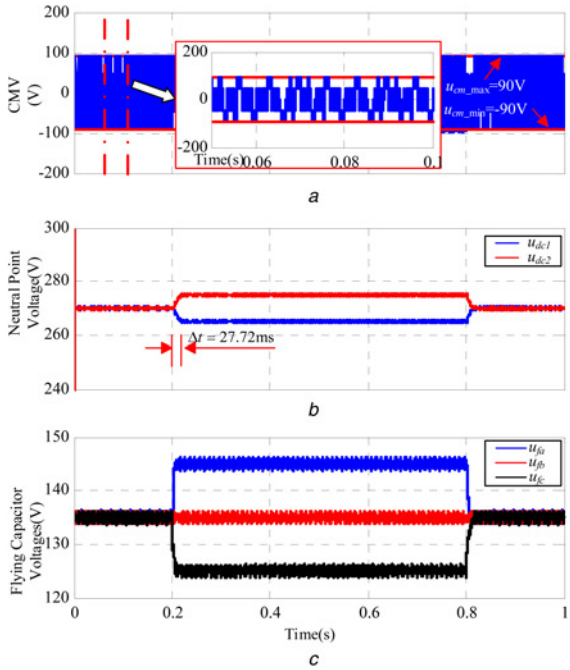

Fig. 8 *Simulation results of case 2*
a CMV
b NP voltage
c FC voltages

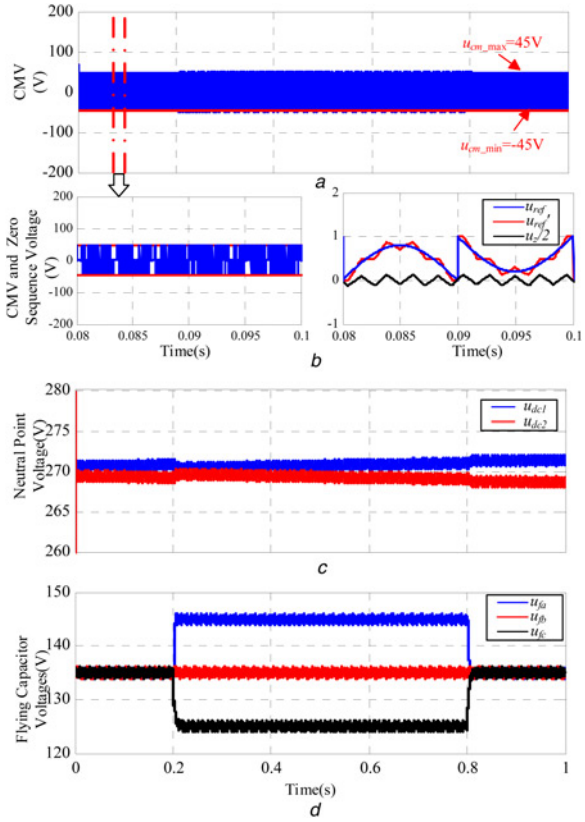

Fig. 9 *Simulation results of case 3*
a CMV
b ZSV (pu)
c NP voltage
d FC voltages

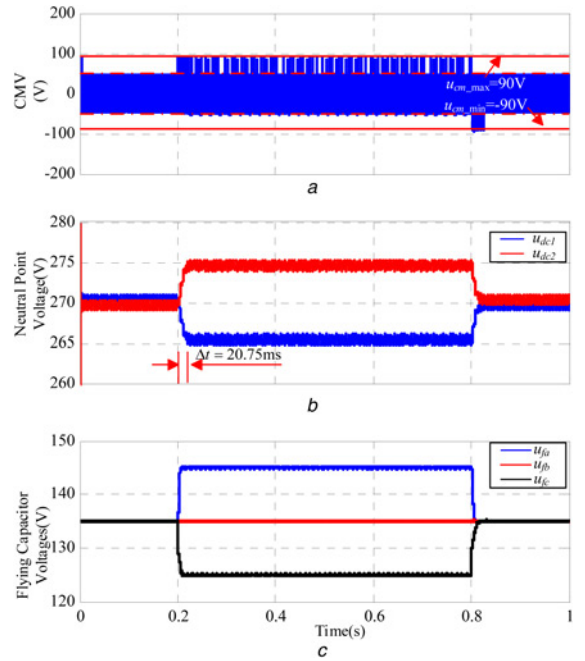

Fig. 10 *Simulation results of the novel CMV reduction strategy*
a CMV
b NP voltage
c FC voltages

Fig. 9 shows the simulation results of case 3. As we can see from Fig. 9*a*, the CMV is reduced furthermore and the maximum value of CMV is about 1/12 of the DC bus voltage. Fig. 9*b* shows the modulation wave and the injected ZSV. The frequency of ZSV is three times the fundamental frequency. Fig. 9*c* illustrates the NP voltages and it is obvious that the voltages do not follow the given value. The simulation result shows that when the injected ZSV is fixed, the ability to balance the NP voltage will lose. Fig. 9*d* shows the FC voltages and they are not influenced as well. At $t = 0.2$ s, the change of FC voltages causes the NP voltage slight fluctuation and it can be analysed in Table 2.

Fig. 10 shows the novel CMV strategy based on the PS-PWM. Fig. 10*a* shows the wave of CMV. Before $t = 0.2$ s, the NP voltage is less than the threshold voltage so the CMV is controlled to $u_{dc}/12$. After the voltage command is given, the NP voltage is larger than the threshold voltage and the NP voltage should be controlled by injecting ZSV. So, the maximum value of CMV increases to $u_{dc}/6$. Fig. 10*b* shows the results of NP voltages. There is an error whose value is the threshold voltage, but it does not affect the normal operation. The FC voltages are shown in Fig. 10*c* and they can follow the voltage command.

Therefore, the ability of NP voltage balance and the reduction of CMV are contradicted, but in this paper, a comprised method has been proposed and it can reduce the CMV significantly and achieve the balance of the NP voltage and FC voltages.

5 Conclusions

This paper focuses on the suppression of five-level ANPC converter's CMV. A novel CMV reduction strategy based on PS-PWM is proposed, which is different from the previous methods proposed by other papers. When the load is symmetrical, it can reduce the CMV's magnitude to $u_{dc}/12$ by restricting ZSV, and the maximum value of CMV is $u_{dc}/6$ by the novel strategy. The NP voltage and FC voltages can be controlled as well. Theoretic analysis and control strategy are all verified by simulation.

6 References

[1] Pou J., Zaragoza J., Ceballos S., *ET AL.*: 'A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter', *IEEE Trans. Power Electron.*, 2012, **27**, (2), pp. 642–651

[2] Wang C., Li Y.: 'Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters', *IEEE Trans. Ind. Electron.*, 2010, **57**, (7), pp. 2262–2271

[3] Fazel S.S., Bernet S., Krug D., *ET AL.*: 'Design and comparison of 4 kV neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters', *IEEE Trans. Ind. Appl.*, 2007, **43**, (4), pp. 1032–1040

[4] Rodríguez J., Steffen B., Bin W., *ET AL.*: 'Multilevel voltage-source-converter topologies for industrial medium-voltage drives', *IEEE Trans. Ind. Electron.*, 2007, **54**, (6), pp. 2930–2945

[5] Guan M., Xu Z.: 'Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions', *IEEE Trans. Power Electron.*, 2012, **27**, (12), pp. 4858–4867

[6] Wang K., Li Y., Zheng Z., *ET AL.*: 'Voltage balancing and fluctuation-suppression methods of floating capacitors in a new modular multilevel converter', *IEEE Trans. Ind. Electron.*, 2013, **60**, (5), pp. 1943–1954

[7] Chaturvedi P.K., Jain S., Agrawal P.: 'Harmonics and common mode voltage reduction in multilevel SPWM technique'. 2008 Annual India Conf. 2008 INDICON, 2008, vol. **2**, pp. 447–452

[8] Liu Z., Wang Y., Tan G., *ET AL.*: 'A novel SVPWM algorithm for five-level active neutral-point-clamped converter', *IEEE Trans. Power Electron.*, 2016, **31**, (5), pp. 3859–3866

[9] Tan G., Deng Q., Liu Z.: 'An optimized SVPWM strategy for five-level active NPC (5L-ANPC) converter', *IEEE Trans. Power Electron.*, 2014, **29**, (1), pp. 386–395

[10] Wang K., Xu L., Zheng Z., *ET AL.*: 'Capacitor voltage balancing of a five-level ANPC converter using phase-shifted PWM', *IEEE Trans. Power Electron.*, 2015, **30**, (3), pp. 1147–1156

[11] Wang K., Zheng Z., Li Y., *ET AL.*: 'Multi-objective optimization PWM control for a back-to-back five-level ANPC converter'. 2012 IEEE Energy Conversion Congress Exposition ECCE 2012, 2012, pp. 3514–3519

[12] Le Q.A., Lee D.C.: 'Modified SVPWM to eliminate common-mode voltages for five-level ANPC inverters'. ECCE 2016 – IEEE Energy Conversion Congress Exposition Proc., 2017, pp. 1–6

[13] Le Q.A., Lee D.C.: 'Reduction of common-mode voltages for five-level active NPC inverters by the space vector modulation technique', *IEEE Trans. Ind. Appl.*, 2017, **53**, (2), pp. 1289–1299