The Journal of Engineering

The 14th International Conference on Developments in Power System Protection (DPSP 2018)

IET Journals
The Institution of Engineering and Technology

Distributed signal processing units for centralised substation protection and control

eISSN 2051-3305
Received on 3rd May 2018
Accepted on 23rd May 2018
E-First on 22nd August 2018
doi: 10.1049/joe.2018.0206
www.ietdl.org

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Abstract: Substation automation systems are characterised by a high degree of functional integration, which can lead to a centralised substation protection and control (CPC) architecture. Most CPC architectures utilise merging units to interface with current and voltage transformers, which causes a high-communication load on the process bus in case of large substations. This study proposes a CPC architecture based on distributed signal processing units (DSPUs) to overcome those drawbacks by publishing the results of the signal processing algorithms directly. The reduction of the communication load through the usage of DSPUs has been shown in a case study, which uses a 16-bay transmission substation topology as a reference.

1 Introduction

Today's substation automation systems (SASs) are impacted strongly by the trend of digitalisation. Two important effects of this digitalisation are the possibility of a high degree of functional integration on a single platform and the replacement of conventional copper cables with Industrial Ethernet-based communication. In the end, this development can result in a centralised substation protection and control (CPC) system. There are different CPC architectures proposed in the literature and implemented by manufacturers. This study emphasises the importance of the functional allocation of digital signal processing within the CPC architecture and of the deterministic behaviour of the centralised platform.

DSP is an essential part of protection and control functions in substations and the significance of DSP grows due to the changing characteristics of power systems. The increased integration of power electronics, such as flexible alternating current transmission System (FACTS) devices or high-voltage direct current (HVDC) converters, leads to higher-harmonic content and new phenomena such as sub-synchronous resonance. These changing characteristics of the power system are detected by the DSP algorithms of protection and control functions. In addition, high-speed protection functions rely on time-domain and travelling-wave-based principles. One of the shortcomings of merging units (MUs) is the lack of high-speed signal processing capabilities, which can be used for these related protection applications. For instance, fault location and travelling-wave protection applications require high-sampling rates of the current and voltage signals. As a result, it is impossible to perform accurate fault location and other high-speed protection application based on those existing MUs. Therefore, this study proposes a CPC architecture, which allocates the signal processing functions on dedicated devices called distributed signal processing units (DSPUs). In this way, the heavy computational burden of DSP is removed from the centralised platform. Hence, the centralised platform becomes scalable and can dedicate its computational resources to the deterministic execution of the protection logic and control functions. In addition, the communication load is reduced due to the working principle of the DSPU. This study introduces two datasets for DSPUs used in transformer bays and transmission line bays, respectively. These datasets represent the results of the signal processing algorithm, which are published on the process bus and aggregated at the centralised platform running the protection logic. In addition, the communication load has been calculated as part of a case study, which uses a 16-bay transmission substation as the calculation base. The results have been compared with CPC architectures based on MUs and DSPUs.

The remainder of the paper is structured in the following way: Section 2 comprises the related work that has been carried out in the field of CPC architectures as well as signal processing in power systems. Section 3 elaborates on the proposed CPC architecture of this paper and defines the scope of operation of DSPUs. Section 4 shows a calculation example of the communication load for different CPC architectures. Finally, the paper ends with a discussion of the results and a conclusion proposing the future work.

2 Related work of CPC architectures

One of the first CPC architectures has been proposed in [1] in 1969. This CPC architecture has been designed to protect a representative transmission substation consisting of 500, 230 and 66 kV voltage levels by sampling 105 current and 24 voltage signals with a 2 kHz sampling rate. From then on, many different CPC architectures have evolved over time. In [2], a CPC architecture is described, which runs the entire protection, control, monitoring and measurement functionality of a 110/10 kV substation on four servers. The substation itself consists of two power transformers, two incoming 110 kV power lines and 40 feeders connected to four 10 kV busbars. In 2015, the Power System Relaying Committee of the IEEE PES Society has published a report [3] on CPC. This report defines a CPC system as 'a system comprised of a high-performance computing platform capable of providing protection, control, monitoring, communication and asset management functions by collecting the data those functions require using high-speed, time synchronized measurements within a substation.' The findings of this report are summarised in [4], which evaluates the different CPC architectures in terms of performance criteria such as availability as well as in terms of cost. One of the differentiating aspects between those SASs is the allocation of functionality between the process, bay and station level. The conventional approach is to keep both main and backup protection functions together with the signal processing algorithms at the bay level. Later approaches move the A/D conversion of the currents and voltages to the process level as part of the MU. This architecture keeps the protection logic at the bay level together with the remaining parts of signal processing, such as discrete Fourier transform (DFT) or wave shape analysis. If the MU also comprises an I/O breaker interface, then these devices are called process interface units (PIUs). Newer approaches suggest that the protection functionality is moved to a centralised station

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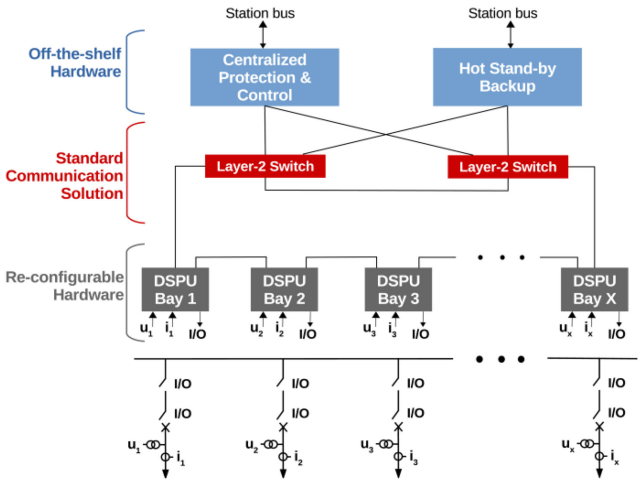

Fig. 1 *Proposed CPC architecture based on DSPUs*

level while keeping the A/D conversion in the MU/PIU at the process level. In [5], an intelligent MU (IMU) is mentioned, which adds a root-mean square (RMS)-based overcurrent protection to the MU. This has the advantage of providing backup protection in case of a communication failure of the process bus. A technically similar concept to the IMU approach has been proposed in [6], which introduces sampled value (SAV) publishing capabilities to bay-level protection relays. The process bus communicates the current and voltage samples with the application layer protocol SAV (IEC 61850-9-2) and binary values as generic object oriented substation event (GOOSE) (IEC 61850-8-1) messages between the MUs and protection relays. In [7], the process bus performance is analysed in case of a centralised function such as synchrocheck and states that the tight sampled value (SV) requirements might be violated in case of a failure of the high-availability-seamless-redundancy ring. Therefore reliability, speed and real-time performance of the communication solution are of high importance. In [8], it is proposed to implement the entire protection functionality on field-programmable gate array (FPGA) hardware. Using dedicated hardware for specific functionality, such as signal processing, is a common approach. Nowadays, digital signal processors are mostly used in protection intelligent electronic device (IEDs) [9].

Since this study proposes a CPC architecture based on DSPUs in Section 3, it is crucial to understand the importance of the signal processing part of protection algorithms in future power grids. In [10], various power system phenomena are described, which have to be considered for the design of the signal processing algorithms of protection and control functions. Those phenomena are lightning and switching surges, inrush current and over-excitation of power transformers, transients in instrument transformers or increased harmonic components. Recently, interharmonics has received more attention, as stated in [11]. Sub-synchronous resonances are an example of such interharmonics. There are already well-established signal processing algorithms for some of the aforementioned power system phenomena. Nonetheless, it can be expected that in the future new sophisticated signal algorithms will be applied for power system protection and control functions, which might require higher-sampling rates than the currently suggested 4 and 4.8 kHz of the protection profile in IEC 61850-9-2LE [12] in case of 50 and 60 Hz systems, respectively. In the latest IEC 61869-9 standard [13], a sampling rate of 4.8 kHz is defined by a digital output publishing rate of 2400 frames per second regardless of the power system frequency. Travelling-wave based protection algorithms require in some cases sampling rates up to 1 MHz, as stated in [14]. An increased sampling rate imposes greater challenges for a deterministic and reliable Ethernet-based process bus communication.

3 Novel substation automation system

Due to the challenges of reliable and deterministic process bus communication in case of high-sampling rates, a novel CPC architecture is proposed in the following section.

3.1 Proposed CPC architecture

The proposed CPC architecture, as shown in Fig. 1, seeks to reduce the computational load of the centralised platform as well as to reduce the communication load of the process and thereby enabling a hard real-time substation protection and control system. To achieve these two objectives, all computationally expensive signal processing algorithms, needed for protection and control purposes, are distributed among dedicated hardware, such as FPGAs while keeping the protection logic centralised on general purpose hardware. These dedicated devices are called DSPUs. DSPUs are synchronised and execute the signal processing algorithms needed by the protection and control logic running on the centralised platform.

The concept of DSPUs is different from the MU in the sense that the outputs of the different signal processing algorithms are published directly, instead of sending the SAV stream. Thus, the information exchange between the DSPUs and the centralised platform can occur at a lower rate than the defined publishing rates in IEC 61850-9-2LE. Furthermore, high-sampling rates of current and voltage inputs can be implemented in the DSPUs and thereby enable the integration of novel signal processing algorithms and protection applications. Examples of such applications are time-domain based and traveling-wave based protection functions. Therefore, the DSPUs are equipped with I/O cards in order to interface with circuit breakers and disconnectors. This setup also enables the integration of backup protection in case of a complete communication failure as suggested by the IMU concept in [5].

3.2 Distributed signal processing unit

The DSPUs are placed at each bay and interface the respective instrument transformers as well as the breakers. Thus, all time-critical hard real-time algorithms, requiring instantaneous values as input, are implemented in the DSPU. It is of importance that the scope of the implemented signal processing algorithms is adaptable depending on the protection application. For instance, line protection applications usually require the phasor information of the fundamental component whereas transformer protection applications require additional information about the harmonic components, such as second, third, and fifth harmonics or even true-RMS values. Thus, the DSPU needs to be configurable to provide different signal processing output-sets according to the protection application. These signal processing output-sets can be defined following the IEC 61850 data modelling concept and specified in form of datasets and common data classes (CDCs). Those datasets can then be mapped to suitable application layer protocols and sent over an Ethernet-based process bus. Two examples of such datasets are defined for a transformer protection application and for a transmission line protection application, respectively. Additionally, the dataset *PhsMeasx*, used for publishing SAVs, is described as well and used as a reference case in Section 4. In the future, more of those datasets need to be defined for other protection objects, such as distribution line, generator or capacitor banks. Furthermore, the DSPU concept allows the integration of disturbance recording functionalities, which can either be triggered by the local DSPU directly or by the centralised platform through GOOSE.

3.2.1 Transformer protection dataset: Transformer protection functions require multiple signal processing inputs in order to reliably detect transformer faults and to distinguish them from normal operational phenomena such as transformer inrush currents. Based on these requirements, a basic dataset for transformer protection is defined in Table 1. This table shows that the dataset does not only contain the fundamental phasors but also the second harmonic for inrush current detection and the third and fifth harmonic for over-excitation detection. These measurements are represented according to the IEC 61850-7-3 CDC called complex

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measured value (CMV). The CMV has been specified in Table 2 and consists of two attributes *cVal.mag.i* and *cVal.ang.i* corresponding to the magnitude and angle of the phasor, respectively. Additionally, a quality attribute is part of the CMV. The quality is a constructed attribute consisting of the Boolean identifiers *validity, detail quality, source, test* and *frozen by operator*.

The utilities communication architecture (UCA) implementation guideline IEC 61850-9-2LE [12] has extended the attribute type quality by the identifier derived to indicate if the value is measured or calculated. The quality attribute is defined to be a 32-bit value and thus many bits are still unused. Therefore, the constructed quality attribute can be further extended to provide additional information to the centralised platform, such as current transformer (CT) saturation detection, open CT detection or wave shape analysis, as shown in Table 3. These algorithms are based on instantaneous values and are, therefore, also implemented in the DSPU. Currently, most of those methods use measurements from multiple sources. Thus, the challenge is to implement reliable standalone algorithms that only rely on the local bay measurements. Table 1 shows that the proposed dataset for transformer protection would correspond to a data volume of 1440 bits.

3.2.2 Transmission line protection dataset: In the case of transmission line protection, the fundamental components of the line currents and phase voltages are of importance. A dataset has been proposed in Table 4, which includes the current and voltage phasors.

These values share the same CDC CMV, as in Table 2, which means that CT saturation detection, open CT detection and wave shape analysis information are included as well. If a transient-based protection application is required to protect the corresponding transmission line, then the travelling wave signals, both with polarity and time step, are also added. Table 4 indicates that the data volume of the dataset is 768 bits. DSPUs offer the possibility to implement custom filters to detect certain power system phenomena, such as sub-synchronous resonances. Nonetheless, they are not considered in the above dataset definition.

3.2.3 PhsMeasx dataset: The dataset PhsMeasx is defined in Table 5 in order to establish a reference case that will be compared with the CPC architecture with DSPUs. This dataset is defined in IEC 61850-9-2LE and comprises the individual current and voltage samples. Considering the CDC SAV, specified in Table 6, the dataset PhsMeasx requires 512 bits. This dataset PhsMeasx is mapped to the application layer protocol SV through the usage of

Table 1 Example of the dataset for transformer protection

Output of the DSP algorithm	Data object IEC 61850-7-4	Common data class IEC 61850-7-3	Data size
current phasor A (fund.)	A.phsA	CMV	96 bits
current phasor B (fund.)	A.phsB	CMV	96 bits
current phasor C (fund.)	A.phsC	CMV	96 bits
current phasor N (fund.)	A.neut	CMV	96 bits
second, third and fifth harmonic of current phase A	HA.phsAHar	array of CMV	224 bits
second, third and fifth harmonic of current phase B	HA.phsBHar	array of CMV	224 bits
second, third and fifth harmonic of current phase C	HA.phsCHar	array of CMV	224 bits
voltage phasor A (fund.)	PhV.phsA	CMV	96 bits
voltage phasor B (fund.)	PhV.phsB	CMV	96 bits
voltage phasor C (fund.)	PhV.phsC	CMV	96 bits
voltage phasor N (fund.)	PhV.neut	CMV	96 bits
			total: 1440 bits

Table 2 CDC of CMV

Attribute name	Type	Description
cVal.mag.i	int32	magnitude of complex value
cVal.ang.i	int32	angle of complex value
q	quality	validity information (32 bits)

Table 3 Constructed quality attribute

Attribute name	Attribute type	Defined in
validity	coded enum	IEC 61850-7-3
overflow	Boolean	IEC 61850-7-3
outOfRange	Boolean	IEC 61850-7-3
badReference	Boolean	IEC 61850-7-3
oscillatory	Boolean	IEC 61850-7-3
failure	Boolean	IEC 61850-7-3
oldData	Boolean	IEC 61850-7-3
inconsistent	Boolean	IEC 61850-7-3
inaccurate	Boolean	IEC 61850-7-3
source	coded enum	IEC 61850-7-3
test	Boolean	IEC 61850-7-3
operatorBlocked	Boolean	IEC 61850-7-3
derived	Boolean	IEC 61850-9-2LE
saturatedCT	Boolean	proposal
openCT	Boolean	proposal
waveShape	Boolean	proposal

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Table 4 Example of the dataset for transmission line protection

Output of the DSP algorithm	Data object IEC 61850-7-4	Common data class IEC 61850-7-3	Data size
current phasor A (fund.)	A.phsA	CMV	96 bits
current phasor B (fund.)	A.phsB	CMV	96 bits
current phasor C (fund.)	A.phsC	CMV	96 bits
current phasor N (fund.)	A.neut	CMV	96 bits
voltage phasor A (fund.)	PhV.phsA	CMV	96 bits
voltage phasor B (fund.)	PhV.phsB	CMV	96 bits
voltage phasor C (fund.)	PhV.phsC	CMV	96 bits
voltage phasor N (fund.)	PhV.neut	CMV	96 bits
		total:	768 bits

Table 5 Dataset PhsMeasX for SAV

Output of the DSP algorithm	Data object IEC 61850-7-4	Common data class IEC 61850-7-3	Data size
SV of current phase A	AmpSv	SAV	64 bits
SV of current phase B	AmpSv	SAV	64 bits
SV of current phase C	AmpSv	SAV	64 bits
SV of neutral current	AmpSv	SAV	64 bits
SV of voltage phase A	VolSv	SAV	64 bits
SV of voltage phase B	VolSv	SAV	64 bits
SV of voltage phase C	VolSv	SAV	64 bits
SV of neutral voltage	VolSv	SAV	64 bits
			total: 512 bits

application service data units (ASDUs), which is then encapsulated in an Ethernet frame and published through the process bus. This described protocol stack is implemented in the MU.

Different digital sampling rates (Hz) and publishing rates (frame/s) have been defined in IEC 61850-9-2LE [12] and in IEC 61869-9 [13] for alternating current protection applications. The following three variants are used as a reference case in Section 4:

- 4 kHz, 1 ASDU, 4000 frames/s (F4000S1I4U4)
- 4.8 kHz, 1 ASDU, 4800 frames/s (F4800S1I4U4)
- 4.8 kHz, 2 ASDUs, 2400 frames/s (F4800S2I4U4)

The variant notation F *f* S *s* I *i* U *u* has been used, as in [5], with

- *f*: digital sampling rate
- *s*: number of ASDUs in a SAV messages
- *i*: number of current quantities in each ASDU
- *u*: number of voltage quantities in each ASDU

3.3 Synchronous substation process image

The synchronously sampled measurements and I/O information of the DSPUs are published through the process bus and are aggregated at the centralised platform in the form of a synchronous substation process image (SSPI), as shown in Fig. 2. The SSPI contains all the measurements and status information, defined in Tables 1 and 4 together with I/O information, such as breaker and disconnector positions. The centralised platform is located at the station level in an electro magnetic interference (EMI)-shielded room and consists of off-the-shelf hardware. The comprehensive protection and control logic of the entire substations, which rely on

Table 6 CDC of SAV

Attribute name	Type	Description
instMag.i	int32	magnitude of complex value
Q	quality	validity information (32 bits)

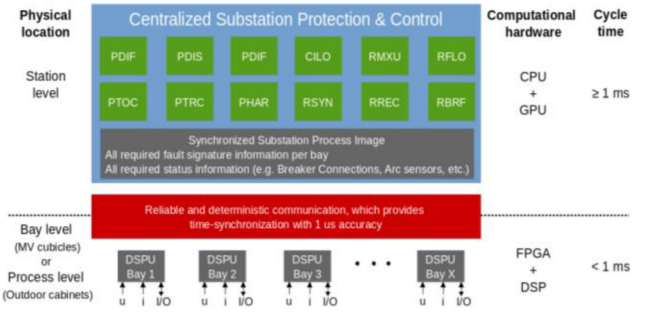

Fig. 2 *Overview of architecture*

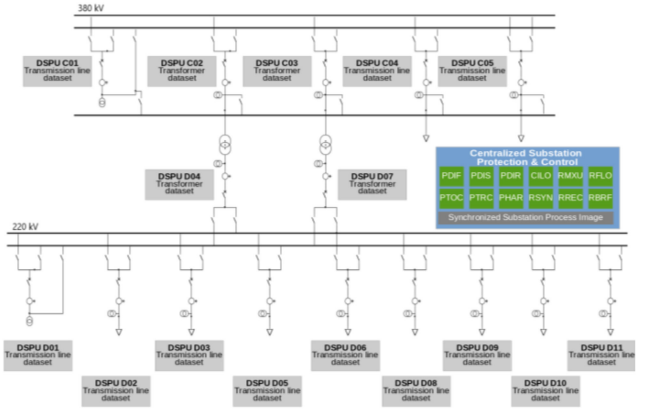

Fig. 3 *DSPU architecture applied to transmission substation topology stated in IEC 61850-5 [15]*

measurements from the frequency domain and status information, are implemented on the centralised platform and run at 1 ms cycle time or slower. On the other hand, applications relying on instantaneous current and voltage values are distributed on the FPGA-based DSPUs and run at cycle times faster than 1 ms. The DSPUs are placed either directly in the respective medium voltage cubicles at the bay level or in outdoor cabinets at the process level. Time synchronisation of the DSPUs is critical and is achieved through the communication media based on the precision time protocol, which provides sub-microsecond accuracy.

4 Case study

In the previous section, the DSPU concept for CPC architectures has been established. This section shows quantitatively the reduction of the communication load in the form of a case study. The case study uses a reference substation topology, which serves as a calculation base of the communication load in case of a purely MU-based process bus versus a DSPU-based process bus.

4.1 Substation topology

The chosen reference substation topology is taken from [15] and represents a large size transmission substation. The 16-bay substation, as shown in Fig. 3, consists of four transformer bays, 10 transmission line bays, and two bus coupler bays.

Each bay is equipped with a current transformer, a voltage transformer, disconnectors and a circuit breaker. For the calculation of the communication load in Section 4.2, only the measurements of the currents and voltages of each respective bay are considered, and the related I/O information of the disconnectors and breakers are neglected. Two different architectures are compared. The first setup considers that each bay has an MU associated with it, which publishes the SV according to the dataset defined in Table 5. The

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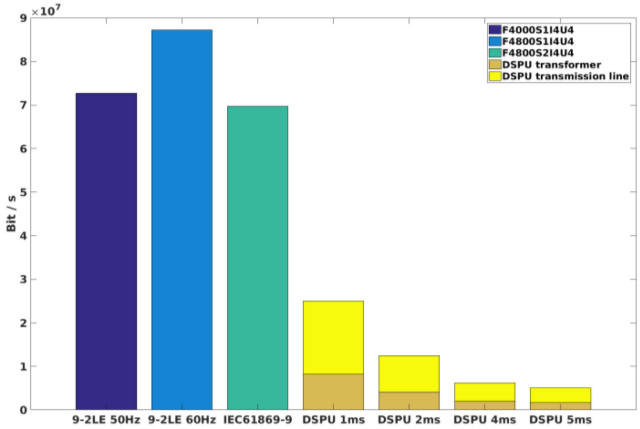

Fig. 4 *Communication load for CPC architectures based on MUs and DSPUs*

second setup considers that each transformer bay is associated with a DSPU implementing the dataset for transformer protection defined in Table 1 and that each transmission line and busbar coupler bay is associated with the transmission line data set defined in Table 4.

4.2 Evaluation of communication load

It is assumed that the datasets, defined in Section 3.2, are mapped to the SV protocol and encapsulated in an Ethernet II frame, with the following parameters:

- Preamble + start frame delimiter (SFD): 8 bytes
- Dest. + Src. MAC address: 12 bytes
- 802.1Q tag: 4 bytes
- Ether type: 2 bytes
- Frame check sequence: 4 bytes
- Interpacket gap: 12 bytes
- *Ethernet overhead in total: 42 bytes*

Hence, the communication overhead due to the header information remains constant regardless of the chosen dataset. This simplification needs to be adjusted if the datasets are mapped to a different application layer protocol. Equations (1) and (2) are used to calculate the communication load for the MU-based and DSPU-based process bus, respectively.

$$\mathrm{LOAD}_{\mathrm{MU}} = \frac{f}{s} \cdot N_{\mathrm{bay}}(E_{\mathrm{th}} + S_{\mathrm{av}} + s(A_{\mathrm{sduH}} + P_{\mathrm{hsMeasx}})), \quad (1)$$

$$\mathrm{LOAD}_{\mathrm{DSPU}} = \frac{1}{s \cdot P} \cdot N_{\mathrm{tr}}(E_{\mathrm{th}} + S_{\mathrm{av}} + s(A_{\mathrm{sduH}} + T_{\mathrm{Data}})) + \frac{1}{s \cdot P} \cdot N_{\mathrm{ln}}(E_{\mathrm{th}} + \mathrm{S}_{\mathrm{av}} + s \cdot (A_{\mathrm{sduH}} + L_{\mathrm{Data}})), \quad (2)$$

where f is the digital sampling rate, s is the number of ASDUs in a message, P is the cycle time of DSPU algorithms, N_{bay} is the number of bays (here 16), N_{tr} is the number of transformer bays (here 4), N_{ln} is the number of line bays (here 12), E_{th} is the Ethernet overhead (42×8 bits), S_{av} is the SV protocol overhead (15×8 bits), A_{sduH} is the ASDU overhead (21×8 bits), P_{hsMeasx}, is the dataset PheasMeasx (512 bits), T_{data} is the dataset of transformer bays (1440 bits), and L_{data} is the dataset of transmission line bay (768 bits)

It can be seen from (1) that an increased sampling rate yields directly a higher-communication load. Furthermore, batching of the samples by increasing the number of ASDUs only has a limited reduction effect, since it saves only on the Ethernet and SV protocol overheads. It becomes clear from (2) that the DSPU-based process bus is not affected by an increased sampling frequency, but rather by the cycle time of the signal processing algorithms running on the DSPUs. Fig. 4 shows the communication load on the process bus for the following cases:

$\mathrm{LOAD}_{\mathrm{MU}}$: F400S1I4U4, F4800S1I4U4, F4800S2I4U4.

$\mathrm{LOAD}_{\mathrm{DSPU}}$: DSPU($P = 1$ ms, $s = 1$), DSPU($P = 2$ ms, $s = 1$), DSPU($P = 4$ ms, $s = 1$), DSPU($P = 5$ ms, $s = 1$).

It can be noticed that the communication load is reduced significantly by the usage of DSPUs over MUs. This advantage becomes evident if applications requiring high-sampling rates are integrated into the CPC architecture. The communication load in CPC architectures using DSPUs are not sensitive to an increased sampling frequency, as shown in (2). On the other hand, the communication load in CPC architectures using the MU would increase considerably, as shown in (1).

5 Conclusion

This study has proposed a new CPC architecture, which allocates the signal processing algorithms and applications, requiring high-sampling frequencies, on a dedicated device called DSPU, while keeping the protection and control logic centralised. Thus, the computational load of the centralised platform is decreased. It has been shown in a case study that the communication load on the process bus can be reduced in comparison with a CPC architecture based on the MU.

This approach brings also several challenges. The IEC 61850 does not specify logical nodes for signal processing functions used for protection purposes. In fact, it is stated that the signal processing functionality is part of the protection logical node. This is due to the fact that certain protection schemes require instantaneous values, such as differential protection schemes based on instantaneous values, as well as different vendors might implement signal processing algorithms with different transient behaviours. For example, the window type and size of DFT algorithm would need to be defined for such logical nodes, so that their outputs can be used by the protection logic from different vendors, similar to C37.118.1. Another challenge is the design of reliable standalone methods for applications, which rely only on local bay measurements, such as CT saturation detection.

Despite those challenges, the benefits of DSPUs become evident with the integration of time domain and travelling-wave-based protection functions and other filters requiring high-sampling rates. Therefore, the future work of this research will involve a hardware-in-the-loop setup of the proposed CPC architecture in order to show the validity of the design.

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