

# Behavioural modelling and power quality simulation of a HVDC electric power system for MEA

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**Abstract:** High-voltage direct current (HVDC) electric power system (EPS) is a promising architecture for more electric aircraft (MEA). With more electric power used, a higher voltage is necessary to make aircrafts more efficient and less weighted. However, there are no standards can be followed to evaluate the power quality of HVDC EPS, especially for 540 VDC system. In this study, a potential HVDC EPS is proposed and power quality is studied by simulation. Behavioural models of the system are established in detail from source to load. Three kinds of typical loads of MEA are defined and their impacts on power quality are analysed including resistances, power electronic converters, and motors. Some suggestions are provided for design and integration of the EPS for MEA.

## 1 Introduction

In order to meet the increasing demand for low cost, high efficiency and emission-free, the concept of more electric aircraft (MEA) has been paid much more attention in recent years [1]. It leads to a dramatic utilisation of electric power by partly removing the conventional mechanical, hydraulic and pneumatic devices. Compared to the AC electric power system (EPS), DC EPS has advantages such as higher reliability, higher efficiency, lower cost, lower weight, and easier maintainability [2, 3].

As a result of the increased electric power, a higher DC bus voltage level is required to reduce the current of feeders, which affects the weight of EWIS cables and power loss of the aircraft. Several papers have discussed the stability [4], control strategy [5], and power management [6] of 270 VDC EPS. Besides, some papers study the current sharing method of multiple paralleling DC sources [7]. There are some standards focused on the requirements of power quality for 270 VDC, such as MIL-STD-704F [8]. However, few of them involve the subject on 540 VDC EPS and its power quality, which is an important topic because a lot of power electronic converters and motors used on aircraft can be represented as either constant power loads or pulse-width modulation (PWM) loads and many types of research have been addressed to reveal the instability problem of the EPS caused by these kinds of loads [8].

In this paper, architecture of a high-voltage direct current (HVDC) (540 V) EPS for MEA is proposed and its electric power characteristics are studied by simulation. In Section 2, the one power channel HVDC EPS is introduced and the behavioural models are established in Section 3. Then simulations are conducted under three different conditions of load operation in order to analyse the power quality of the EPS in Section 4. Finally, conclusions are drawn in Section 5.

## 2 Proposed system

The proposed HVDC EPS is indicated in Fig. 1. As the purpose of this paper is an analysis of the power quality of the system, only one channel of the distribution system is shown.

The 540 VDC bus is supplied by a 200 kVA high-speed permanent magnet generator (PMG) whose AC output is converted into DC power by an active front-end rectifier. Both the cables from the PMG to the rectifier and from the rectifier to the bus are considered.

Loads of the 540 VDC bus include a 50 kW wing ice protection system (WIPS) and two permanent-magnet motors driven by two controllers, namely the 60 kW environmental control system (ECS) and the 20 kW fight control system (FCS), respectively. A 60 kVA DC/AC inverter (INV) inverts 540 VDC into AC voltage to feed a 115 VAC bus. A 10 kW DC/DC converter (CONV) converts 540 VDC into 28 VDC to feed a 28 VDC bus. In addition, a 10 kW transformer rectifier unit (TRU) can convert the AC power from 115 VAC bus into 28 VDC to feed another 28 VDC bus. There are batteries paralleled with the two 28 VDC buses, which are ignored in this paper, assuming that batteries have no influence on the power quality at this analysis. The 115 VAC bus supplies power for galley and other AC loads and the 28 VDC bus supplies power for instruments and other devices of low voltage used for control.

## 3 System modelling

In this section, behavioural models of the system are derived. First, the PMG model and the rectifier model are derived in a  $d$ - $q$  coordination, which rotates synchronously with the magnet flux. The PMG equations are given by (1), where  $v_d$  and  $v_q$  are the voltages of the PMG stator in  $d$  and  $q$  axes,  $i_d$  and  $i_q$  are the currents of the PMG stator in  $d$  and  $q$  axes.  $R_s$ ,  $L_d$ , and  $L_q$  are the resistance,  $d$ -axis inductance, and  $q$ -axis inductance of the PMG stator, respectively.  $\Psi_f$  is the flux generated by the rotor permanent magnet, and  $\omega_e$  is the electrical rotational speed of the rotor

$$\begin{cases} v_d = R_s i_d + L_d \frac{di_d}{dt} - \omega_e L_q i_q \\ v_q = R_s i_q + L_q \frac{di_q}{dt} + \omega_e L_d i_d + \omega_e \Psi_f \end{cases} \quad (1)$$

The rectifier equations are given by (2), of which the circuit is

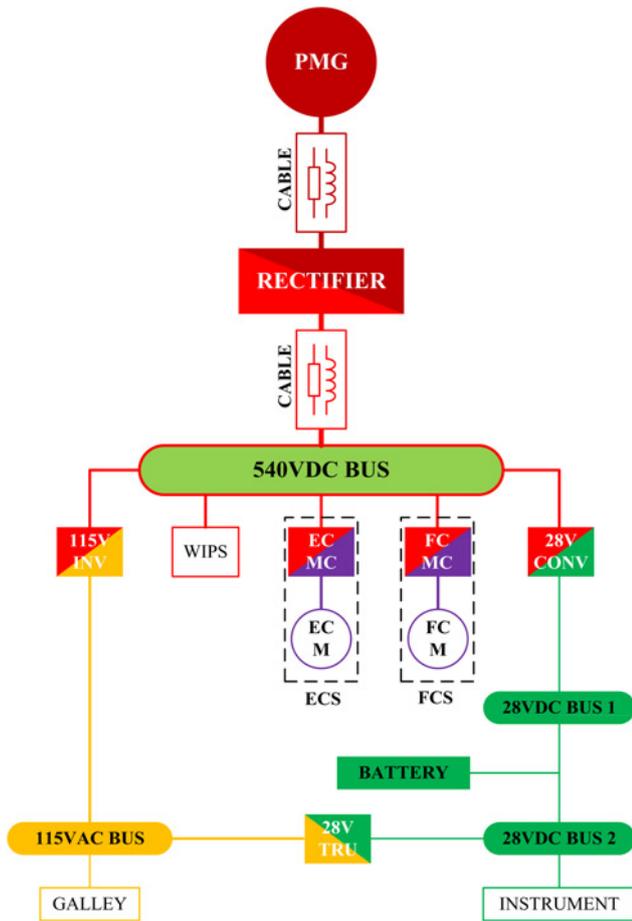


Fig. 1 Configuration of the proposed HVDC EPS

shown in Fig. 2.

$$\begin{aligned}
 v_d &= r_{\text{cable}} i_d + L_{\text{cable}} \frac{di_d}{dt} - \omega_e L_{\text{cable}} i_q + S_d v_{\text{dc}} \\
 v_q &= r_{\text{cable}} i_q + L_{\text{cable}} \frac{di_q}{dt} - \omega_e L_{\text{cable}} i_d + S_q v_{\text{dc}} \\
 C_{\text{dc}} \frac{dv_{\text{dc}}}{dt} &= \frac{3}{2} (S_d i_d + S_q i_q) - i_o
 \end{aligned} \quad (2)$$

In (2), cables are modelled as resistance and inductance in series, which written as  $r_{c\_ac}$  and  $L_{c\_ac}$ .  $C_{dc}$  and  $v_{dc}$  are the DC bus capacitor and voltage, respectively, while  $i_o$  is the output current fed to the 540 VDC bus.  $S_d$  and  $S_q$  are the switching functions transformed from the  $a$ - $b$ - $c$  coordination, where  $S=1$  if the upper switch is on while  $S=0$  if the down switch is on.

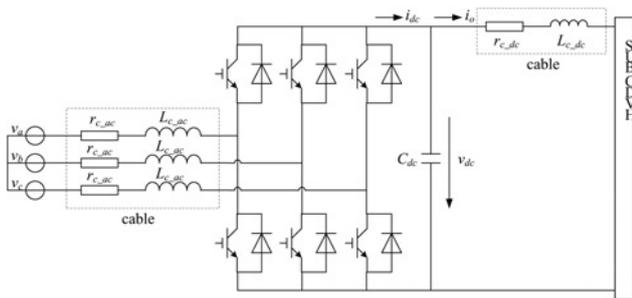


Fig. 2 Circuit of the active front-end rectifier

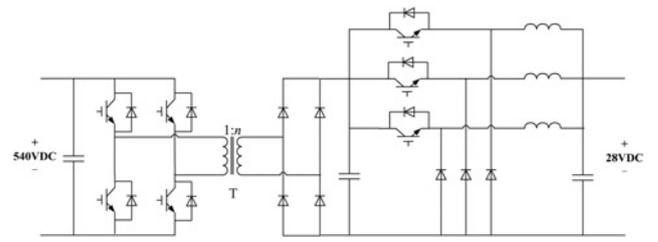


Fig. 3 Circuit of the 540 VDC/28 VDC converter

Considering cables of the DC side, voltage of the HVDC bus can be calculated as

$$v_{\text{bus}} = v_{\text{dc}} - r_{c\_dc} i_o - L_{c\_dc} \frac{di_o}{dt} \quad (3)$$

As for the models of the loads, three types are considered. WIPS, galley, and all the loads under 28-VDC buses are treated as variable resistances, which vary with load demand changing. The value of the resistance is calculated by its power demand and voltage as

$$R_{\text{load}} = \frac{V_{\text{bus}}^2}{P_{\text{load}}} \quad (4)$$

In (4),  $R_{\text{load}}$  and  $P_{\text{load}}$  refer to the resistance and the power of the load, respectively, while  $V_{\text{bus}}$  refers to the voltage of the bus where the load gets a power supply.

The 28 V CONV and 28 V TRU are small loads which convert power into DC power, which are the second type of load. The topology of CONV is a 2-level cascade converter that the first one is a voltage-fed full bridge converter stepping down the voltage to about 40 V and the second one is an interleaved buck converter, whose circuit is indicated in Fig. 3. Besides, the topology of TRU is a 12-pulse transformer rectifier, which is commonly used on EPS of aircraft, as shown in Fig. 4.

The 115 V INV is a large PWM load, but most of the devices fed by 115-VAC bus are resistances. The topology of INV is also a 2-level cascade converter, of which the circuit is given in Fig. 5. The voltage is regulated to 400 VDC by the full-bridge DC-DC converter and inverted to 115 V, 400 Hz AC power by the half-bridge DC-AC inverter.

Moreover, the two motor controllers invert DC power into AC power, while the two motors behave as constant power loads,

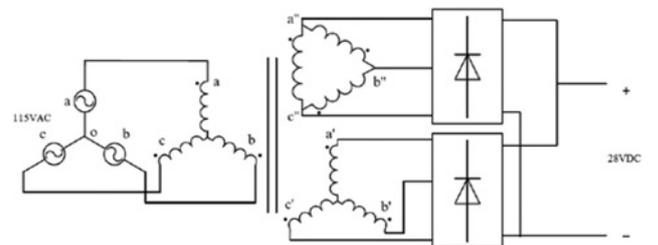


Fig. 4 Circuit of the 115 VAC/28 VDC TRU

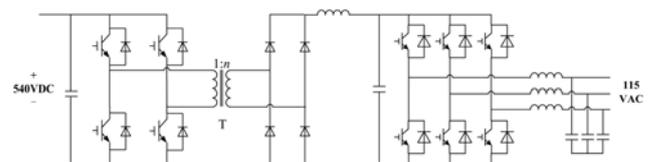
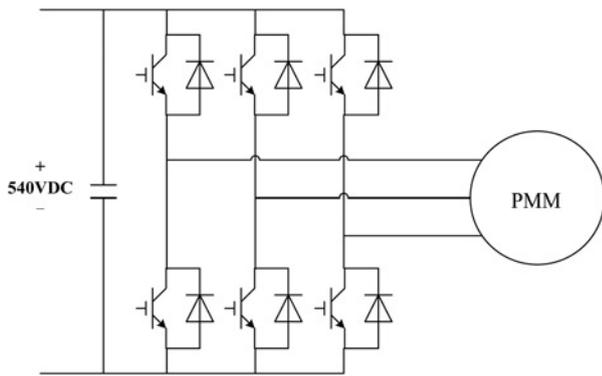


Fig. 5 Circuit of the 540 VDC/115 VAC inverter



**Fig. 6** Circuit of the inverter and motor

which are divided into the third type of load. The circuit of the inverter and motor is shown in Fig. 6.

#### 4 Case study

In this section, the impact of the three kinds of typical loads used on the proposed MEA EPS is analysed by the models derived in the above section, namely resistances, PWM converters, and inverters and motors.

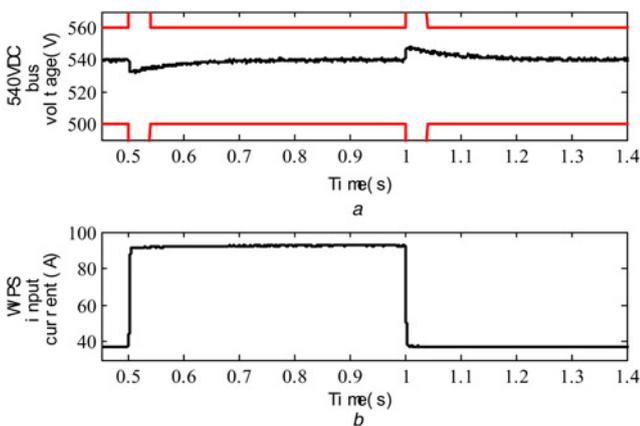
##### 4.1 Resistive loads

In Fig. 7, dynamic performance of the EPS is presented, when the power of WIPS is changed. The power demand increases from 20 to 50 kW at 0.5 s, which results in the drop of 540-VDC bus voltage. Then, the power of WIPS returns to 20 kW at 1 s with the raise of the voltage.

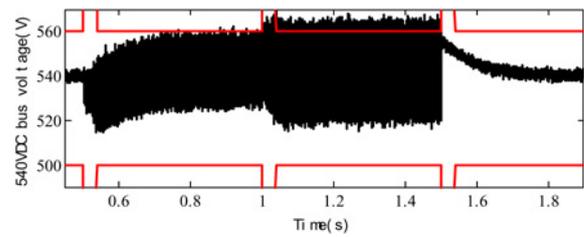
It is noted that the red line in Fig. 7a is the requirements of the voltage inherited from MIL-STD-704F [9], by double the limits of voltage for 270-VDC. In this case, the requirements are satisfied in both dynamic and steady state. It is easy to know that resistive load has little influence on the power quality in the steady state. For example, the voltage ripple of the 540-VDC bus voltage is  $\pm 1.2$  V in a time range from 0.9 to 1 s, which is much smaller than  $\pm 6$  V of the requirement in MIL-STD-704F.

##### 4.2 Converters

Fig. 8 indicates the voltage of 540-VDC bus while INV, CONV, and TRU load changing. The voltage ripple becomes quite large at 0.5 s, which is caused by the increase of 50-kW AC load and



**Fig. 7** Voltage of 540-VDC bus and input current of WIPS while WIPS load changing  
a Voltage of 540-VDC bus  
b Input current of WIPS

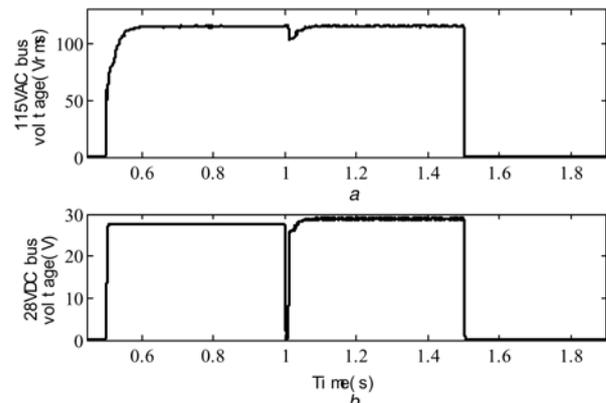


**Fig. 8** Voltage of 540-VDC bus while INV, CONV, and TRU load changing

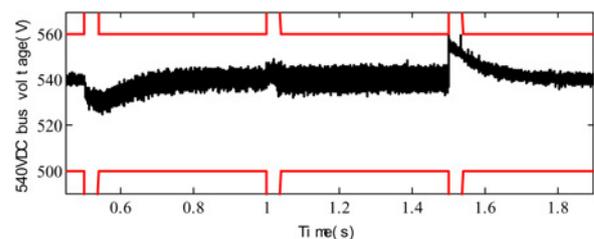
10-kW DC load on the 115-VAC bus and 28 VDC bus, respectively. More specifically, the ripple rises from  $\pm 3.5$  to  $\pm 18.8$  V, twice more than the requirement in MIL-STD-704F.

When a fault occurs on CONV at 1 s, the voltage of 28-VDC bus shown in Fig. 9 falls to zero. After 10 ms, TRU feeds the 28-VDC bus to recover the voltage. The voltage ripple becomes even larger ( $\pm 25.7$  V), exceeding the upper limit. Besides, the voltage ripple of the 28-VDC bus is also worsened from  $\pm 0.006$  V to  $\pm 0.245$  V. Consequently, it is considerable to change the filters of the INV to meet the power quality demands.

To validate the above analysis, the DC-link capacitors at the input ports of INV are increased from 0.3 to 0.8 mF, of which the simulation result of 230-VAC bus voltage is shown in Fig. 10. It is confirmed that modification of filters is helpful to decrease the voltage ripple and make power quality satisfy the demands in both steady and dynamic states, where the ripple in the steady state falls to  $\pm 5.9$  V at 0.9 s. However, a drawback is the increase in weight and cost, where some further studies are required to a trade-off between them. Besides, after the power increase of INV at 1 s, voltage ripple also rises to  $\pm 7.1$  V, exceeding the limit of MIL-STD-704F, which indicates that the capacitors are not large enough or that other solution are needed.



**Fig. 9** Voltage of 115-VAC bus and 28-VDC bus while INV, CONV, and TRU load changing  
a Voltage of 115-VAC bus  
b Voltage of 28-VDC bus



**Fig. 10** Voltage of 540-VDC bus while INV, CONV, and TRU load changing with the DC-link capacitors increased

### 4.3 Inverters and motors

When ECS load changing, the voltage of 230-VAC bus is given in Fig. 11. At 0.5 s, a load request of 60 kW processed by ECM, which is shown in Fig. 12a, results in the voltage drop of 230-VAC bus. Similar to the condition of INV, ECMC is also a large power inverter which has a side effect on the voltage ripple. So the DC-link capacitors of ECMC are set to be 0.8 mF to reduce the voltage ripple which is  $\pm 6.0$  V at 0.9 s.

At 1 s, the power demand of ECS reduces to 30 kW and the rotation speed of ECM varies from 30,000 to 15,000 r/min simultaneously. In Fig. 12b, the change of frequency of ECM input current can be seen, which causes the raise of voltage ripple to  $\pm 8.4$  V. It is inferred that the frequency change of the AC load can influence the ripple of DC voltage too, although the load power decreases.

Another testing case of inverter and motor is the FCS. As shown in Fig. 13, the transient voltage drop of the 540-VDC bus is dramatic, which is far below the limit of 400 V of the standard when loads of the two FCMs are set to be 10 and 5 kN, respectively, at 0.5 s. It is caused by the large torque requirement of FCM at the beginning of its working, which is indicated by the input current of FCMC1 in

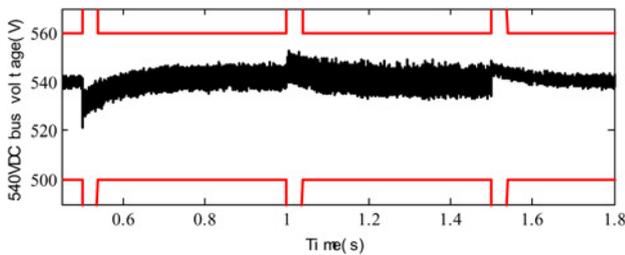


Fig. 11 Voltage of 540-VDC bus while ECS load changing

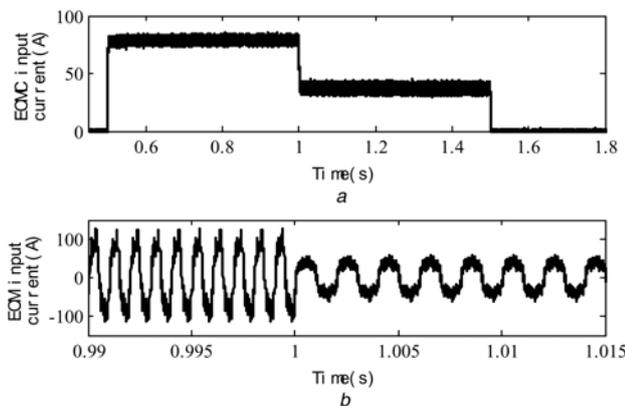


Fig. 12 Input current of ECMC and ECM while ECS load changing  
a Input current of ECMC  
b Input current of ECM

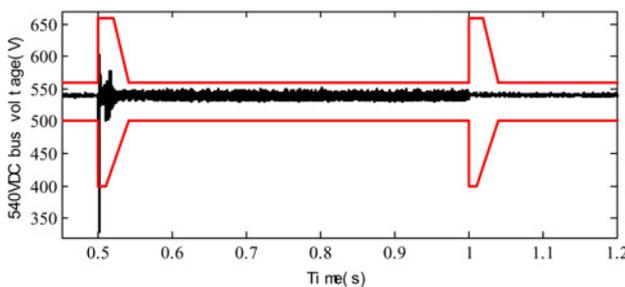


Fig. 13 Voltage of 540-VDC bus while FCS loads changing

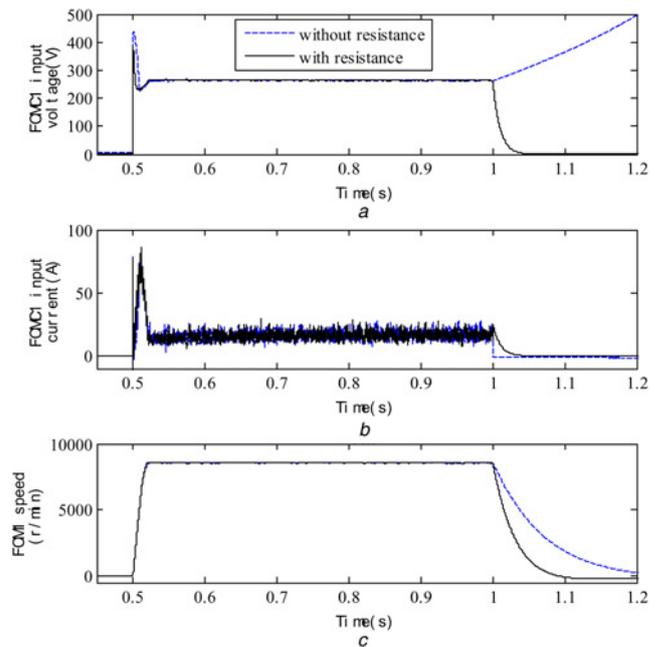


Fig. 14 Input voltage and input current of FCMC1 and speed of FCM1 while FCS loads changing  
a Input voltage of FCMC1  
b Input current of FCMC1  
c Speed of FCM1

blue dash line in Fig. 14. After the transient, current reaches a steady state and the voltage in Fig. 13 stays within the limit properly.

However, the voltage ripple of the 540-VDC bus also surpasses the limit, which is  $\pm 9.9$  V at 0.9 s, although the steady power of FCM1 is  $< 5$  kW. There are two levels of converters regulating the electric power to feed the FCMs, which is the reason for the ripple.

Another phenomenon should be noticed in Fig. 14 is that the voltage of FCMC1 increases at 1 s when the FCS stops operating instead of declining to zero. It caused by the regeneration of power of the FCM1 and rectification of the freewheeling diodes of the FCMC1. There are no energy storage or consumption elements in the circuit, resulting in the raise of voltage. But it has no influence on the 540-VDC bus thanks to the contractor at the input port of FCMC1.

To dissipate the regeneration energy, a paralleled resistance is installed at the input of FCMC. The simulation results are shown in black line in Fig. 14. The input voltage of FCMC1 is reduced to  $< 1$  V within 60 ms while the rotating speed of FCM also decelerates more dramatically.

## 5 Conclusion

In this paper, power quality of a proposed HVDC EPS for MEA is studied. Models from PMG and front-end rectifier to the loads are established with cables considered. Three typical kinds of loads are selected and their impacts on power quality are analysed by simulation, including resistive loads, PWM converters, and inverters and motors.

The results indicate that the influences of inverters are dramatic while the impact of resistance can be ignored. So filters of inverters should be designed carefully to alleviate the effect. Motors of large power such as motors in ECS also have a side effect on power quality, whose frequency is variable when power changing. The influence of FCS is indicated mainly at the beginning of operation with a large current demand, which causes a huge voltage drop and the dissipation of regeneration energy which may induce the raise of DC voltage. Another phenomenon that should be noticed

is that power quality of the 28 VDC power fed by 115 VAC is deteriorated. So it may be necessary for the proposed EPS system to design an individual power supply channel in order to feed the essential loads of 28-VDC bus.

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