The 4th International Symposium on More Electric Aircraft Technology (MEA 2017)

8–9 November 2017

Vector control implementation in field programmable gate array for 200 kHz GaN-based motor drive systems

Zhiwen Luo[1], *Yongdong Li*[2], *Xinyan Zhang*[1], *Kui Wang*[2]

[1]*College of Electrical Engineering, Xinjiang University, Urumqi, People's Republic of China*
[2]*Department of Electrical Engineering, Tsinghua University, Beijing, People's Republic of China*
E-mail: wangkui@tsinghua.edu.cn

Published in *The Journal of Engineering*; Received on 10th January 2018; Revised on 21st February 2018; Accepted on 5th March 2018

Abstract: GaN devices used to drive a three-phase inverter drive motor can greatly improve the switching frequency and increase the power density. However, the traditional microcontroller unit (MCU) controller cannot achieve high switching frequency single-cycle control. This paper describes the use of GaN devices in the design of a three-phase motor drive system to drive a permanent magnet synchronous motor and vector control algorithm, that is completely implemented in a field programmable gate array. The system achieves 200-kHz switching frequency single-cycle precise control, as verified by the experimental results.

1 Introduction

The rapid development wide bandgap devices based on GaN and SiC provide the potential to improve the power density of power conversion systems [1–3]. Compared to its silicon (Si) counterparts, GaN offers lower resistance and higher switching speed under the same operating conditions. In the field of motor control, Si-based devices suffer low switching frequency control problems. Furthermore, the trend of miniaturisation of the motors used in electric aircraft and future machines is leading to the use of 10,000–100,000 rpm high-speed rotating motors [4]. To take full advantage of the high switching frequency of GaN devices in the motor control, it is necessary to increase the current control frequency.

The conventional motor control uses microcontrollers or digital signal processing (DSP) chips to perform all the algorithms. They have some advantages, such as ease of programming and the possibility to provide a pulse width modulation (PWM) generator. However, they must execute all the algorithms in sequence, hence limiting the speed of calculating the algorithm. To solve this problem, currently, the multi-CPU approach must be used in some applications. This inevitably leads to complex control and cost increases.

In this paper, a new hardware platform is used. All the motor vector algorithms are used to complete the field programmable gate array (FPGA), thus greatly improving the computational time of the algorithm and the reliability of the algorithm. The controller used is Xilinx company's ZYNQ-7000. This controller is an embedded dual CPU and FPGA, and between the CPU and FPGA is a flexible and high-speed bus interface.

2 GaN high electron mobility transistor (HEMT) three-phase design

The first-generation GaN power transistor was first made available to the market in 2007 [3]. The current commercial maximum power of a GaN power transistor is 650 V/60 A designed by a GaN system company. This GaN power transistor has a very small value of Rds (on)**Q*g = 748.2 mΩ*nC, which allows for high switching frequency. Moreover, the package uses laminate surface mounted devices (SMD), which offers ultra-low package inductance, and the top side cooling also provides the convenience of heat sink installation. Thus, the GaN system device (GS66516 T) is quite suitable for use in a high-power density inverter [5, 6].

To reduce the bus stray inductance and facilitate printed circuit board (PCB) design, the GaN HEMT three-phase inverter structure, which involves a three daughter-board and motherboard design, is used. The daughter-board drive circuit and the PCB structure are shown in Fig. 1.

Each daughter board is a half bridge circuit, and the SI8233AD drive chip is used to drive the GaN HEMT circuit. This drive chip can supply 4 A of current when the GaN HEMT during the opening moment. In addition, a output enables and hardware dead is supplied [7]. Furthermore, to prevent driving crosstalk caused by the Miller effect, resulting in the wrong opening of the GaN HEMT, the active clamp PNP triode (Q2, Q4) is used. The GaN HEMT is installed on the top layer for ease of installation of the 37.5 mm × 37.5 mm heat sink. The 4-mm gold-plate pin is used as the power interface on the daughter board to reduce bus stray inductance.

A three-phase GaN HEMT inverter with volume of 12 cm × 15 cm × 4 cm is shown in Fig. 2. Fig. 2*a* shows how each daughter-board is installed in the motherboard. Figs. 2*b* and *c* show a complete structure of front view and side view; a pen is used to indicate the real volume.

To ensure the pulse signal is not disturbed, a three-fibre interface of 10 MHz bandwidth is used to transmit each phase of the PWM signal. Twenty-four volts are the drive signal and logic signal of the main power source; the isolate DC–DC power module is used for the corresponding voltage-level conversion.

Since the full turn-on voltage of the GaN HEMT device is 6.8 V, the threshold voltage is 1.4 V, and the turn-off voltage is 0 V. Thus, the PCB design of the driver circuit is critical, and the minimum loop impedance of the driver circuit must be ensured. To test the stability of the GaN HEMT, the drive circuit must perform the double pulse test. Fig. 2 shows the double pulse test waveform.

According to Fig. 3, when the bus voltage is 400 V, the GaN HEMT turn-on time is ∼30 ns, and the VGs do not exhibit a drive ring. Moreover, during the turn-off time, the active clamp transistor occurs around the negative voltage; this process is conducive to reducing the drive crosstalk, which proves the GaN HEMT drive circuit design is reliable (Figs. 4 and 5).

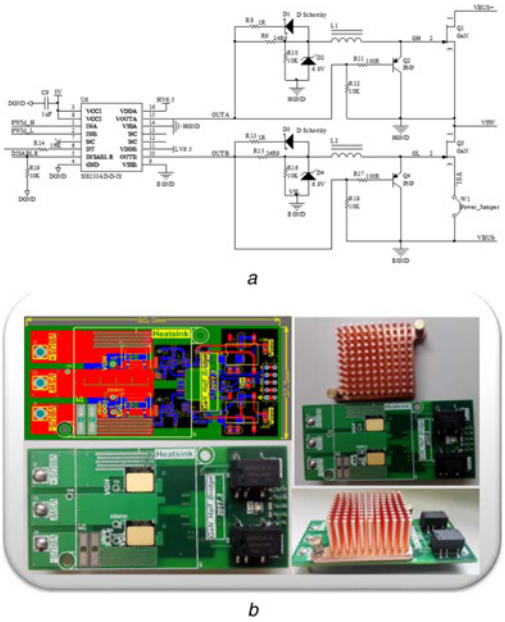

Fig. 1 *Daughter-board drive circuit and PCB structure*

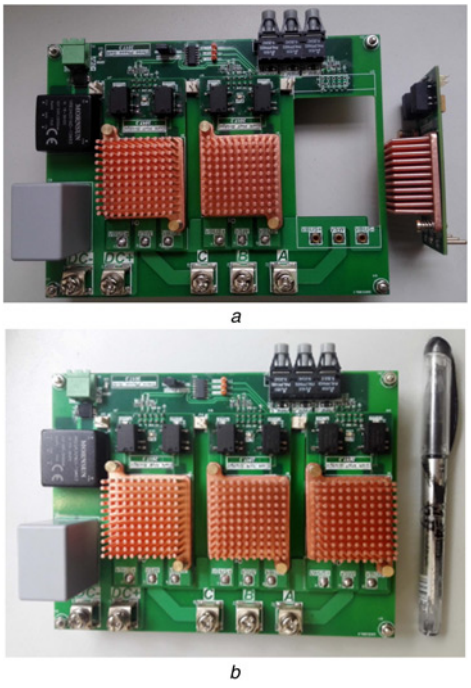

Fig. 2 *Three-phase GaN HEMT inverter motherboard and daughter-board structure*
(a) Not fully installed, ***(b)*** Front view

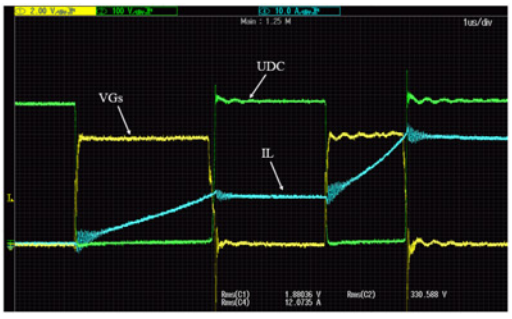

Fig. 3 *Double pulse test waveform*

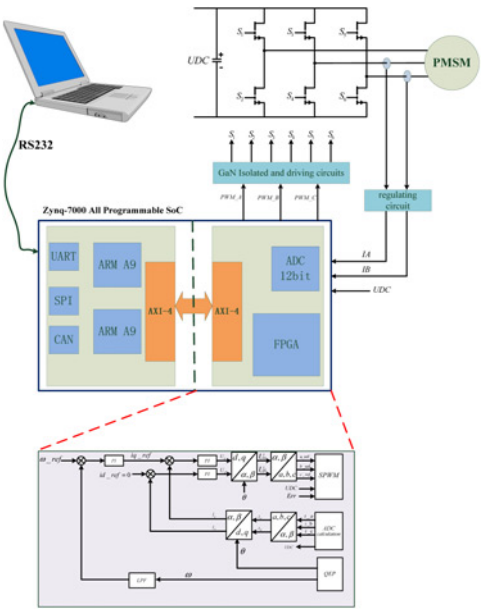

Fig. 4 *Structure of the system framework*

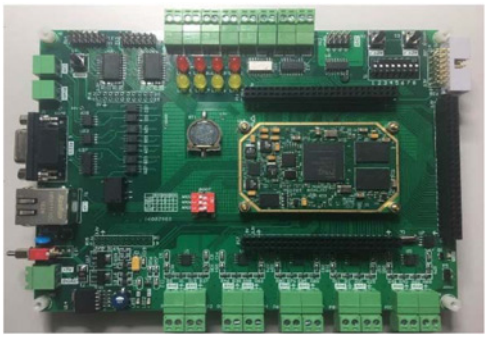

Fig. 5 *Core controller ZYNQ-7000*

3 Vector control implementation in FPGA

To optimise the performance of GaN HEMT inverters, the traditional microprocessor control methods must be discarded. Thus, the implementation of the motor vector control algorithm in FPGA to achieve hardware acceleration is an excellent method. In addition to reducing the algorithm running speed to within 1 μs, the FPGA is insensitive to external interference [8, 9].

This design uses the latest ZYNQ-7000 controller from Xilinx, which integrates a dual ARM Cortex-A9 MPCore hard process core and FPGA logic resources. The chip has a high-speed data exchange bus between the FPGA and the CPU.

The entire motor vector control algorithm runs in the FPGA, not only reducing the algorithm run time but also enhancing the reliability of the system [10, 11]. The motor current through the conditioning circuit is directly read by the embedded analog-to-digital converter (ADC). During each current control cycle, the FPGA can directly read the current value, and then the vector control algorithm will be implemented. Finally, the PWM signal will be generated by the FPGA, and then the PWM signal via the high-speed (10 MHz) fibre is sent to the GaN HEMT inverter.

All of the system initialisation parameters are first calculated by the ARM A9 processor and then are sent to the FPGA vector algorithm intellectual property (IP) core through the AXI-4 inter communicate bus. To facilitate system parameter debugging, the vector algorithm running in the FPGA can be transmitted to the ARM A9 processor through the high-speed AXI-4 inter

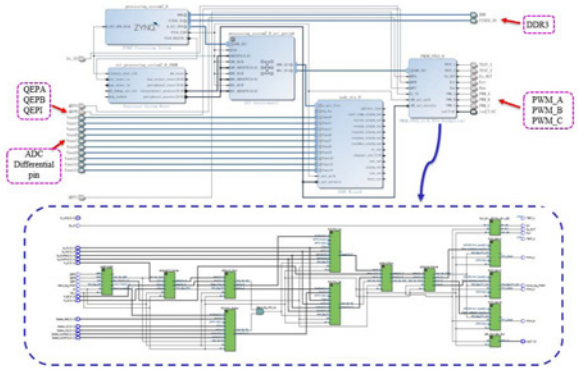

Fig. 6 *Vector algorithm symbol in FPGA*

communicate bus. Finally, the data is sent through the RS232 serial port to communicate with the PC.

In this design, the core controller includes a ZYNQ-7000 processor, an analogue-to-digital convener conditioning circuit, an Ethernet and RS232 communication interface and a fibre board interface.

In the algorithm design of the FPGA, the timing is the most important factor. So in this vector algorithm design, using hierarchical and modular structure design method. Finally, the whole vector control algorithm is divided into proportion integration differentiation (PID), QEP, Clark, IClark, Park, iPark, LPF module as shown in Fig. 6. In addition, the advantages of using this design can facilitate the debug of a signal module and also conducive to the FPGA design timing [12].

After each module design is completed, the logic of the algorithm is first verified on the ModelSim software. Fig. 7 shows the some model's behavioural simulation verified in ModelSim software, includes the coordinate transformation, PID implementation, and QEP to get the speed and angle.

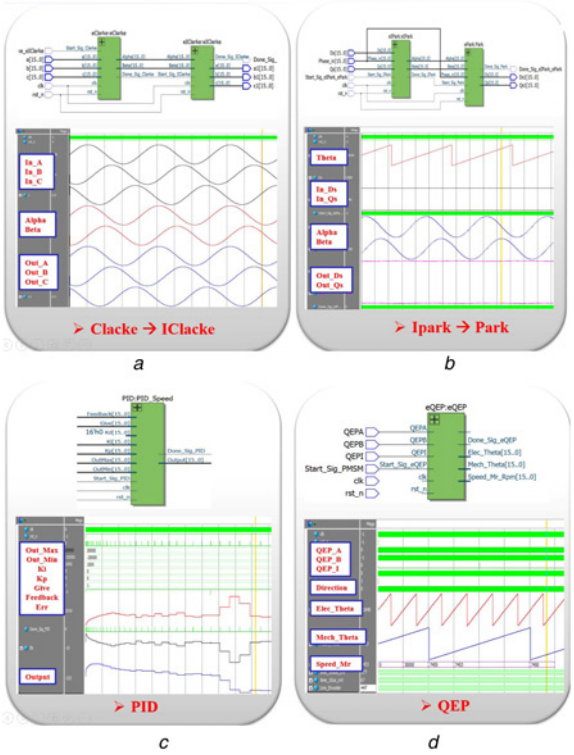

Fig. 7 *Coordinate transformation*
(a) Clacke to IClacke, ***(b)*** Ipark to Park, ***(c)*** PID, ***(d)*** QEP

To accurately verify that the coordinate module can work normally, the design packet verification method is used. Here, Clack-IClacke and IPark-Park are allocated to alternate groups. In the Clack-IClacke group, shown in Fig. 7*a*, In_A, In_B, and In_C are the input signals sent to the Clacke module, which outputs the Alpha and Beta signal; these signals are sent to the IClacke module, which then outputs the Out_A, Out_B, and Out_C signals. Finally, comparing the In _A and Out_A, In _B and Out_B, In _C and Out_C, if each group of signals has the same amplitude and phase, then the module is designed correctly.

The Ipark-Park group shown in Fig. 7*b* has the same detection method: In_Ds, In_Qs and Theta signals are the input signals of Ipark, and the Park module generates the Out_Ds and Out_Qs signals. The amplitudes of In_Ds and Out_Ds and those of In_Qs and Out_Qs are compared to determine whether they are equal.

In the PID module shown in Fig. 7*c*, the first-order Duler method is used to discretise the PID formula. The module input is the initial values of Kp, Ki, Out_Max, Out_Min and Give. The feedback variable is generated by the simulation. Finally, the Err and Output signals' change trends are examined to verify whether the module design is correct.

The QEP module is shown in Fig. 7*d*; the output of the photoelectric encoder orthogonal QEP_A, QEP_B, and QEP_Z signals is used to calculate the motor speed and the mechanical and electrical angles. Verification is also achieved through examination of the

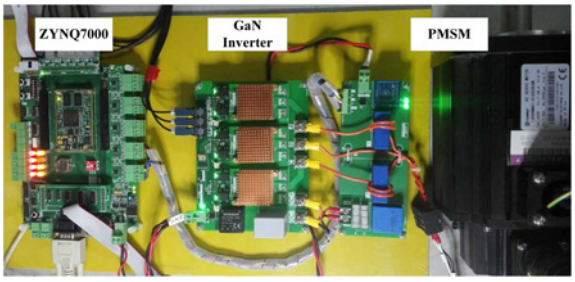

Fig. 8 *GaN-base inverter motor experimental platform*

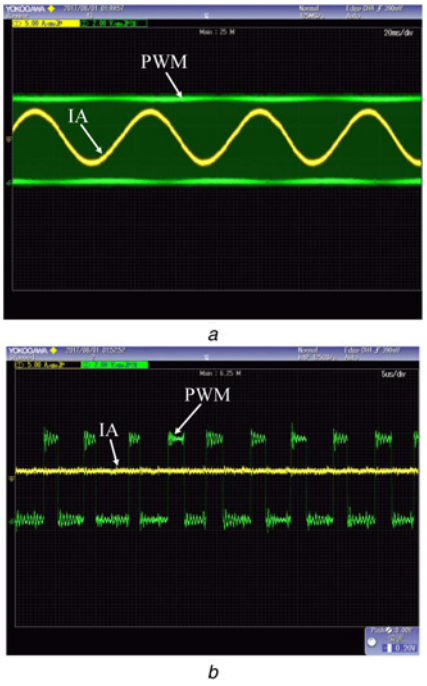

Fig. 9 *Phase current of the PMSM and the PWM signal*
(a) Original waveform, ***(b)*** Magnified view of part of the waveform

doi: 10.1049/joe.2018.0032

simulation input QEP_A, QEP_B, QEP_Z signals to determine if the output variable is correct.

4 Experiment

All algorithms must be experimentally validated on a GaN-based experimental platform. Fig. 8 shows the GaN-based inverter motor experimental platform, Including the ZYNQ-7000 core controller, the GaN-based inverter, and the PMSM motor.

The motor's control commands are sent to the core controller via the PC to the ARM A9 of the ZYNQ7000 and then to the FPGA logic IP unit via the AXI-4 bus.

The motor control parameters are adjusted to control the PMSM at the control frequency of 200 kHz. Fig. 9 shows the PMSM's single-phase current waveform and the PWM signal.

Fig. 9*a* shows that, at the switching frequency of 200 kHz, the PMSM's single-phase current is better. The magnified view of the partial waveform shown in Fig. 9*b* shows that the rate of change of current is very small.

5 Conclusion

In this paper, a three-phase inverter was designed based on GaN devices, and then the vector control algorithm of the motor was realised in the FPGA. Each algorithm module was validated in the ModelSim software regarding the behaviour of logic simulation to ensure the algorithm's correctness. Finally, all the algorithms were transplanted into the ZYNQ7000 processor to control a PMSM and the reliability of vector algorithm was verified experimentally.

6 Acknowledgments

The authors acknowledge the Power Electronics and Motor Control research group at the Tsinghua University Department of Electrical Engineering for providing support.

7 References

[1] Xue L., Shen Z., Boroyevich D.: 'Dual active bridge-based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple', *IEEE Trans. Power Electron.*, 2015, **30**, (12), pp. 7299–7307

[2] Guo F., Fu L., Li H.: 'A dual-input full-bridge current-source isolated DC/DC converter based on quasi-switched-capacitor circuit for photovoltaic systems with energy storage'. Proc. IEEE Appl. Power, Applied Power Electronics Conference & Exposition, 2015, pp. 1757–1762

[3] Li H., Zhang X., Zhang Z.: 'Design of a 10 kW GaN-based high power density three-phase inverter'. 2016 IEEE Energy Conversio. Energy Conversion Congress & Exposition, 2017, pp. 1–8

[4] Jeppesen B.P., Crosland A., Chau T.: 'An FPGA-based platform for integrated power and motion control'. IECON 2016–42nd Annual Conf. IEEE Industrial Electronics Society, Florence, 2016, pp. 2684–2689

[5] Wu Y.F.: 'Paralleling high-speed GaN power HEMTs for quadrupled power output'. Proc. Applied Power Electronics Conf. Exposition (APEC), 2013 IEEE, 17–21 March 2013, pp. 211–214

[6] Li H., Zhang X., Wen L.: 'Evaluation of high voltage cascode GaN HEMTs in parallel operation'. In Proc. 2016 IEEE Applied Power Electronics Conf. Exposition (APEC), Long Beach, CA, 2016, pp. 990–995

[7] Lu J., Tian Q., Bai K.: 'An indirect matrix converter based 97%-efficiency onboard level 2 battery charger using E-mode GaN HEMTs'. Proc. Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2015 IEEE 3rd Workshop on, Blacksburg, VA, 2015, pp. 351–358

[8] Dahm N., Huebner M., Becker J.: 'FPGA system-on-chip solution for a field oriented hybrid stepper motor control'. 2012 9th Int. Multi-Conf. Systems, Signals and Devices, 2012, pp. 1–6

[9] Saxena A.: 'Performance and cost comparison of PM BLDC motors for ceiling fan'. 2014 IEEE Int. Conf. PowerElectronics, Drives and Energy Systems (PEDES), 2015, pp. 1–5

[10] Vazquez Mora J.L., Lelkes A., Pacas J.M.: 'External rotor pm motor fed by a load commutated inverter for fan applications'. Proc. IEEE 2002 28th Annual Conf. IECON 02, 2002, vol. 1, pp. 767–770

[11] Li S., Zhou B., Liu Y, Feng Y.: 'A novel method of initial rotor position estimation for surface mounted permanent magnet synchronous motor'. 2010 Int. Conf. Electrical and Control Engineering, 2010, pp. 4924–4927

[12] Kung Y.S., Risfendra R., Lin Y.D., *ET AL.*: 'FPGA-realization of a sensorless speed controller for PMSM drives using novel sliding mode observer', On-line publication by Microsystem Technologies