

Research on the modulation and control of multilevel matrix converter

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Published in *The Journal of Engineering*; Received on 25th January 2018; Accepted on 2nd February 2018

Abstract: This paper discusses the effects of different space vector modulation (SVM) hexagon partition on common mode voltage suppression at high modulation index and presents an improved capacitor voltage balance strategy for multilevel matrix converter. Matrix converter is a compact designed converter which allows direct AC–AC power transfer without an intermediate DC link. Multilevel matrix converters, which utilises a multilevel structure on a traditional matrix converter, expand these characters to high-voltage and high-power situations. This paper is concerned with SVM of three-level matrix converter and concentrates on the comparison between different hexagon partitions; the improved balancing strategy is employed to improve the performance of flying capacitor voltage control. Simulation from Matlab/Simulink and results from a small-scale experimental prototype are presented to validate the theoretical results.

1. Introduction

The conventional three-phase to three-phase matrix converter consists of an array of nine bi-directional switches arranged so that any output line can connect to any input line. The conventional matrix converter can generate the desired outputs with arbitrary amplitude and frequency [1, 2].

Due to the advantages in using multi-level technology, such as improved power quality, fewer harmonics and extended power rating [3], the multi-level topology has been widely accepted in many application [4–6]. The multi-level converter can synthesise the required waveforms from several levels of voltages (at least three levels).

In a capacitor clamped multi-level converter, the extra voltage levels are provided and maintained by a group of properly controlled flying capacitors. The voltage levels across the flying capacitors can be controlled by charging or discharging the corresponding flying capacitors [7]. As a typical capacitor clamped multi-level inverter is shown in Fig. 1.

The three-level capacitor-clamped matrix converter consists of eighteen bi-directional switches and requires one clamping capacitor per input or output leg, giving a total of nine capacitors. Modulation index was limited to 0.5 when Venturini strategy is adopted [8].

The space vector modulation (SVM) of multilevel matrix converter (MLMC) first introduced by transferring MLMC modulation problems to several MC modulation problems [9]; also amplitude coefficient was employed in duty calculation to improve the performance in terms of modulation precision [10].

However, in the high-voltage and high-power frequency conversion speed regulation system, considering the reliability of the control system, and the service life of the AC motor, the common mode voltage (CMV) must be considered, for a three-phase system, the CMV can be represented as

$$V_{cm} = \frac{V_u + V_v + V_w}{3} \quad (1)$$

where V_i ($i = u, v, w$) means the output voltage of each phase of the matrix converter.

In order to reduce the CMV of MC, many modulation strategies have been presented [11–14], but they all focus on the modulation of MC at low modulation index. In [15], the modulation of CMV suppression for three-level matrix converter (3LMC) is presented, but it also only be useful at the low modulation index.

As a continuous of previous works on multilevel matrix converter and CMV suppression, this paper focus on the different SVM hexagon partition of MLMC and proposes a novel capacitor balance strategy, which can make fully use of redundant switching states and useful to reduce CMV. The content of this paper is organised as follows: Section 2 reviews the 3LMC topology and compares four different SVM hexagon partitions; Section 3 presents the basic 3LMC flying capacitor voltage control and the proposed capacitor voltage balance strategy, the mathematic derivation of utility function and the difference in voltage states selection; Section 4 presents the simulation results to validate the theoretical finding; Section 5 presents the experimental prototype and experimental results.

2. Space vector modulation for 3LMC

2.1 Review of multilevel matrix converter SVM

Space vector theory allows a three-phase set of quantities to be represented by a single vector on a complex plane. Advantage of SVM over modified Venturini modulation includes its robust, less amount of calculation, high-voltage transfer ratio etc. Its application to MC modulation [1, 2] is as follows.

Referring to Fig. 2, the voltage and current vector from three phases can be written as

$$\begin{cases} V_A = V_{in} \cos(\omega_{in} t) \\ V_B = V_{in} \cos(\omega_{in} t - 2\pi/3) \\ V_C = V_{in} \cos(\omega_{in} t - 4\pi/3) \end{cases} \quad (2)$$

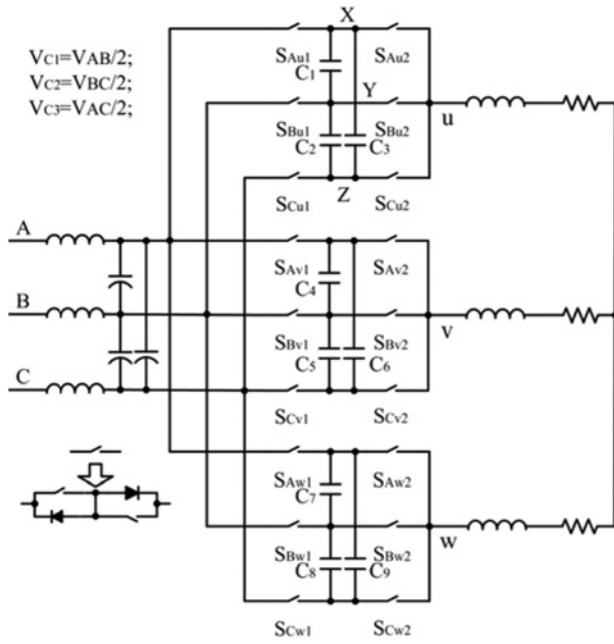


Fig. 1 Topology of three-level matrix converter

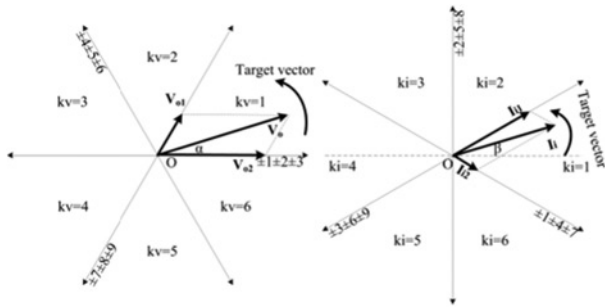


Fig. 2 Current and voltage SVM of matrix converter

$$\begin{cases} I_{in} = 2(I_A + I_B e^{j2\pi/3} + I_C e^{j4\pi/3})/3 \\ V_o = 2(V_u + V_v e^{j2\pi/3} + V_w e^{j4\pi/3})/3 \end{cases} \quad (3)$$

$$\begin{cases} \text{Re}_{I_{in}} = (2I_A - I_B - I_C)/3 \\ \text{Im}_{I_{in}} = (I_B - I_C)/\sqrt{3} \\ \omega_i t = k\pi \pm \arctan(\text{Im}_{I_{in}}/\text{Re}_{I_{in}}) \end{cases} \quad (4)$$

$$\begin{cases} \text{Re}_{V_o} = (2V_u - V_v - V_w)/3 \\ \text{Im}_{V_o} = (V_v - V_w)/\sqrt{3} \\ \omega_o t = k\pi \pm \arctan(\text{Im}_{V_o}/\text{Re}_{V_o}) \end{cases} \quad (5)$$

where I_{in} and V_o are the input current and output voltage space vector, Re and Im label the real and imaginary parts of the space vector, the ω_o and ω_i are the output voltage and input current vector velocity in rad/s.

For a conventional MC, there are $27(3^3)$ allowable switching states. Expressed as space vectors, 18 of these states produce stationary vectors and a further three produces zero vectors. The remaining six states produce rotating vectors with variable angles which are generally not useful in the SVM. Eighteen states can be labeled from '±1' to '±9' by their voltage and current directions; four of these states will be employed in every single modulation cycle.

Table 1 Voltage states available

No	Switching state	Output voltage state	Input current state
1(F)	$S_{Ai1}S_{Ai2}$	V_A	i_o injected into A
2(F)	$S_{Bi1}S_{Bi2}$	V_B	i_o injected into B
3(F)	$S_{Ci1}S_{Ci2}$	V_C	i_o injected into C
4(H)	$S_{Bi1}S_{Ci2}$	$(V_B + V_C)/2$	i_{oi} injected into B
	$S_{Ci1}S_{Bi2}$	$(V_B + V_C)/2$	i_o injected into C
5(H)	$S_{Ci1}S_{Ai2}$	$(V_C + V_A)/2$	i_o injected into C
	$S_{Ai1}S_{Ci2}$	$(V_C + V_A)/2$	i_o injected into A
6(H)	$S_{Ai1}S_{Bi2}$	$(V_A + V_B)/2$	i_o injected into A
	$S_{Bi1}S_{Ai2}$	$(V_A + V_B)/2$	i_o injected into B

'F' denotes full voltage output; 'H' denotes half voltage output.

Compared to multilevel AC–DC–AC converters, multilevel MCs do not have the large DC capacitors to maintain the DC-link energy and the flying capacitor voltage need to be controlled to be sinusoidal waveform. Hence, the voltage of capacitors to be sinusoidal waveform. Hence, the voltage of capacitors in multilevel MCs must track half line–line voltages, which are $V_{AB}/2$, $V_{BC}/2$, and $V_{AC}/2$. As shown in Table 1, each output phase can output six different voltages, respectively (shown in Table 1), thus lead to $729(9^3)$ allowable switching states and $216(6^3)$ allowable voltage states for the three-input and three-output case.

In [15], to simplify the modulation, the SVM of the 3LMC can be regarded as a combination of four subsystem (shown in Fig. 3), and each subsystem can be seen as an independent MC with the different number of redundant states.

The subsystems 1, 2, 3 do not have redundant states, but each space vector in subsystem 4 can be produced by three kinds of switching states, the example states are shown in Table 2.

2.2 SVM hexagon partition I

In this partition, every 60° sector can be divided into four triangles (shown in Fig. 4); these four triangles consist of two equivalent triangles (2 and 4) and two obtuse triangles (1 and 3).

2.3 SVM hexagon partition II

By merging the subsystems with the same phase shift and similar amplitudes, SVM hexagon partition can be simplified. As shown in Fig. 5, after subsystem 2 is replaced by subsystem 1, the remaining three subsystems are used to synthesis the output voltage. This partition is same to SVM hexagon of three-level neutral-point-clamped converter and be a candidate to consider.

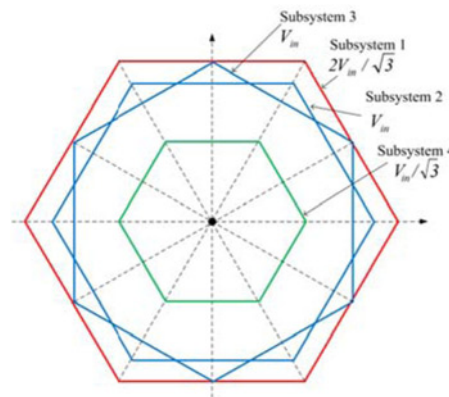
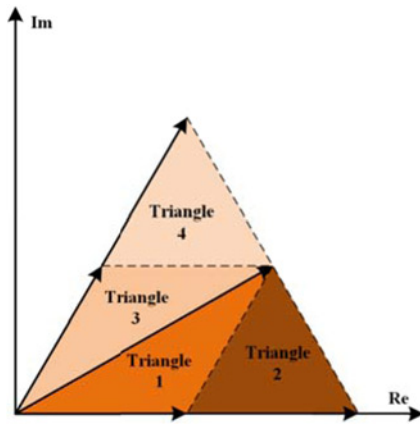
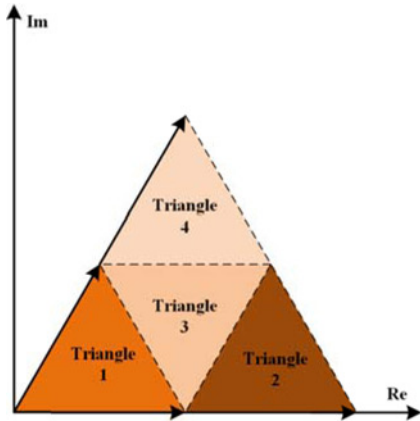


Fig. 3 SVM voltage hexagon for three-level matrix converter

Table 2 Voltage states for subsystem 4

States (+)	Voltage states (+)	States (-)	Voltage states (-)
+1	{1,6,6}	-1	{6,1,1}
	{6,2,2}		{2,6,6}
	{5,4,4}		{4,5,5}
+2	{2,4,4}	-2	{4,2,2}
	{4,3,3}		{3,4,4}
	{6,5,5}		{5,6,6}
+3	{3,5,5}	-3	{5,3,3}
	{5,1,1}		{1,5,5}
	{4,6,6}		{6,4,4}

{1, 6, 6} means $V_U = V_A$, $V_V = (V_A + V_B)/2$, $V_W = (V_A + V_B)/2$, the rest is similar.

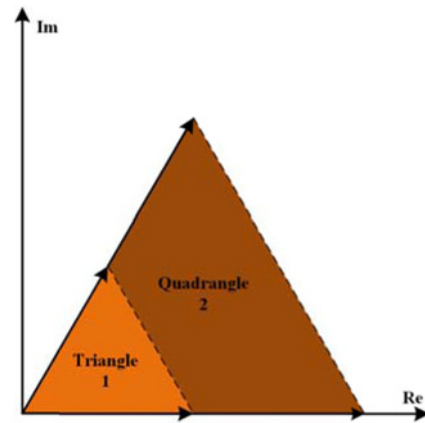
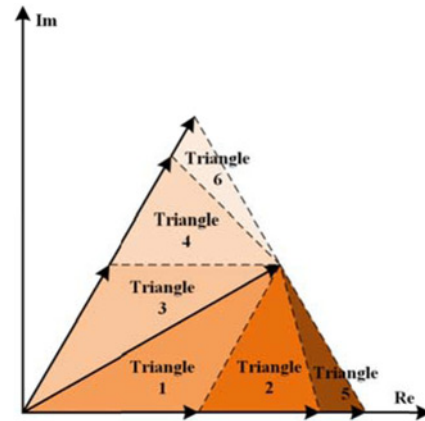
**Fig. 4** SVM hexagon partition consists of obtuse and equilateral triangles**Fig. 5** SVM hexagon partition consists of equilateral triangles

2.4 SVM hexagon partition III

For the sake of simplification, modulation that only employs the most typical voltage states is shown in Fig. 6. Section denoted by triangle 1 is a scaled-down version of matrix SVM hexagon; unlike triangle, quadrangle needs eight vectors to synthesis, modulation in quadrangle 2 can be regarded as control cycle separated into two matrix converters; operation time of which is decided by modulation index.

2.5 SVM hexagon partition IV

SVM hexagon IV contains all four subsystems. In Fig. 7, every 60° sector can be divided into six triangles as shown in Fig. 7. The six

**Fig. 6** SVM hexagon partition consists of triangle and quadrangle**Fig. 7** SVM hexagon partition consists of six triangles

triangles consist of both oxygen triangles (3, 4) and obtuse triangle (1, 2, 5 and 6). Modulation with full subsystems will make full use of voltage states. There are no redundant states in triangles 5 and 6.

Note that SVM hexagon partition IV has the densest division, modulation with all four subsystems can make full use of voltage states, more half amplitude voltage states can be used, which is effectively helped in the suppression of CMV and the balance of the flying capacitor voltages. Especially with high modulation index, it can avoid to use subsystem 1 at the most of the situation, since the subsystem 1 only consists of full amplitude states and produce maximum CMV than other subsystems.

2.6 Four-step commutation and vector sequence with minimum dead-zone loss

The four-step commutation acts as an important role in MC SVM which has already been discussed in [9]. The four-step commutation of MLMC can be regarded as two individual MC four-step commutations [10]. Nine switches from S_{AU1} to S_{CW1} commute independently from the other nine.

In triangle modulation, six vectors are adopted to synthesis the output, vector sequence that smooth the output THD should be symmetry and the minimum of four-step duty loss. The sequence: $V_5 \rightarrow V_3 \rightarrow V_1 \rightarrow V_2 \rightarrow V_4 \rightarrow V_6 \rightarrow V_4 \rightarrow V_2 \rightarrow V_1 \rightarrow V_3 \rightarrow V_5$ which satisfies both criterions are employed in synthesis.

3 Flying capacitor voltage control for 3LMC

3.1 Basic flying capacitor balance strategy

There are three redundant switching states available when vectors from subsystem 4 are employed in modulation, note that half

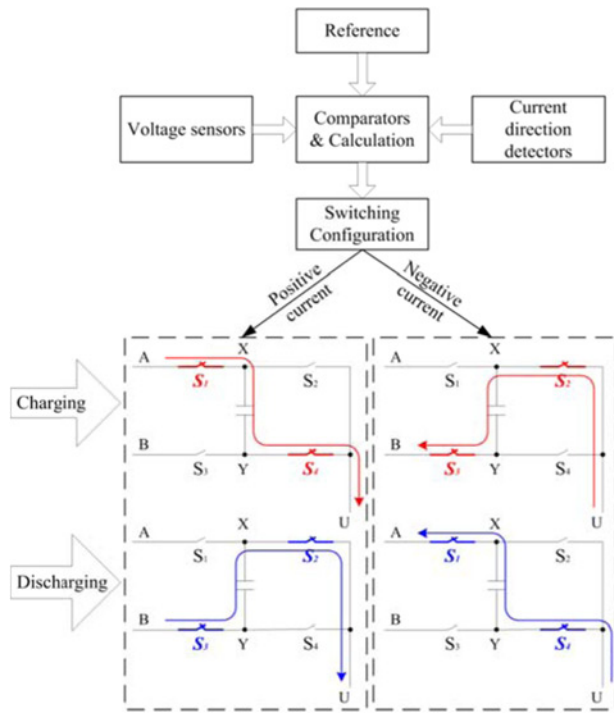


Fig. 8 Basic flying capacitor balance algorithm

voltage states influence capacitor voltage more than full voltage states, using {5,4,4} other than {1,6,6} in state '+1' will better control the capacitor intuitively. Fig. 8 illustrates the basic balance control algorithm for a certain half voltage output, using direction of output current and capacitor status (need to charge or discharge) to determine the accurate current path and then the switching patterns. By employing half voltage states, it is obvious that all flying capacitor can be controlled at either charging or discharging states without affecting the instantaneous output voltage:

- (i) *For positive current*: if voltages of flying capacitors lower than reference, the capacitor needs to be charged and the switches S_1 and S_4 are switched on; if not, the capacitor needs to be discharged and the switches S_2 and S_3 are switched on.
- (ii) *For negative current*: if voltage of flying capacitor lower than reference, the capacitor needs to be charged and the switches S_2 and S_3 are switched on. If not, the capacitor needs to be discharged and the switches S_1 and S_4 are switched on.

Considering that flying capacitors have a relatively small capacity (usually several μF), this balance strategy will operate every time when output half voltage.

3.2 Flying capacitor control based on utility function

For a low-modulation index situation, small current is risky to maintain the sinusoidal capacitor voltage; on the other hand, when load current is considerable high, capacitors may have too much voltage disturbance, because of the single charge or discharge operation in control cycle. Note that redundant states of subsystem 4 is more than others, making full use of the redundant states in this subsystem will benefit capacitor balance.

Utility function is a solution to this complex capacitor problem; the proposed balance strategy based on utility function (shown in Fig. 9) includes the following steps:

- (i) *Set up a matrix to demonstrate the voltage gap*: Matrix that contains information of all capacitors should be set up to satisfy the

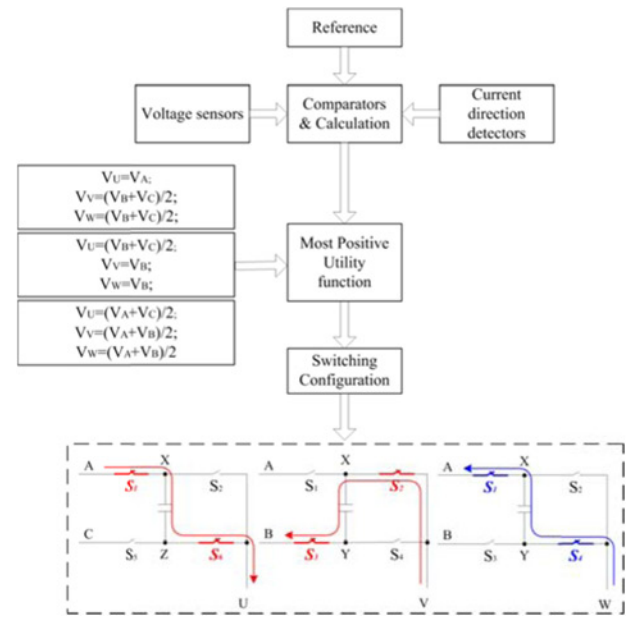


Fig. 9 Proposed flying capacitor balance algorithm using utility function

quantitative analysis needs:

$$M_{\text{cap}} = \begin{bmatrix} \text{ref}C_1 - U_{C1} & \text{ref}C_2 - U_{C2} & \text{ref}C_3 - U_{C3} \\ \text{ref}C_1 - U_{C4} & \text{ref}C_2 - U_{C5} & \text{ref}C_3 - U_{C6} \\ \text{ref}C_1 - U_{C7} & \text{ref}C_2 - U_{C8} & \text{ref}C_3 - U_{C9} \end{bmatrix} \quad (6)$$

where nine elements in M_{cap} indicate the voltage gap between real value and reference value of flying capacitors.

- (ii) *Take consider of the influence of output current*: Note that current of different amplitude or direction will have different influence on flying capacitor; voltage gap from each phase should multiply the corresponding phase current to describe the influence:

$$\begin{cases} M_{\text{cap},j}(1,j) = M_{\text{cap}}(1,j) \times I_U \\ M_{\text{cap},j}(2,j) = M_{\text{cap}}(2,j) \times I_V \\ M_{\text{cap},j}(3,j) = M_{\text{cap}}(3,j) \times I_W \end{cases} \quad (7)$$

- (iii) *Enumerate different voltage states and calculate the corresponding utility functions*: After voltage states selection and duty cycle calculation, all possible switching states will be enumerated with influence matrix to predict the prospective capacitor voltage. Choose the switching states that maximise utility function will drive capacitor closer to their theoretical value.

- (iv) *Employ states which imply the most positive utility function*: For every vector from V_1 to V_6 , repeat the former steps to let voltage of capacitors track their reference, which is a prerequisite to output accurate voltage.

According to the SVM hexagon, the number of redundant states in each subsystem is different. These redundant states produce the same output voltage vector, but lead to different input current states and different flying capacitor charging or discharging. In the same way as for other multilevel topologies, more redundant states mean better control of the flying capacitor voltage. Difference between basic balance strategy and proposed strategy includes:

- (i) Basic balance strategy chooses voltage states which affect capacitors the most and ignore redundant states while the proposed one can make full use of all available states.

(ii) Basic balance strategy deal with single capacitor at a time while the proposed one considers all capacitors as a whole to balance by adopting utility function.

4 Simulation results

To validate the theoretical findings, an MATLAB simulation is utilised, parameters of which are shown in Table 3. Results with different hexagon partitions and different flying capacitor control strategies are presented to verify the analysis.

Figs. 10 and 11 show the simulation results of the 3LMC using SVM hexagon partition I with a modulation index of 60%. Figs. 12 and 13 show the simulation results of the 3LMC using

Table 3 Simulation parameters

Simulation parameters	Value	Comment
input phase voltage	100 V (peak)	three phase
input frequency	50 Hz	—
reference output voltage	60 V (peak)	60% modulation index
reference output frequency	70 Hz	—
load	10 mH + 5 Ω	three-phase RL load
flying capacitors	2.5 μ F	Δ connected
switching frequency	2.5 kHz	—
IGBT turn off delay	45 ns	—

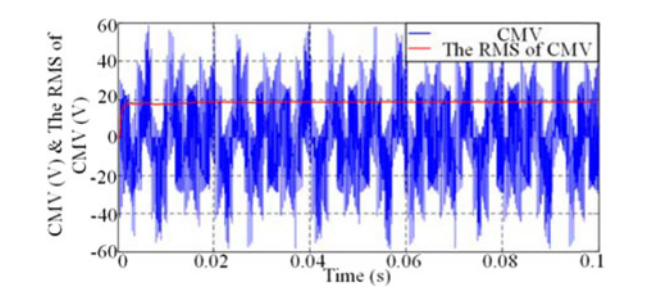


Fig. 10 CMV when using SVM hexagon partition I

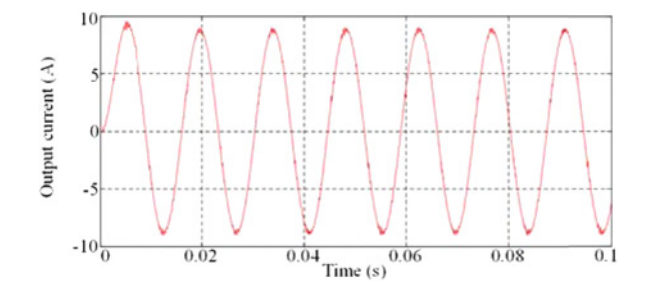


Fig. 11 Output current when using SVM hexagon partition I

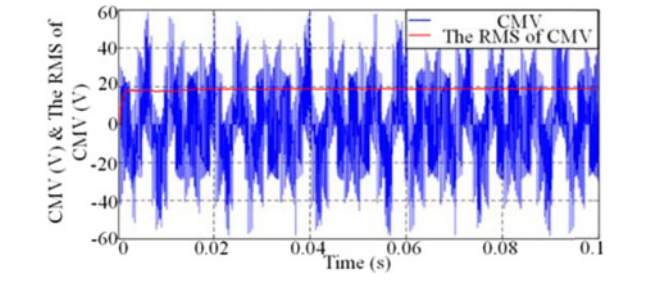


Fig. 12 CMV when using SVM hexagon partition II

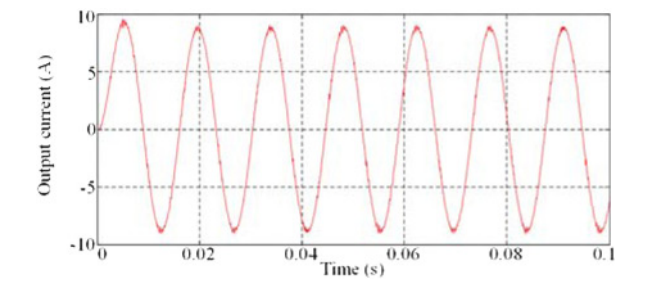


Fig. 13 Output current when using SVM hexagon partition II

SVM hexagon partition II with a modulation index of 60%. Figs. 14 and 15 show the simulation results of the 3LMC using SVM hexagon partition III with a modulation index of 60%. Fig. 16 and 17 show the simulation results of the 3LMC using SVM hexagon partition IV with a modulation index of 60%. Figs. 18–21 present the comparisons of flying capacitor voltage control. After 0.02 s, proposed balance strategy is switched to basic ones under four partitions.

From the simulation results (Figs. 10–21), the following conclusions can be made:

(i) The output currents are both modulated as required sinusoidal waveform.

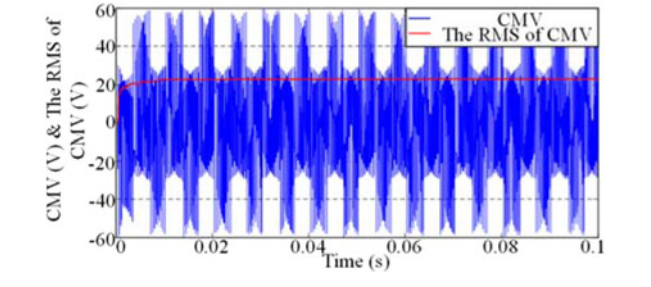


Fig. 14 CMV when using SVM hexagon partition III

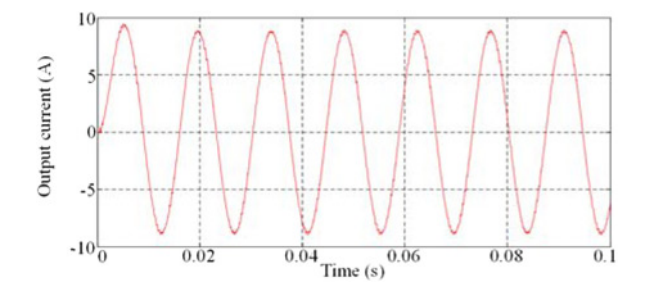


Fig. 15 Output current when using SVM hexagon partition III

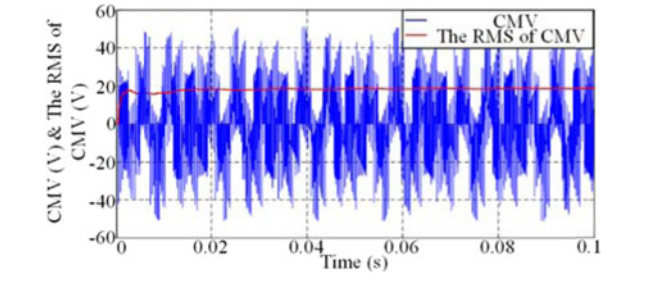


Fig. 16 CMV when using SVM hexagon partition IV

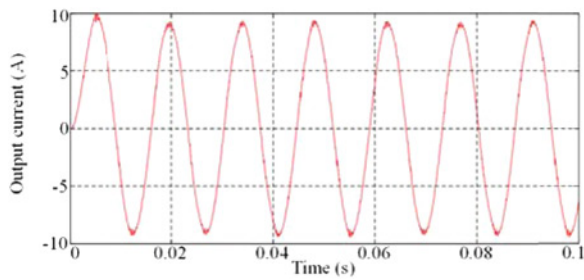


Fig. 17 Output current when using SVM hexagon partition IV

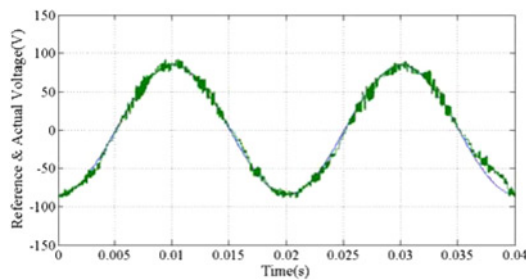


Fig. 18 Capacitor voltage using SVM hexagon partition

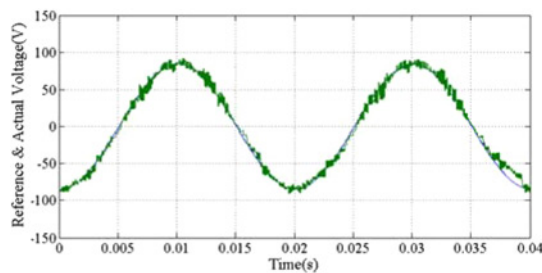


Fig. 19 Capacitor voltage using SVM hexagon partition II

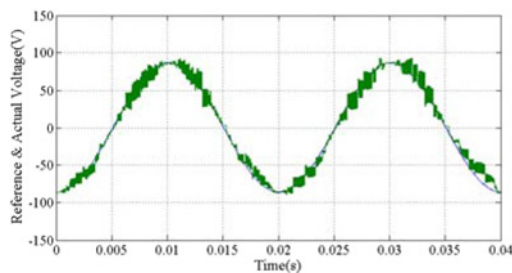


Fig. 20 Capacitor voltage using SVM hexagon partition III

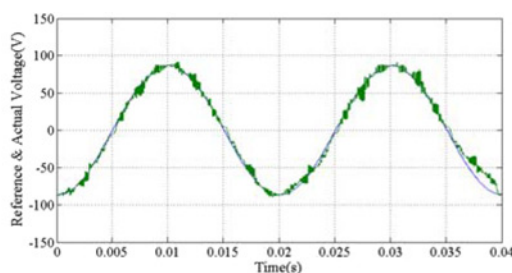


Fig. 21 Capacitor voltage using SVM hexagon partition IV

(ii) In these four ways of SVM hexagon partition, the best partition is the SVM hexagon partition IV. The peak voltage of CMV is 60% of the input phase voltage when the SVM hexagon partition I, II or III been used, the peak voltage of CMV is <50% of the input phase voltage when the SVM hexagon partition IV is used. With high modulation index, compared to other hexagon partition, the SVM hexagon partition makes a further 10% reduction of CMV.

(iii) Flying capacitor voltages can be controlled to follow the reference sinusoidal waveforms; proposed balance can achieve better performance than basic ones, redundant states smooth the voltage distortion compared to its reference value.

(iv) The capacitor voltage shows some distortion compared to its reference value since the high modulation index leads to a lot of use of the full voltage states, which have no contribution on capacitor voltage balance control.

In this case, the SVM is proposed to be implemented in SVM hexagon partition IV and the future experimental works is also based on the modulation in SVM hexagon partition IV.

5 Experimental results

The control of the multi-level matrix converter is implemented using a digital signal processor (DSP) and a field programmable gate array (FPGA) with a series of circuits which allow information such as gate drive signals and measurement signals to be transferred to and from the power PCB boards, plus a protection circuit of main circuit, as shown in Figs. 22 and 23.

The experimental parameters are given in Table 4. The experimental waveforms include the CMV (shown in Fig. 24) and

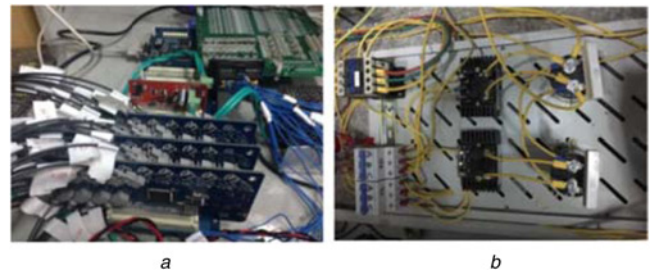


Fig. 22 Control card and protection circuit
a DSP- and FPGA-based PWM card
b Protection circuit of main circuit

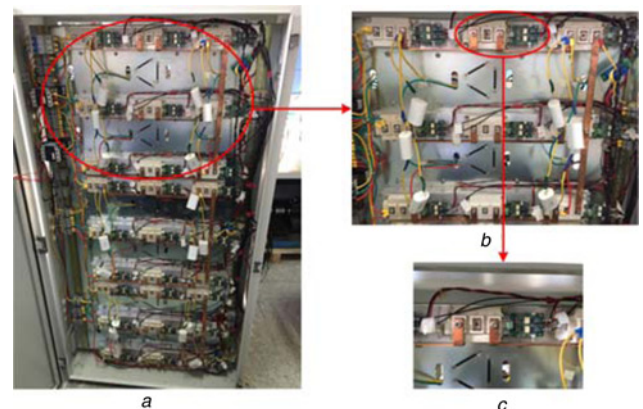
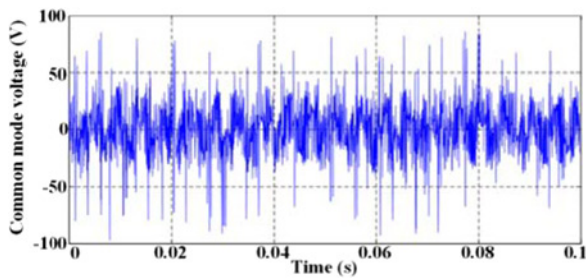
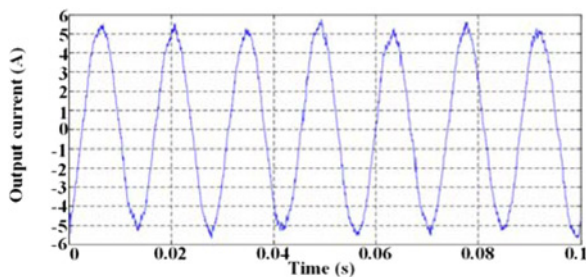
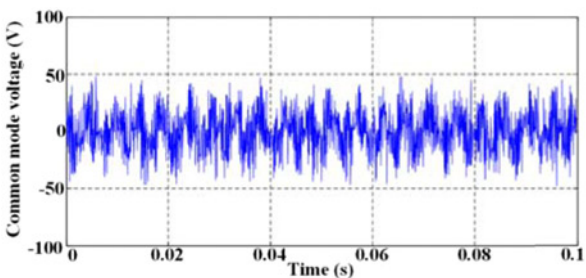
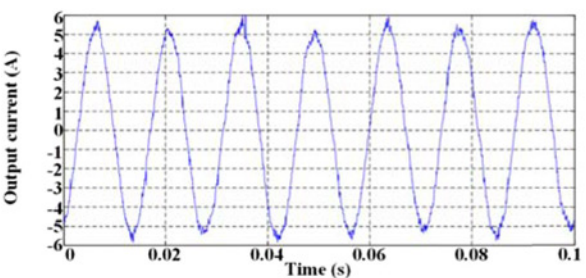


Fig. 23 Experimental prototype
a 3LMC
b Single output of 3LMC
c Bi-directional switch with gate driver

Table 4 Experimental parameters

Parameter	Value
input voltage	100 V (peak)
input frequency	50 Hz
reference output frequency	70 Hz
modulation index	60%
load	10 mH + 5 Ω
flying capacitor	2 μ F
switching frequency	2.5 kHz

**Fig. 24** CMV when using traditional SVM**Fig. 25** Output current when using traditional SVM**Fig. 26** CMV when using SVM hexagon partition IV**Fig. 27** Output current when using SVM hexagon partition IV

output currents (shown in Fig. 25) at 60% modulation index using the traditional SVM [10]; the CMV (shown in Fig. 26) and output currents (shown in Fig. 27) at 60% modulation index using SVM hexagon partition IV and proposed balance strategy. From the experimental results, it can be seen that the output current is controlled and follows the references with the correct amplitude and frequency.

6 Conclusion

This paper presents the theoretical analysis of the SVM algorithm for 3LMC, which consists of the flying capacitor voltage control based on redundant states and the influence of different SVM hexagon partition on CMV. The contribution of this paper includes the comparison of four SVM hexagon partitions, also a novel capacitor balance strategy is proposed to make full use of redundant states and then achieve better balance of AC flying capacitors.

To validate the proposed modulation strategy and the flying capacitor voltage balancing algorithms, Simulation results have been presented. The simulation compares output current and CMV with four SVM hexagon partitions. Novel capacitor voltage control strategy promotes the capacitor balance and the flying capacitor voltages can be controlled to follow the desired AC waveforms. The 3LMC is therefore a feasible topology for high-voltage applications. To validate the theoretical findings, a prototype converter has been built. The experimental results give similar waveforms as the simulation results.

7 Acknowledgments

This paper was funded by National Natural Science Foundation of China (grant nos. 51277108, 51307095, 51577005), Beijing Natural Science Foundation (grant no. 4142026) and Aeronautical Science Foundation of China (grant no. 2015ZC51030).

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