

Research on space-vector modulation and common-mode voltage of four-leg matrix converter

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Published in *The Journal of Engineering*; Received on 10th January 2018; Accepted on 17th January 2018

Abstract: Four-leg matrix converter (MC) is an AC–AC converter which has the ability to drive the unbalanced load. It can be used in many fields such as the ice protection system of More Electrical Aircraft to reach a considerably high power density. Detailed space-vector modulation algorithm and circuit modelling are discussed in this study. Analysis, modelling, and characteristics of common-mode voltage (CMV) are presented. The relationship between the peak value of CMV and circuit parameters is studied and quantitative results are provided. Simulation of a four-leg MC driving system is built and an experimental platform based on DSP/CPLD control system is set up.

1 Introduction

Matrix converter (MC) is a direct AC–AC converter which demands little passive device. Thus it has a remarkable advantage in power density. MC has many characteristics including compact structure, sinusoidal input and output currents, adjustable output frequency and amplitude and unit input power factor [1]. The application prospect of MC is extensive in many fields such as More Electric Aircraft (MEA) and spacecraft.

Mason *et al.* [2] proposed a four-leg MC using space-vector modulation (SVM) method in 2005. In 2010, Crdenas *et al.* [3] give its experimental validation. Four-leg MC based on a traditional three-phase MC has an additional neutral leg connecting to the neutral point of three-phase load. The fourth leg provides a path for zero sequence current to drive the unbalanced load. Ice protection system of MEA is considered as an application situation for four-leg MC in which power density and unbalanced load driving are required.

Many modulation methods of matrix converter with different theories are proposed during these years, including SVM method [4, 5], model predictive control (MPC) [6, 7] and so on. A lot of work has been done for research on compensation for abnormal input voltage [8], common-mode voltage mitigation, loss reduction and efficiency increase [9] and reactive power control [10].

Common-mode voltage (CMV) is another important issue for converters using pulse-width modulation technology. Traditional SVM method of matrix converter generates CMV with the same peak value as input phase voltage amplitude. Several mitigation methods based on SVM method including optimised zero vector [11, 12], stationary vector instead of zero vector [13, 14], rotating vector modulation [15] are proposed. MPC is also applied to control CMV peak value in [16].

This paper mainly studies on the SVM method of a four-leg MC, circuit analysis based on the symmetrical component method and CMV characteristics with the balanced load or the unbalanced load.

2 Four-leg MC

A conventional three-leg MC consists of 3 bridges with 9 bidirectional switches while a four-leg MC consists of 4 bridges and

12 switches. The topology of a four-leg MC driving system can be observed in Fig. 1.

Switching rules of a four-leg MC are shown in (1), where S_{ij} represents the state of the switch between input phase i and output phase j . There are totally $81(3^4)$ valid switching states for a four-leg MC

$$\begin{aligned} S_{Au} + S_{Bu} + S_{Cu} = 1, S_{Av} + S_{Bv} + S_{Cv} = 1 \\ S_{Aw} + S_{Bw} + S_{Cw} = 1, S_{An} + S_{Bn} + S_{Cn} = 1 \end{aligned} \quad (1)$$

3 SVM method

The modulation method in this work is SVM. SVM method for a four-leg MC is firstly introduced in [2]. Compared to traditional SVM method for three-leg MCs, the output voltage space of the new method is extended to 3D while the input current space remains the same

$$\vec{I}_i = \begin{bmatrix} I_{i\alpha} \\ I_{i\beta} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \quad (2)$$

$$\vec{I}_i = \begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2\sqrt{2} & 1/2\sqrt{2} & 1/2\sqrt{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (3)$$

There are 45 switching states used in the SVM method. Three of them are zero vectors and the other 42 states refer to stationary vectors. Rotating vectors are not applied in this SVM method.

Coordinate transformation formulas of input current vector and output voltage vector are given in (2) and (3), respectively. Input current space and output voltage space are presented in Figs. 2 and 3. Input current vector I_i has the same angle with input voltage vector V_i considering input unity power factor. The output voltage vector V_o has three freedom degrees so that the output voltage of each phase is independent. There are 6 basic

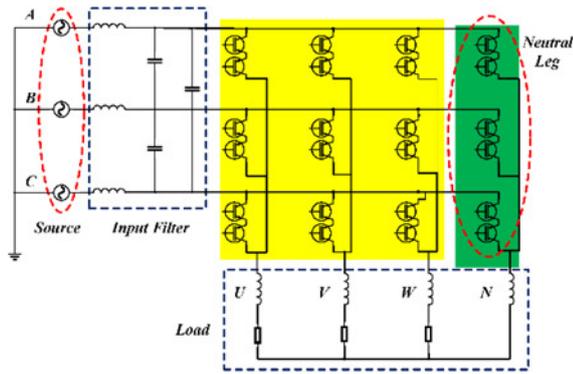


Fig. 1 Four-leg MC driving system

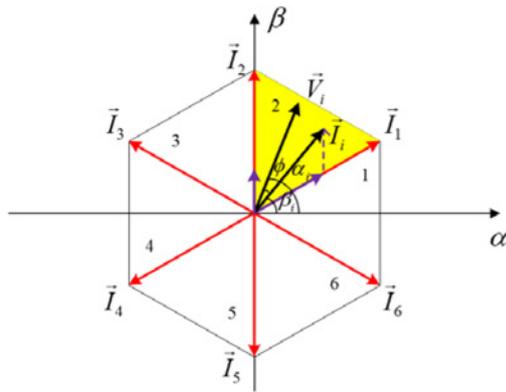


Fig. 2 Input current space

current vectors $I_1 - I_6$ and 14 basic output voltage vectors $V_1 - V_{14}$ for all 45 switching states.

For each tiny section, a certain vector corresponds to several specific basic vectors so that it is convenient to use these close vectors to synthesise the target vector. Input current space is divided into six sectors and specific division is shown in Fig. 2. Output voltage space is divided into six prisms and each prism consists

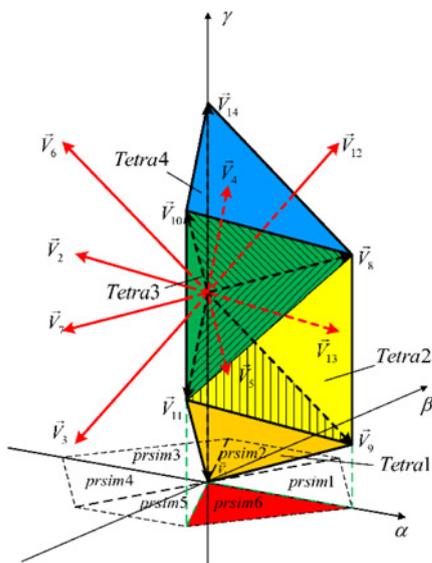


Fig. 3 Output voltage space

of four tetrahedrons shown in Fig. 3. There are totally 24 tetrahedrons or simplified 12 in output voltage space

$$\begin{cases} \delta_{I} = \frac{2 V_o \cos \omega_1 \sin(\pi/6 - \beta_i)}{\sqrt{3} V_i \cos \phi} \\ \delta_{II} = \frac{2 V_o \cos \omega_2 \sin(\pi/6 - \beta_i)}{\sqrt{3} V_i \cos \phi} \\ \delta_{III} = \frac{2 V_o \cos \omega_3 \sin(\pi/6 - \beta_i)}{\sqrt{3} V_i \cos \phi} \\ \delta_{IV} = \frac{2 V_o \cos \omega_1 \sin(\pi/6 + \beta_i)}{\sqrt{3} V_i \cos \phi} \\ \delta_V = \frac{2 V_o \cos \omega_2 \sin(\pi/6 + \beta_i)}{\sqrt{3} V_i \cos \phi} \\ \delta_{VI} = \frac{2 V_o \cos \omega_3 \sin(\pi/6 + \beta_i)}{\sqrt{3} V_i \cos \phi} \end{cases} \quad (4)$$

Input voltage sector is obtained using input voltage angle α_i while β_i refers to the angle of I_i . In addition, the location of output voltage vector can be obtained according to the polarity of load three-phase voltage using the method introduced in [17]. The criterion for each tetrahedron including its basic voltage vectors and polarity of target load line to neutral voltage can be given. Switching states in each period can be decided to combine locations of I_i and V_o . Table 1 gives the procedure of switching states selection taking input sector 2 and output prism 1 tetra 4 for an example. There are six valid switching states referring to stationary vectors in each switching period. Duty cycles $\delta_I - \delta_{VI}$ can be calculated using (4). $v_1 - v_3$ correspond to three basic vectors of each tetrahedron. Consider n_{23} as the normal vector of the plane decided by v_1, v_2 . ω_1 is the angle between V_o and n_{23} . And ω_2, ω_3 are the angles between V_o and n_{23}, n_{12} . $\cos \phi$ is the input power factor which equals 1 in most cases. V_o and V_i are the amplitudes of output voltage vector and input voltage vector, respectively.

There are six main steps of this SVM algorithm. Its flow diagram is presented in Fig. 4. The first step is to read data of input voltage obtained from voltage sensors in the practical system. Current values are also needed for commutation based on detection of current directions. As unbalanced load changes the voltage of neutral point, the calculation of output voltage of four-leg MCs needs circuit parameters and is more complicated than that of traditional MCs. An equivalent model and symmetrical component theory are used to deal with the unbalanced load

$$\begin{cases} v_u = V_u \cos \omega t \\ v_v = V_v \cos(\omega t - 2\pi/3) \\ v_w = V_w \cos(\omega t + 2\pi/3) \end{cases} \begin{cases} i_u = I_u \cos \omega t \\ i_v = I_v \cos(\omega t - 2\pi/3) \\ i_w = I_w \cos(\omega t + 2\pi/3) \end{cases} \quad (5)$$

Each output leg is equivalent to a similarly ideal voltage source for a load. The average equivalent model of four-leg MC which is shown in Fig. 5 can be obtained. $V_u - V_n$ are equivalent average voltages of four output legs in a steady state. u, v, w, n are the four leg output points and neutral point is set as n' . $i_u - i_n$ are the output currents. $L_u - L_n$ are the output inductors and $R_u - R_n$ are the load resistors. Consider $V_{un'}, V_{vn'}, V_{wn'}$ as the output three-phase voltages

Table 1 Selection of switching states

	Sector 2	Prism 1 Tetra 4
switching states	$\pm 3, \pm 6, \pm 9, \pm 12, \pm 15,$ $\pm 18, \pm 21, \pm 2, \pm 5, \pm 8,$ $\pm 11, \pm 14, \pm 17, \pm 20$	$\pm 1, \pm 2, \pm 3, \pm 10, \pm 11,$ $\pm 12, \pm 19, \pm 20, \pm 21$
common states	$\pm 2, \pm 3, \pm 11, \pm 12, \pm 20, \pm 21$	
final states	$\pm 2, -3, \pm 11, -12, \pm 20, -21$	

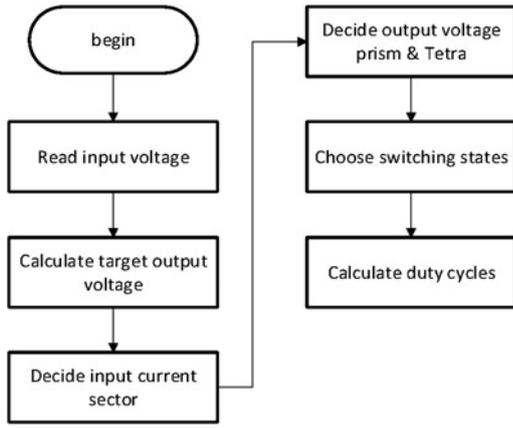


Fig. 4 SVM algorithm diagram

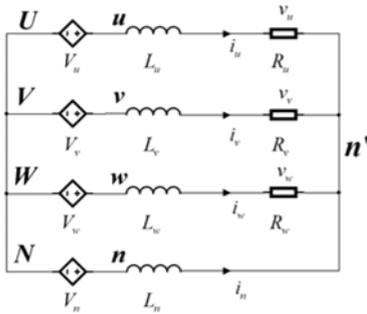


Fig. 5 Steady-state average equivalent model of four-leg MC

which are balanced or unbalanced. Three-phase load voltages are v_u, v_v, v_w and three-phase load currents are i_u, i_v, i_w .

The load current is a target value for four-leg MC so that load model can be regarded as a current source. Three-phase voltage and three-phase current are presented in (5). Three sequence components are obtained in (6), respectively, using the symmetrical component method. Similarly, sequence components of load

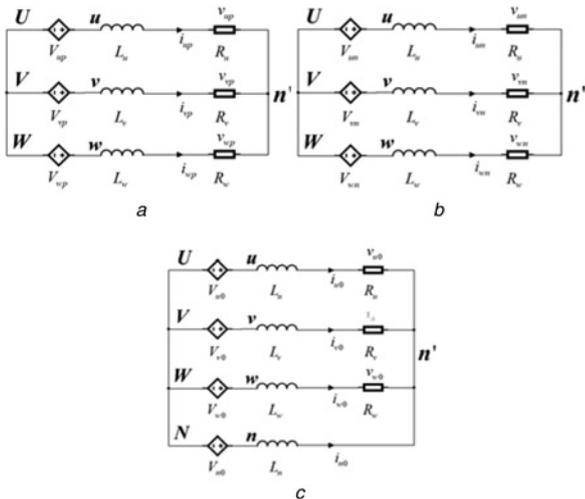


Fig. 6 Sequence equivalent circuit

- a Positive sequence
- b Negative sequence
- c Zero sequence

voltages $v_{up}, v_{vp}, v_{wp}, v_{un}, v_{vn}, v_{wn}, v_{u0}, v_{v0}, v_{w0}$ can be obtained and these expressions are omitted for conciseness

$$\begin{aligned} \mathbf{i}_p &= \mathbf{M} \cdot \mathbf{i}, \mathbf{i}_p = [i_{up} \ i_{vp} \ i_{wp}]^T \\ \mathbf{i}_n &= \mathbf{M}^T \cdot \mathbf{i}, \mathbf{i}_n = [i_{un} \ i_{vn} \ i_{wn}]^T \\ \mathbf{i}_o &= \mathbf{I} \cdot \mathbf{i}, \mathbf{i}_o = [i_{u0} \ i_{v0} \ i_{w0}]^T \end{aligned} \quad (6)$$

$$\mathbf{M} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}, \quad \mathbf{I} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$$

Positive, negative and zero sequence equivalent circuits are shown in Figs. 6a–c, respectively. Voltage equations of each sequence circuit are listed in (7) based on KVL and (5), (6). i_{n0} in zero sequence equivalent circuit equals $-(i_{u0} + i_{v0} + i_{w0})$. The expression of target leg output voltage can be obtained combining (5)–(7) and it is shown in (8). It is convenient to calculate target output voltage under any balanced or unbalanced load condition using this result

$$\begin{aligned} \begin{bmatrix} V_{up} \\ V_{vp} \\ V_{wp} \end{bmatrix} &= \begin{bmatrix} L_u \frac{di_{up}}{dt} + v_{up} \\ L_v \frac{di_{vp}}{dt} + v_{vp} \\ L_w \frac{di_{wp}}{dt} + v_{wp} \end{bmatrix}, \quad \begin{bmatrix} V_{un} \\ V_{vn} \\ V_{wn} \end{bmatrix} = \begin{bmatrix} L_u \frac{di_{un}}{dt} + v_{un} \\ L_v \frac{di_{vn}}{dt} + v_{vn} \\ L_w \frac{di_{wn}}{dt} + v_{wn} \end{bmatrix} \\ \begin{bmatrix} V_{u0} \\ V_{v0} \\ V_{w0} \end{bmatrix} &= \begin{bmatrix} L_u \frac{di_{u0}}{dt} + v_{u0} + L_n \frac{di_{n0}}{dt} \\ L_v \frac{di_{v0}}{dt} + v_{v0} + L_n \frac{di_{n0}}{dt} \\ L_w \frac{di_{w0}}{dt} + v_{w0} + L_n \frac{di_{n0}}{dt} \end{bmatrix} \end{aligned} \quad (7)$$

$$\begin{aligned} V_u &= v_u \cos \omega t - \omega L_u I_u \sin \omega t \\ &\quad - \omega L_n \left[I_u \sin \omega t + I_v \sin \left(\omega t - \frac{2}{3} \pi \right) + I_w \sin \left(\omega t + \frac{2}{3} \pi \right) \right] \\ V_v &= v_v \cos \left(\omega t - \frac{2}{3} \pi \right) - \omega L_u I_u \sin \left(\omega t - \frac{2}{3} \pi \right) \\ &\quad - \omega L_n \left[I_u \sin \omega t + I_v \sin \left(\omega t - \frac{2}{3} \pi \right) + I_w \sin \left(\omega t + \frac{2}{3} \pi \right) \right] \\ V_w &= v_w \cos \left(\omega t + \frac{2}{3} \pi \right) - \omega L_u I_u \sin \left(\omega t + \frac{2}{3} \pi \right) \\ &\quad - \omega L_n \left[I_u \sin \omega t + I_v \sin \left(\omega t - \frac{2}{3} \pi \right) + I_w \sin \left(\omega t + \frac{2}{3} \pi \right) \right] \end{aligned} \quad (8)$$

The third step is to decide input voltage sector after the step of calculating target output voltage. The angle and sector of input voltage vector are the same as those of input current vector considering unit power factor so that this sector can be decided using data of input voltage. The next step of SVM method is to decide output voltage prism and tetrahedron. It can be realised referring to the angle $\phi_{\alpha\beta}$ of output voltage in a α – β plane. Table 1 gives a general procedure for choosing switching states. Finally, duty cycles of each switch state can be obtained using (4).

4 CMV analysis

CMV of four-leg MC is the voltage of neutral point. Analysis of CMV is provided detailed in [18]. Some basic analysis is repeated

and new results of CMV are presented in the following. Observing topology of the whole electrical driving system shown in Fig. 1, the circuit equation can be obtained. Equations in (9) show basic relations among load voltages and currents according to KVL

$$\begin{cases} v_a = L \frac{di_a}{dt} + v_{an} + v_n, v_b = L \frac{di_b}{dt} + v_{bn} + v_n \\ v_c = L \frac{di_c}{dt} + v_{cn} + v_n, v_f = L \frac{di_n}{dt} + v_n \\ i_a + i_b + i_c + i_n = 0 \end{cases} \quad (9)$$

In (9), v_a-v_f are leg output voltages, $v_{an}-v_{cn}$ are load phase voltages, are load currents and is neutral point voltage. L is output inductor and L_n is the neutral inductor. The other current condition can be obtained due to KCL which is shown in (9), too. The expression of v_n is derived using the above equations

$$v_n = \frac{k(v_a + v_b + v_c) + v_f - k(v_{an} + v_{bn} + v_{cn})}{3k + 1} \quad (10)$$

Parameter derived from (10) $k=L_n/L$. CMV of four-leg MC which is v_n in (10) relates to leg output voltages, load phase voltages, and inductor factor k . It is necessary to discuss this problem with balanced or unbalanced load separately.

4.1 Balanced load

A strict voltage restriction arises with balanced load voltage which is that the sum of load phase voltages is zero. According to this condition, the expression of CMV can be simplified as (11) in which the value of CMV only relates to k and leg output voltage. Time-domain analytical expressions of input voltage are shown in (12). Four groups of switching states shown in Table 2 are divided combining (11) and (12). M, N refers to A, B or C while $M \neq N$

$$v_n = \frac{k(v_a + v_b + v_c) + v_f}{3k + 1} \quad (11)$$

$$\begin{cases} v_A = U_m \cos \omega t \\ v_B = U_m \cos (\omega t - 120^\circ) \\ v_C = U_m \cos (\omega t + 120^\circ) \end{cases} \quad (12)$$

Phasor method is applied to calculate the amplitude of CMV as CMV value is an AC item. The simple calculation procedure is omitted. Amplitudes of input voltages are standardised in all calculations. Results of CMV amplitudes in Table 3 indicate that CMV amplitude in each group is the same. It only relates to the inductor factor k ignoring the fluctuation of the input voltage. Curves between CMV amplitude and k of four groups can be observed in Fig. 7.

Table 2 Groups of switching states.

Group	Switching states	CMV
1	ZA, ZB, ZC	$V_n = V_M$
2	$\pm 19, \pm 20, \pm 21$	$v_n = \frac{3kv_M + v_N}{3k + 1}$
3	$\pm 1, \pm 2, \pm 3, \pm 4, \pm 5,$ $\pm 6, \pm 7, \pm 8, \pm 9,$	$v_n = \frac{(2k + 1)v_M + kv_N}{3k + 1}$
4	$\pm 10, \pm 11, \pm 12, \pm 13, \pm 14,$ $\pm 15, \pm 16, \pm 17, \pm 18$	$v_n = \frac{2kv_M + (k + 1)v_N}{3k + 1}$

Table 3 Simulation parameters

Parameter	Symbol	Value
input phase voltage (rms)	U_s	220 V
input frequency	f_i	50 Hz
input filter inductor	L_f	1 mH
input filter capacitor	C_f	33 μ F
input damping resistor	R_f	20 Ω
load inductor	L	5 mH
load resistor	R	5 Ω
neutral leg inductor	L_n	5 mH
output frequency	f_o	70 Hz
switching frequency	f_s	20 kHz

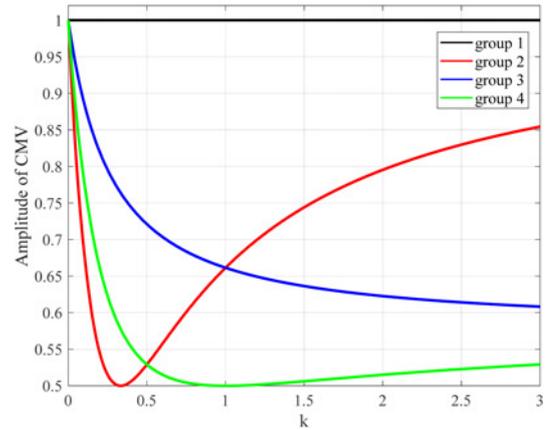


Fig. 7 Curve of amplitude of CMV and k in balanced load

4.2 Unbalanced load

Influence factors and calculation results with unbalanced load are much complicated than those with a balanced load. Three situations of unbalanced load are discussed in [18]. However, only the unbalanced condition of the asymmetric voltage drop of two phases is necessary to analyse as a general situation covering all possible cases actually.

As the sum of load phase voltages cannot be neglected, take m_a, m_b, m_c as the modulation factor of each phase and take m as the whole modulation factor which is no larger than 0.866. θ is the lag angle caused by load inductors. v_{unbal} and v_{bal} are introduced to describe balanced and unbalanced parts in CMV. The expression of v_n with unbalanced load is presented in (14)

$$\begin{cases} v_{an} = m \cdot m_a \cdot v_A \cdot e^{j\theta} \\ v_{bn} = m \cdot m_b \cdot v_B \cdot e^{j\theta} \\ v_{cn} = m \cdot m_c \cdot v_C \cdot e^{j\theta} \end{cases} \quad (13)$$

$$\begin{cases} v_{unbal} = v_{an} + v_{bn} + v_{cn} \\ v_{bal} = k(v_a + v_b + v_c) + v_f, v_n = \frac{v_{bal} - kv_{unbal}}{3k + 1} \end{cases} \quad (14)$$

$$\begin{cases} U_{unbal} = m_{bc} \angle \gamma \\ m_{bc} = m \sqrt{m_b^2 + m_c^2 - m_b m_c - m_b - m_c + 1} \end{cases} \quad (15)$$

$$A_{CMV} = \frac{|U_{bal}| + k|U_{unbal}|}{3k + 1} \quad (16)$$

v_{unbal} and v_{bal} are both alternative voltages but differ in the frequency. v_n is possible to reach its peak value when v_{bal} and v_{unbal} have opposite phases. Nevertheless, this restriction reaching maximum value is too strict to meet in a real system. Generally, the sum of amplitudes of v_{bal} and kv_{unbal} dividing $3k + 1$ gives an upper bound of CMV. After calculating in phasor method, the

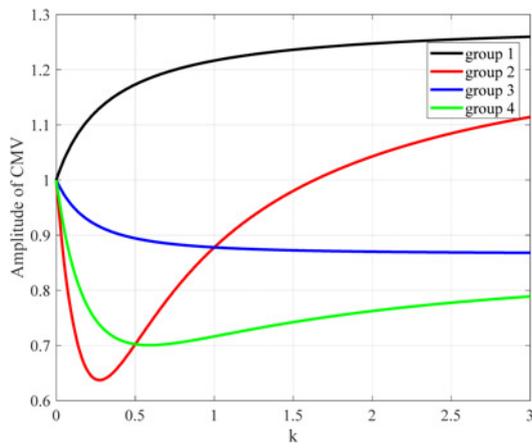


Fig. 8 Curve of amplitude of CMV and k in unbalanced load

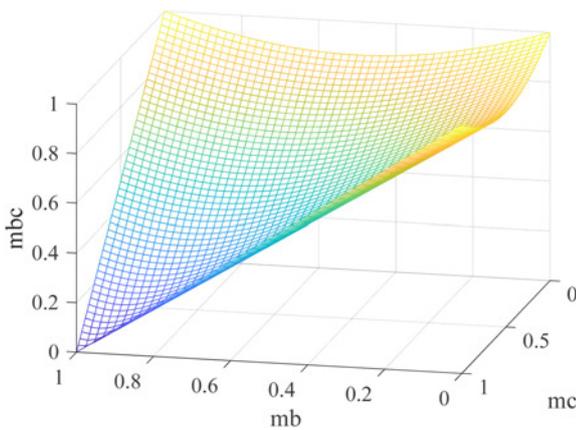


Fig. 9 Surface of m_{bc}

amplitude of v_{unbal} is shown in (15). The amplitude of v_n is obtained combining v_{bal} expression of four groups in Table 2 together with v_{unbal} . Set A_{CMV} as the amplitude of CMV which means the possible peak value and its expression is shown in (16). In fact, $k \cdot m_{bc}$ represents the positive correlation of unbalanced load voltage with neutral point voltage.

Specially, study how four curves in Fig. 7 change in condition of $m_b = 0$ and $m_c = 1$ which is single-phase voltage drop. New results are shown in Fig. 8.

Comparing Figs. 7 and 8, four curves all rises under the effect of v_{unbal} . Cross points of groups 2, 3 and groups 2, 4 still have same values of k which are 0.5 and 1.0, respectively. Groups 2 and 3 reach their minimum values with different k compared to balanced ones. Generally, the variation tendency of four curves does not change while every curve rises with the increase of m_{bc} .

According to (15), the surface of m_{bc} can be obtained which is presented in Fig. 9. Observing this surface, m_{bc} reaches its maximum when m_b or m_c equals zero. The surface above gives a visual quantified description of the unbalanced part in different conditions. The value of m_{bc} can be obtained with every possible value of m_b and m_c so that the rising level of A_{CMV} can be estimated.

5 Simulation results

This paper uses MATLAB/Simulink to build a simulation circuit of a four-leg MC driving system with the same topology in Fig. 1. RLC damping low-pass filter is used as an input filter. Circuit parameters are listed in Table 3. In addition, the SVM algorithm in this paper uses optimised zero vector method to reduce CMV.

5.1 Balanced load

Simulation system takes $R = 5 \Omega$ and $L = 5 \text{ mH}$ as balanced three-phase load. The modulation factor of the whole load is $m = 0.8$ while three-phase modulation factors all equal to 1, $m_a = m_b = m_c = 1$.

The three-phase input current is balanced as expected. Fig. 10 presents the wave of balanced output three-phase currents. Cyan curve is the current of the neutral leg.

5.2 Unbalanced load

The unbalanced load is realised using unbalanced target output voltage with balanced load parameters including resistor R and inductor L . Modulation of three-phase load is $m_a = 1$, $m_b = 0.5$, $m_c = 0.8$ while the $m = 0.8$. Simulation wave of the input current of phase A is shown in Fig. 11. Observing simulation result, input current with unbalanced load has a high THD around 23% due to load power fluctuation. Fig. 12 shows the wave of load current. The amplitude of phase a current equals 50 A while the

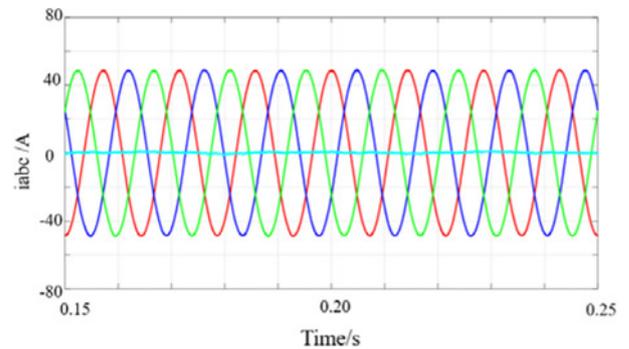


Fig. 10 Simulation waves of output currents with balanced load

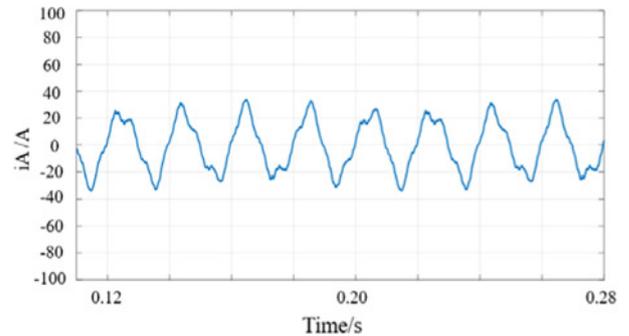


Fig. 11 Simulation wave of a phase input current with unbalanced load

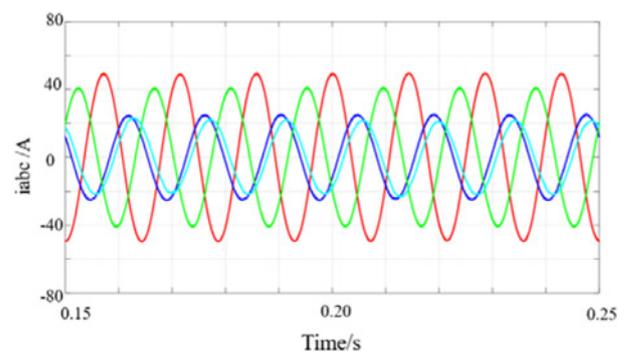


Fig. 12 Simulation waves of output currents with unbalanced load

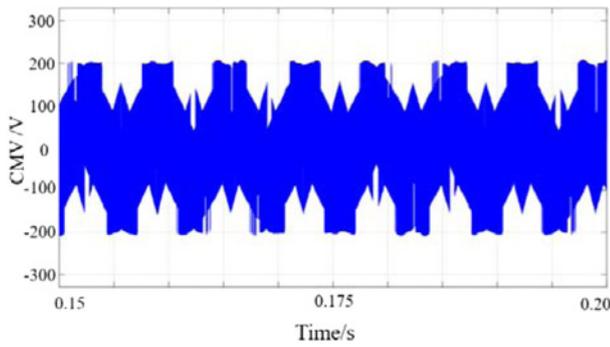


Fig. 13 Simulation wave of CMV with balanced load

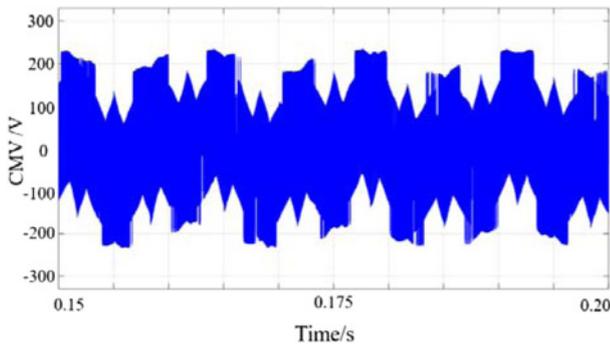


Fig. 14 Simulation wave of CMV with unbalanced load

amplitude of currents b and c is 25 A, 40 A, respectively. This result meets the target value and proves the correctness of SVM method. Comparing Figs. 12 and 13, load currents have much better quality and much less THD than input currents.

5.3 Common-mode voltage

Fig. 13 shows the simulation wave of CMV with a balanced load using optimised zero vector method in the condition of Section 5.1. Fig. 14 shows the wave of CMV with an unbalanced load in the condition of Section 5.2. CMV in unbalanced condition has a larger peak value. Standardised peak values of groups 1, 3, 4 are 0.5872, 0.7486, 0.5872 according to (15) while switching states of group 2 are not used. The theoretical calculation result of CMV peak value with unbalanced load is 233 V which matches simulation results.

6 Experimental results

Experimental platform based on TMS320F28335 is set up and commutation is realised by CPLD. Fig. 15 shows the picture of the experimental system in practice. Part of experimental parameters is shown in Table 4.

Fig. 16 shows the experimental results of the input voltage and current with a balanced load in which modulation factor m is 0.8. The yellow wave in Fig. 16 is input voltage of phase A and the green one is input current. Unit input power factor is realised in this driving system. Output current waves with balanced load are shown in Fig. 17. Three-phase load current is balanced and neutral current in yellow is nearly zero.

Waveforms of unbalanced load currents are presented in Fig. 18 while $m_a=0.5$, $m_b=m_c=1$. The current of phase a has a half amplitude of current of b or c . Neutral current is similar to a phase current but some difference still remains because of parameter errors and open-loop control.

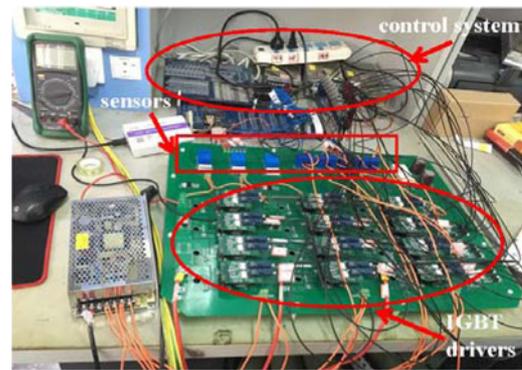


Fig. 15 Picture of experimental device

Table 4 Experimental parameters

Parameter	Symbol	Value
input phase voltage (rms)	U_s	40 V
input frequency	f_i	50 Hz
input filter inductor	L_f	1 mH
input filter capacitor	C_f	50 μ F
input damping resistor	R_f	30 Ω
load inductor	L	10 mH
load resistor	R	5 Ω
neutral leg inductor	L_n	10 mH
output frequency	f_o	50 Hz
switching frequency	f_s	2 kHz

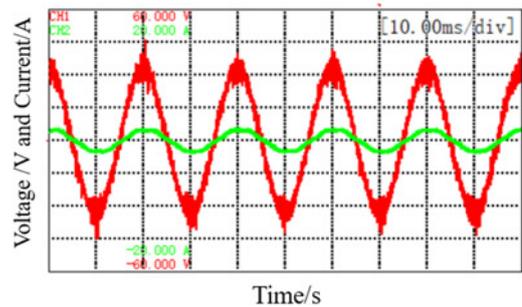


Fig. 16 Waveforms of input voltage and current with balanced load

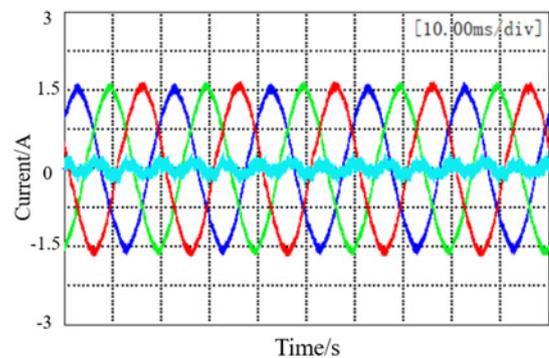


Fig. 17 Waveforms of load currents with balanced load

Traditional SVM method is applied to compare with optimised zero vector method. Fig. 19 shows the CMV in the traditional method with full zero vectors while Fig. 20 gives the result of

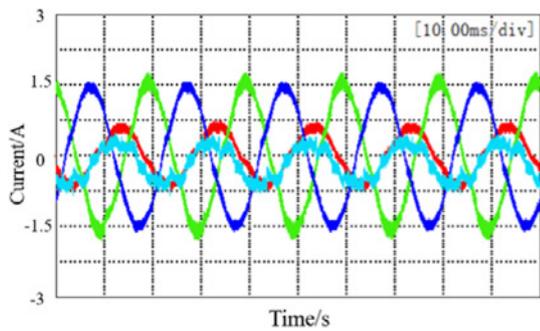


Fig. 18 Waveforms of load currents with unbalanced load

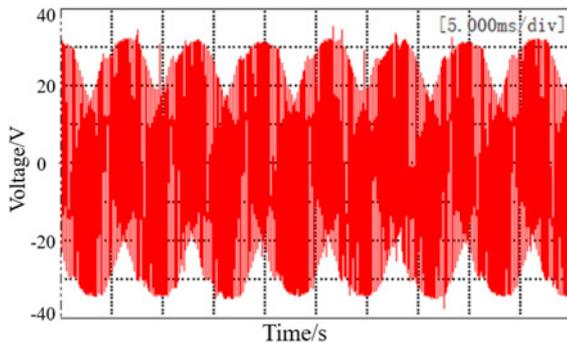


Fig. 19 Waveform of CMV using traditional method

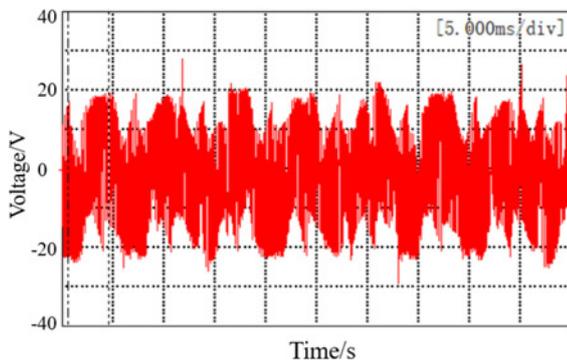


Fig. 20 Waveform of CMV using optimised zero vector method

optimised zero vector method. Combining these two waves above, the amplitude of CMV in Fig. 19 is 32 V and that in Fig. 20 is 22 V. Optimised zero vector method mitigates 31% of CMV peak value.

7 Conclusions

After studying on SVM method and CMV of a four-leg MC, this paper generates several conclusions. SVM method is applied to drive a four-leg MC with both balanced and unbalanced loads. Circuit modelling and analysis is discussed using the symmetrical component method. CMV peak value relates to three main parameters including inductor factor k , input voltage and the sum of load phase voltages. Specific characteristics of CMV with unbalanced load are presented and a general method to estimate CMV peak value is proposed. Optimised zero vector method is used to

reduce the CMV peak value. In general, the amplitude of CMV rises with the increase of the degree of load unbalance. Results of simulation and experiment are presented to verify theoretical results.

8 References

- [1] Wheeler P.W., Rodriguez J., Clare J.C., *ET AL.*: 'Matrix converters: a technology review', *IEEE Trans. Ind. Electron.*, 2002, **49**, (2), pp. 276–288
- [2] Mason N.J., Wheeler P.W., Clare J.C.: 'Space vector modulation for a 4-leg matrix converter'. 2005 IEEE 36th Power Electronics Specialists Conf., June 2005, pp. 31–38
- [3] Crdenas R., Pea R., Wheeler P., *ET AL.*: 'Experimental validation of a space vector modulation method for a 4-leg matrix converter'. 5th IET Int. Conf. Power Electronics, Machines and Drives (PEMD 2010), April 2010, pp. 1–6
- [4] Huber L., Borojevic D., Burany N.: 'Voltage space vector based pwm control of forced commutated cycloconverters'. 15th Annual Conf. of IEEE Industrial Electronics Society, November 1989, vol. 1, pp. 106–111
- [5] Casadei D., Serra G., Tani A., *ET AL.*: 'Matrix converter modulation strategies: a new general approach based on space-vector representation of the switch state', *IEEE Trans. Ind. Electron.*, 2002, **49**, (2), pp. 370–381
- [6] Formentini A., Trentin A., Marchesoni M., *ET AL.*: 'Speed finite control set model predictive control of a pmsm fed by matrix converter', *IEEE Trans. Ind. Electron.*, 2015, **62**, (11), pp. 6786–6796
- [7] Rivera M., Wilson A., Rojas C.A., *ET AL.*: 'A comparative assessment of model predictive current control and space vector modulation in a direct matrix converter', *IEEE Trans. Ind. Electron.*, 2013, **60**, (2), pp. 578–588
- [8] Mei Y., Sun K., Zhou D., *ET AL.*: 'Analysis and compensation of matrix converter operation under abnormal input voltage conditions'. The 4th Int. Power Electronics and Motion Control Conf. 2004, IPESC 2004, August 2004, vol. 3, pp. 1311–1315
- [9] Nagafuchi S., Abe T., Higuchi T.: 'Loss evaluation for arcp matrix converter'. 2013 IEEE 10th Int. Conf. Power Electronics and Drive Systems (PEDS), April 2013, pp. 608–612
- [10] Schafmeister F., Kolar J.W.: 'Novel modulation schemes for conventional and sparse matrix converters facilitating reactive power transfer independent of active power flow'. 2004 IEEE 35th Annual Power Electronics Specialists Conf. (IEEE Cat. No.04CH37551), 2004, vol. 4, pp. 2917–2923
- [11] Cha H.J., Enjeti P.N.: 'An approach to reduce common mode voltage in matrix converter', *IEEE Trans. Ind. Appl.*, 2003, **39**, (4), pp. 1151–1159
- [12] Kang J.K., Kume T., Hara H., *ET AL.*: 'Common mode voltage characteristics of matrix converter-driven ac machines'. Fourtieth IAS Annual Meeting. Conf. Record of the 2005 Industry Applications Conf. 2005, October 2005, vol. 4, pp. 2382–2387
- [13] Chen R., Su M., Sun Y., *ET AL.*: 'A novel commutation strategy to suppress the common mode voltage for the matrix converter'. 2009 Asia-Pacific Power and Energy Engineering Conf., March 2009, pp. 1–4
- [14] Shi T., Huang Q., Yan Y., *ET AL.*: 'Suppression of common mode voltage for matrix converter based on improved double line voltage synthesis strategy', *IET Power Electron.*, 2014, **7**, (6), pp. 1384–1395
- [15] Nguyen H.N., Lee H.H.: 'An enhanced svm method to drive matrix converters for zero common-mode voltage', *IEEE Trans. Power Electron.*, 2015, **30**, (4), pp. 1788–1792
- [16] Vargas R., Ammann U., Rodriguez J., *ET AL.*: 'Predictive strategy to control common-mode voltage in loads fed by matrix converters', *IEEE Trans. Ind. Electron.*, 2008, **55**, (12), pp. 4372–4380
- [17] Zhang R., Prasad V.H., Borojevich D., *ET AL.*: 'Three-dimensional space vector modulation for four-leg voltage-source converters', *IEEE Trans. Power Electron.*, 2002, **17**, (3), pp. 314–326
- [18] Xu H., Xu L.: 'Analysis of common mode voltage for a four-leg matrix converter'. 2017 IEEE Transportation Electrification Conf. and Expo, Asia-Pacific (ITEC Asia-Pacific), Harbin, People's Republic of China, August 2017