

# Isolated soft-switched boost DC–DC converter with low-voltage stress and high step-up ratio

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Published in *The Journal of Engineering*; Received on 21st January 2018; Accepted on 5th March 2018

**Abstract:** This study presents a novel soft-switched isolated boost converter which can provide a high-step-up ratio and high efficiency with low-voltage stress for portable application as well as a photovoltaic-assisted converter system. A lossless active clamp snubber circuit helps in achieving zero-voltage-switching turn-off and zero-current-switching (ZCS) turn-on of the main switch and ZCS turn-off of diodes that reduce switching losses. An auxiliary switch with an energy recovery circuit helps to increase power conversion efficiency and reduces switching stress across the main switch. The proposed idea is simulation through computer-assisted software PSIM 9.1.1 and validated experimentally through a designed prototype 250 W direct current (DC)–DC converter.

## 1 Introduction

Isolated single stage direct current (DC)–DC converters with a high step-up ratio are widely used for portable fuel cells, vehicular inverters, and modulated integrated photovoltaic systems because of high-power density, low weight, and cost [1–5]. A voltage source with a series connected inductor based isolated step-up converter is suitable because of low current ripples. Active clamp and passive clamp have their corresponding disadvantages like power loss in residual current device snubber and active clamp with four switch topologies suffer from achieving high efficiency and cost [6–14]. The different topologies of the isolated converter, i.e. fly-back converters, partial-resonant buck–boost converters, and non-isolated dc–dc converters with soft switching had both step-down and step-up ability [15–19]. Two small alternating current (AC) capacitors are required on both sides of the transformer to realise soft switching [4]. They also provide passive clamping. However, these types of converters suffer from bigger transformer size. Quasi-resonant converters and zero voltage switching (ZVS) occur at both turn-on and turn-off of all the semiconductor devices but restricted to the load level and voltage values [20]. Similarly, fly back converter isolation can be realised by employing an air-gapped high-frequency transformer. The parallel capacitor helps in realising zero-voltage turn-on and turn-off for converter's switches [5, 6]. However, these types of converters suffer from a limited duty ratio variation. Z-source-based [21, 22] topology becomes popular because of the low-voltage stress of switches and it can boost the input voltage to the desired levels with low-duty ratios. The coupled inductor used in these types of converters stores leakage energy. By changing switching pattern-stored energy can be recovered. Low-voltage MOSFETs can be used as switching stress is less as well as the resistance of the switch is less and hence conduction loss is less while in the case of hard switching the switching losses are high. The active clamped converter has three basic topologies such as push-pull, half-bridge, and full-bridge converters. However, the push-pull and half bridge structures have better performance in high current and low-voltage applications. Zero-voltage switching (ZVS) turn-on of switches is easy to achieve as discussed in [23–25]. Transformer leakage inductance creates voltage spikes, which can be eliminated by a lossless clamping circuit. However, due to high switching count on these

converters, switching losses are increased [7–9] they are less efficient in low-power applications.

A single-switch isolated DC–DC converter with soft switching has advantages like smaller transformer size and does not require the bulky output inductor. Due to less switch count, efficiency is improved. In this study, an isolated soft-switched boost converter is proposed. The advantages of the proposed converter are ZVS turn-off and zero current switching (ZCS) turn-on of the main switch. ZCS turn-off of secondary diodes leads to a low-voltage spike. Less volume of the transformer is required because of low magnetising current. Current ripple is less due to continuous conduction mode (CCM) operation. A low-rated lossless snubber circuit is connected across the switch. These features help to achieve high efficiency and low cost for step-up applications. Furthermore, an auxiliary energy recovery circuit enhances conversion efficiency.

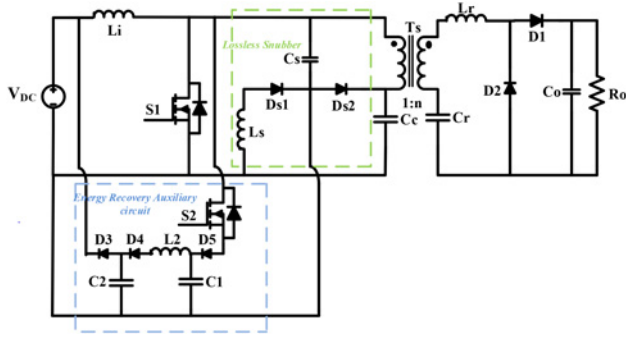
## 2 Proposed converter with energy recovery circuit

The proposed isolated resonant DC–DC converter is shown in Fig. 1. A lossless snubber circuit, which consists of a series capacitor ( $C_s$ ), series inductance ( $L_s$ ), and diodes  $D_{s1}$  and  $D_{s2}$ , are connected to the primary side of the transformer. It helps to achieve soft switching of switch  $S_1$ , i.e. ZCS turn-on and ZVS turn-off, where  $S_1$  and  $S_2$  are the main switch and auxiliary switch, respectively. It also helps in reducing voltage spike in the main switch due to leakage inductances.  $C_c$  is the clamp capacitor. In the primary side, another resonating branch is formed with  $C_1$ ,  $L_2$ ,  $D_4$ , and  $C_2$ , which helps in energy recovery from  $C_s$ . The transformation ratio of the switching transformer is  $n$  as shown in Fig. 1.

In the secondary side, a resonating tank consists of the leakage inductance of the transformer ( $L_r$ ) and resonating capacitance ( $C_r$ ) which helps in restoring leakage inductance energy of the switching transformer as well as achieving ZCS for the diodes  $D_1$  and  $D_2$  during turn-off commutation. The resonant frequency ( $f_{r1}$ ), angular frequency  $\omega_{r1} = 2\pi f_{r1}$ , and time period ( $T_{r1}$ ) of the secondary side main.

The resonant tank is given by  $f_{r1} = (1/2\pi\sqrt{L_r C_r})$  and  $T_{r1} = (1/f_{r1})$ .

There are three basic cases of operations illustrated for the proposed converter, i.e. *Case 1*: operation at below resonance, *Case 2*: operation at above resonance, and *Case 3*: operation at critical resonance. Below resonance operation is considered as



**Fig. 1** Proposed isolated boost converter with energy recovery circuit

switch turn-off current and  $di/dt$  of the diode is less. The below-resonance operation occurred when  $DT_s > 0.5T_{r1}$ , where  $T_s$  and  $D$  are the switching period and duty ratio of the main switch, respectively. In general, ZVS turn-on and ZCS turn-off have taken place in the flyback type isolated converters where magnetising energy is stored on time and transferred to secondary during off time [7, 11, 17]. However, in this proposed converter, boost type isolated topology is considered where energy is transferred to secondary during the on-switching period and hence ZCS turn-on and ZVS turn-off of the main switch are investigated. The waveforms of voltages and currents for different components in the case of below resonance are shown in Fig. 2a, where  $v_{cs}$ ,  $v_{cr}$ , and  $i_{Lr}$  are the instantaneous values of snubber capacitor voltage, secondary resonating capacitor voltage, and leakage inductor current, respectively. The currents through diodes  $D_1$  and  $D_2$  are denoted as  $i_{D1}$  and  $i_{D2}$ , respectively. Fig. 2b shows the waveforms of voltages and currents considering the effect of using an auxiliary circuit, where  $V_{s1}$  and  $i_{s1}$  are the voltage across and current through the main switch, respectively.  $i_s$  and  $i_L$  are the source current and main inductor current, respectively. It can be observed from the waveforms that turn-on commutation is achieved as ZCS while turn-off commutation takes place as ZVS for the main switch  $S_1$ . Furthermore, considering one switching period ( $T_s$ ) of the proposed converter for below resonance operation are illustrated and possible modes are explained in Figs. 3a–c.

**Mode 1 ( $t_0 - t_1$ ):** This mode starts when  $S_1$  is on and second resonant tank  $L_s$  and  $C_s$  which are on the primary side as shown in Fig. 1, starts resonating with an angular frequency, by  $\omega_{r2} = (1/\sqrt{L_s C_s})$ . The snubber inductor current  $i_{is}$  flows through  $L_s$ ,  $D_{s1}$ ,  $C_s$ , and  $S_1$ .

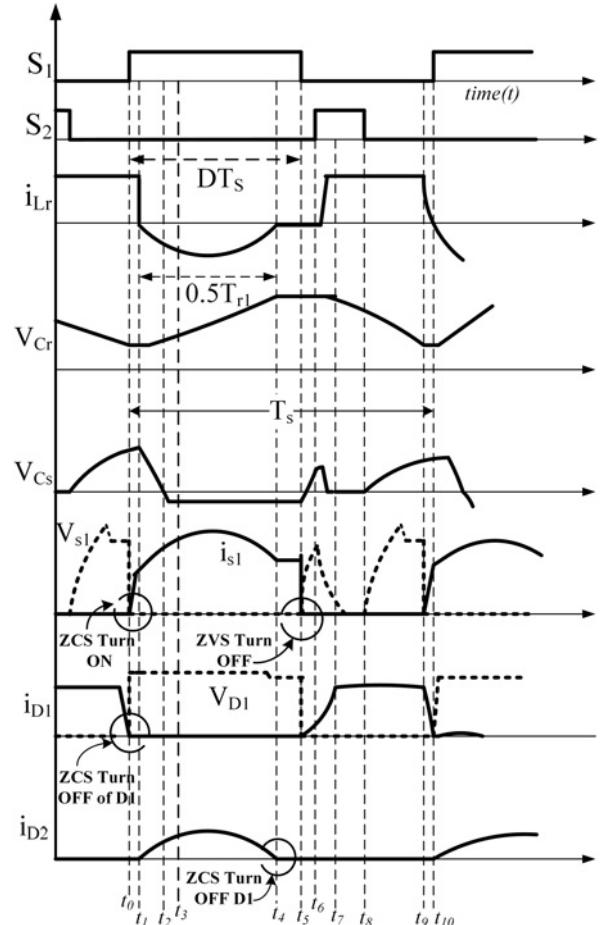
The voltage and current equation can be derived from the equivalent circuit as shown in Fig. 3a. The first-order differential equations that represent this mode are given by  $C_s(dV_{Cs}/dt) = I_{Ls} - I_i$  and  $L_s(di_{Ls}/dt) = V_i - v_{Cs}(t_0)$ , where  $V_i = V_{DC}$ . Furthermore, the expression for the snubber inductor in the second-order differential equation is represented as  $(d^2 i_{Ls}/dt^2) + (1/L_s C_s)i_{Ls} = (I_{Lm}/L_s C_s)$ , where  $i_{Ls}(t) = -I_{Lm}$ . By solving, the above expressions of voltage and current are given by

$$v_{Cs}(t)|_{t_0}^t = |v_{Cs}(t_0)| \cos \{\omega_{r2}(t - t_0)\}, \quad t_0 < t < t_2, \quad (1)$$

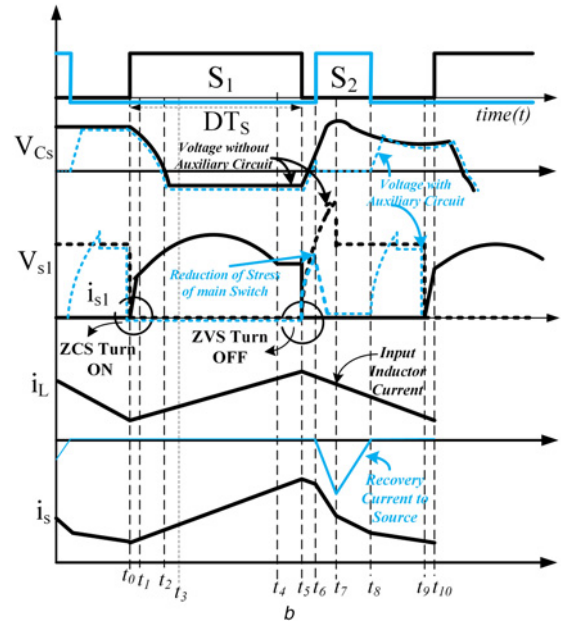
$$i_{Ls}(t)|_{t_0}^t = \left| v_{Cs}(t_0) \sqrt{\frac{C_s}{L_s}} \right| \sin \{\omega_{r2}(t - t_0)\}, \quad t_0 < t < t_2. \quad (2)$$

Main switch current  $i_{s1}$  increases linearly after ZCS turn-on [26]. At the same time,  $i_{Lr}$  starts decreasing as shown in Fig. 2a.

**Mode 2 ( $t_1 - t_2$ ):** This mode starts when the  $i_{Lr}$  direction changes. Resonant current flows through  $L_r$ ,  $C_r$ , and  $D_2$  as shown in Fig. 3a. At time  $t_1$ , resonant capacitor voltage,  $v_{Cr}(t_1) = V_{Cr,min} - nV_{Cc}$ , which can be written as  $v_{Cr}(t) = \{(nV_{Cc} - V_{Cr,min})\} \cos \omega_{r1}(t - t_1)$ , where  $V_{Cc}$  is the clamp capacitor voltage. Again,  $L_r(di_{Lr}/dt) = nV_{Cc} - v_{Cr}(t)$ , where  $t_1 < t < t_4$  then



a



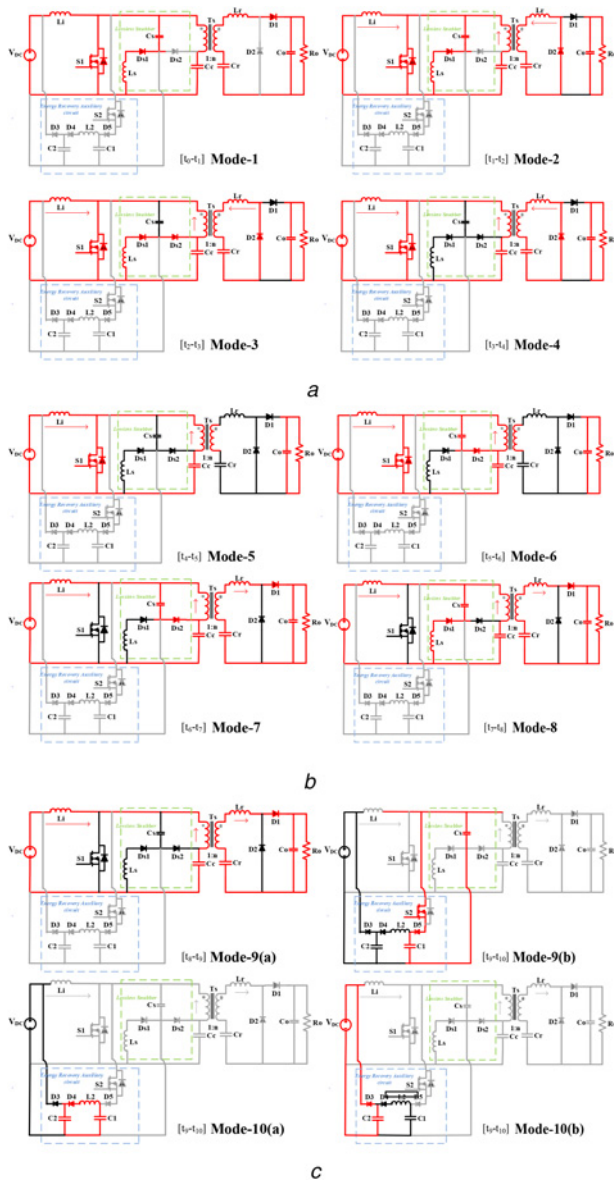
b

**Fig. 2** Circuit operational waveform

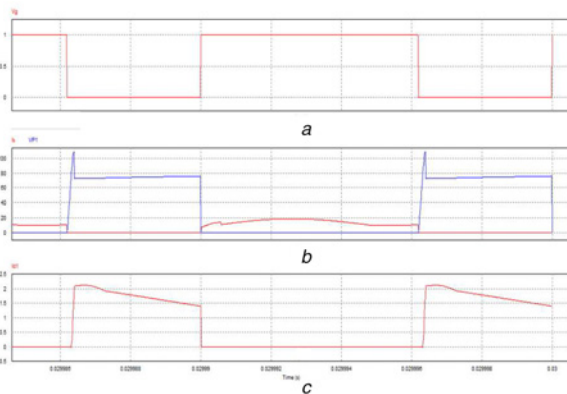
a Waveforms of the converter for below resonance operation  
b Waveforms with considering the effect of auxiliary circuit

the equations for  $v_{Cr}$  and  $i_{Lr}$  are given as

$$\left. \begin{aligned} v_{Cr}(t) &= (v_{Cr,min} - nV_{Cc}) \cos \{\omega_{r1}(t - t_1)\} + nV_{Cc} \\ i_{Lr}(t) &= (v_{Cr,min} - nV_{Cc}) \sqrt{\frac{C_r}{L_r}} \sin \{\omega_{r1}(t - t_1)\} \end{aligned} \right\}. \quad (3)$$



**Fig. 3** Proposed converter operation  
a Mode 1 to mode 4  
b Mode 5 to mode 8  
c Mode 9 to mode 10



**Fig. 4** Below resonance  
a Switching pulse  
b Main switch voltage and current  
c Current of diode  $D_2$

The resonance between  $(L_S - C_S)$  ends when the voltage across  $C_S$  is equal to  $V_{CS} = -V_{CC}$ .

**Mode 3** ( $t_2 - t_3$ ): In this mode,  $D_{S2}$  is turned on as shown in Fig. 4. At steady state voltage across  $C_C$  is  $V_{CC}$ . During  $t_2 < t < t_3$ , current  $i_{Ls}$ , is expressed as  $i_{Ls}(t) = i_{Ls}(t_2) + (V_{CC}/L_s)(t_2 - t)$ ,  $i_{Ls}$  reaches zero and this confirms the end of this mode. As  $i_{Ls}$  is zero and it ensures diode  $D_{S1}$  and  $D_{S2}$  are ZCS turned off.

**Mode 4** ( $t_3 - t_4$ ): This mode ends when  $i_{Lr}$  reaches zero after resonance formed by  $(L_r - C_r)$  as shown in Fig. 3a.

**Mode 5** ( $t_4 - t_5$ ): In this mode,  $i_{S1}$  is equal to  $I_i + I_{Lm}$  which is constant as presented in Fig. 3b.

**Mode 6** ( $t_5 - t_6$ ): This mode starts with turning off of main switch  $S_1$ . Then  $I_i + I_{Lm}$  flows through  $C_s$ ,  $D_{S2}$ , and  $C_c$  as shown in Fig. 5. The voltage across the snubber circuit between  $t_5 < t < t_6$  is determined by

$$v_{Cs}(t) = \frac{I_i + I_{Lm}}{C_s}(t - t_5) - V_{CC}. \quad (4)$$

**Mode 7** ( $t_6 - t_7$ ): In this mode, diode  $D_1$  is on as shown in Fig. 3b.  $L_r$  and  $C_s$  start resonating, and the resonating current flows through  $C_s$ ,  $D_{S2}$ ,  $L_r$ ,  $D_1$ , and  $C_r$

$$i_{Lr}(t) = [1 - \cos(\omega_r(t - t_6))](I_i + I_{Lm}) \text{ for } t_6 < t < t_7, \quad (5)$$

where  $\omega_r = n/\sqrt{L_r C_s}$  and this mode ends when this resonating current reaches the value of  $i_{Lr} = (I_i + I_{Lm})/n$ .

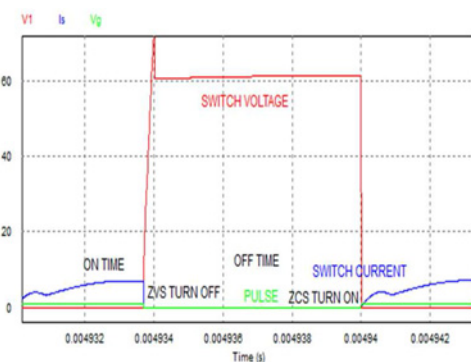
**Mode 8** ( $t_7 - t_8$ ):  $D_{S1}$  is turned-on in this mode as shown in Fig. 3b. Current  $i_{Ls}$  is expressed as

$$i_{Ls}(t) = \left[ V_{CC} + \frac{V_0}{n} - \left( V_{Cs,max} + \frac{V_{Cr,max}}{n} \right) \right] \times \sqrt{\frac{C_s}{L_s}} \sin(\omega_r(t - t_7)).$$

At  $t_8$ ,  $i_{Ls}$  reaches zero value.

**Mode 9** ( $t_8 - t_9$ ): In this mode, switch  $S_1$  is turned-off. Magnetising current maintains core magnetic flux as shown in Fig. 3c.

**Mode 10** ( $t_9 - t_{10}$ ): This mode starts when switch  $S_2$  is turned-on. The stored charge in floating capacitor  $C_s$  is transferred through  $S_2$ ,  $D_5$ , to the capacitor  $C_1$ . The on time for switch  $S_2$  is lesser than main switch  $S_1$  off time. The resonating tank formed by  $L_2$ ,  $C_1$ ,  $C_2$  helps to recover energy to the source when  $D_3$  is in forward bias, shown in Fig. 6. The resonance time is lesser than the turn-on time of auxiliary switch  $S_2$  as mentioned in Fig. 3. The on time of the auxiliary switch is chosen such that average voltages across the floating snubber capacitor become zero. The conversion efficiency is improved because of the energy recovery from the floating capacitor. The current flowing through energy recovery inductor



**Fig. 5** Main switch turn-on (ZCS) and turn-off (ZVS)



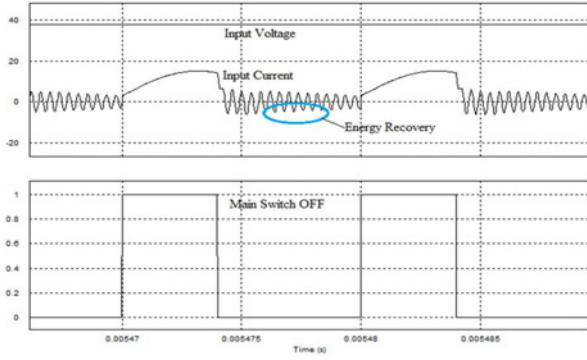


Fig. 6 Energy recovery done by auxiliary circuit

$L_2$  during this time is given as

$$I_{L2} = V_{C1(\max)} \sqrt{\frac{C_1 C_2}{L_2 (C_1 + C_2)}} \sin \sqrt{\frac{C_1 + C_2}{L_1 C_1 C_2}} t. \quad (6)$$

Diode  $D_3$  is forward biased if the voltage across recovery circuit capacitor  $C_2$  (i.e.  $V_{C2}$ ) is higher than supply  $V_{DC}$  input voltage. During turn-off of the main switch  $S_1$ , the leakage stored energy of the transformer across capacitor  $C_s$  is supplied back to the source. It increases power conversion efficiency and reduces the switching stress of the main switch as shown in Fig. 2b.

### 3 Voltage gain of the proposed converter

Let us assume that the voltage across  $C_c$  remains constant and the magnetising current across the transformer is zero during the switching time  $T_s$ . Resonance operation in the circuit can be obtained by three operations such as below resonance operation (i.e.  $DT_s > 0.5T_{r1}$ ), critical resonance operation (i.e.  $DT_s = 0.5T_{r1}$ ), and above resonance operation (i.e.  $DT_s < 0.5T_{r1}$ ). Moreover, only two operations, i.e. below resonance and above resonance operations are explained in detail.

#### 3.1 Below resonance operation ( $DT_s > 0.5T_{r1}$ )

Average current flowing through the diode  $D_2$  is equal to the load current  $I_0$  under the steady state condition. Therefore, the average value of  $I_{D2}$  is given by

$$I_{D2, \text{avg}} = \frac{V_0}{R_0} = \frac{1}{T_s} \int_{t_1}^{t_4} i_{D2}(t) dt = \frac{1}{T_s} \int_{t_1}^{t_4} -i_{Lr}(t) dt. \quad (7)$$

From (7) and (3), the equation for  $V_{Cr}$  can be rewritten as

$$V_{Cr} = nV_{Cc} \pm \frac{V_0}{2C_v f_s R_0} V_{Cr, \max} = nV_{Cc} + \frac{V_0}{2C_v f_s R_0}. \quad (8)$$

Time interval,  $t_7 - t_6 = (\pi/2\omega_{i3})$  from (5) and (8). The voltage gain can be obtained as  $((n + B + C)/(1 - D + A))$  for switching time to  $(1 - D)T_s$ , where

$$A = \frac{\pi f_s}{2\omega_{i3}}, \quad B = \frac{C_s(2C_v f_s R_0 - 1)}{2nC_r},$$

$$C = \frac{C_m[C_v f_s R_0(1 - \cos(\omega_r DT_s)) - \cos(\omega_r DT_s)]}{nC_r(1 - \cos(\omega_r DT_s))},$$

$$\omega_{s1} = \frac{n}{\sqrt{L_1 C_1}} \text{ and } D_2 < D_1.$$

#### 3.2 Above resonance operation ( $DT_s < 0.5T_{r1}$ )

The operating principles remain the same as below resonance. Practically,  $C_s \ll C_r$ . The time interval from  $t_0$  to  $t_3$  can be approximated as  $DT_s$ . The average current of diode  $D_2$  is identical to the average load current, which can be written as  $I_{D2, \text{avg}} = (V_0/R_0) = (1/T_s) \int_{t_1}^{t_4} -i_{Lr}(t) dt$ , where  $i_{D2}(t) = -i_{Lr}(t)$

$$\left. \begin{aligned} V_{Cr, \min} &= nV_{Cc} - \frac{V_0}{C_v f_s R_0(1 - \cos(\omega_{r1} DT_s))} \\ V_{Cr, \max} &= nV_{Cc} + \frac{V_0 \cos(\omega_{r1} DT_s)}{C_v f_s R_0(1 - \cos(\omega_{r1} DT_s))} \end{aligned} \right\}. \quad (9)$$

The time interval between  $t_7$  and  $t_6$  can be expressed as  $\Delta t = (nV_0/I_0 f_s R_0)$  while time interval,  $t_3 - t_5 = (C_s/I_0)((V_0 - V_{Cr, \max})/n) + V_{Cc}$ , Solving the above equations, current gain and voltage gain can be derived, i.e.

$$\frac{I_0}{I_i} = \frac{1 - D - (\pi f_s/2\omega_{i3})}{n + ((C_s(2C_v f_s R_0 - 1))/2nC_r)}, \text{ and } \frac{V_0}{V_i} = \frac{n + C + E}{1 - D - A}, \quad (10)$$

where  $C = ((C_m[C_v f_s R_0(1 - \cos(\omega_r DT_s)) - \cos(\omega_r DT_s)])/(nC_r(1 - \cos(\omega_r DT_s))))$ ,  $E = R_0 f_{s1} C_1(1 - \cos(\omega_{s1} D_2 T_s))$ ,  $A = (\pi f_s/2\omega_{i3})$  and  $\omega_{i3} = (\pi/2(t_7 - t_6))$ .

### 4 Design analysis

The design procedure for the various components is illustrated in this section for the proposed converter. The calculation of various components, i.e.  $L_r$ ,  $C_r$ ,  $L_s$ , and  $C_s$  are explained in detail and finally, loss estimation for the switching devices is discussed.

#### 4.1 Determination of $n$ , $L_r$ , and $C_r$

The voltage gain of the isolated boost converter can be approximated as  $(V_0/V_i) = (n/(1 - D))$  for simplification of the calculation. The duty ratio has to be  $< 0.5$  to maintain zero magnetising flux within a switching cycle. The below-resonance operation is chosen due to smaller switch turn-off current and diode  $di/dt$ . The minimum duty cycle for operation is  $D_{\min} = \pi f_s \sqrt{L_r C_r}$ ,  $L_r$  should be designed such that it minimises the reverse-recovery effects of diode  $D_1$ . The interval from  $t_0$  to  $t_1$ , which is expressed as

$$t_0 - t_1 = 3 t_{\pi 1} = \frac{(I_i + I_{Lm})L_r}{nV_0(1 + 1/2C_v f_s R_0)}. \quad (11)$$

Furthermore

$$I_{S1, \text{rms}} \simeq \sqrt{D} I_i + n \pi I_0 2 \sqrt{2 D_{\min}} \forall (D_{\min} < D < D_{\max})$$

$$\& V_{S1, \text{on}} = v_{S1}(t_0) = V_0 - V_{Cr, \min} + V_{Cc},$$

where  $t_{\pi 1}$  is the reverse-recovery time of diode  $D_1$ . The root-mean square input current and turn-on voltage of switch  $S_1$  can be obtained as follows:

$$I_{S1, \text{rms}} \simeq \sqrt{D} I_i + \frac{n \pi I_0}{2 \sqrt{2 D_{\min}}}, \quad (D_{\min} < D < D_{\max}),$$

$$V_{S1, \text{on}} = v_{S1}(t_0) = \frac{V_0 - V_{Cr, \min}}{n} + V_{Cc}. \quad (12)$$

#### 4.2 Determination of the value of $C_s$

Snubber capacitance  $C_s$  can be calculated from the above equations. The proposed topology explained above had a major advantage over another existing converter listed in Table 1. The advantage

**Table 1** Comparison of DC–DC converters with transformer isolation hardware prototype [27]

Topology	$P_{\max}$ , kW	$f_s$ , kHz	$V_{\text{input}}$	$V_{\text{output}}$	Voltage gain	No. of switches	Gain	Efficiency (%) @250 W
active clamp step up converter [28]	0.10	20	30–60 V	350 V	$n/(1-D)$	2	11.6	89
resonant push-pull converter [8]	1.5	70	35–60	350	$2n/(1-D)$	4	10	90.5
high step-up zero-voltage switching current-fed converter [27]	0.4	100	45	200	$n/[D(1-D)]$	4	4.4	90
resonant half-bridge converter [27]	0.25	100	36	430	—	2	11.9	89.5
resonant half-bridge dual converter [27]	0.1	1000	20	360	—	2	18	90
current fed multi-resonant converter [29]	0.15	255	23	350	—	2	15.2	85
series-parallel Resonant converter [30]	0.19	215	20–35	700	—	4	35	87
proposed topology	0.25	100	24	350	—	2	14.5	93

in terms of gain, voltage stress, and efficiency are superior in the proposed converter even the switch count is approximately near to other topologies with marginal increment in cost

$$\left. \begin{aligned} I_{L_s, \text{avg}} &= \frac{C_s}{T_s} \left[ v_{C_s}(t_0) + 3V_{C_c} - 2V_{C_{s, \max}} + \frac{2(V_0 - V_{C_{r, \max}})}{n} \right. \\ &\quad \left. + 0.5v_{C_s}(t_0) \sin \left( \cos^{-1} \left( \frac{-V_{C_c}}{v_{C_s}(t_0)} \right) \right) \cos^{-1} \left( -\frac{V_{C_c}}{v_{C_s}(t_0)} \right) \right. \\ &\quad \left. v_{C_s}(t_0) = 2 \left( V_{C_c} + \frac{V_0 - V_{C_{r, \max}}}{n} \right) - V_{C_{s, \max}}, \text{ and} \right. \\ &\quad \left. V_{C_{s, \max}} = \frac{I_i + I_{L_m}}{n} \sqrt{L_r/C_s} + \frac{V_0 - V_{C_{r, \max}}}{n} \right] \end{aligned} \right\} \quad (13)$$

#### 4.3 Determination of the value of $L_s$

Snubber inductance  $L_s$  minimised the reverse recovery of snubber diode  $D_{s1}$  and  $D_{s2}$ . Therefore, the time interval from  $t_2$  to  $t_3$  should be greater than  $t_{rr2}$ , which is expressed as

$$t_3 - t_2 = 3t_{rr2} = \frac{v_{C_s}(t_0)L_s \sin(\cos^{-1}(-V_i/v_{C_s}(t_0)))}{V_i} \sqrt{\frac{L_s}{C_s}} \quad (14)$$

where  $t_{rr2}$  is the reverse-recovery time of diodes  $D_{s1}$  and  $D_{s2}$ . Switch selection is based on maximum current and reverse voltage rating, i.e. maximum stress that output diodes  $D_1$  and  $D_2$  have. The maximum voltage stress is  $V_o$ . The peak current of output diode  $D_2$  is  $I_o/n$  from the equation. Maximum stress across the switch  $S_1$  is determined by the following equation:

$$V_{S1, \max}(t) = \frac{I_i + I_{L_m}}{n} \sqrt{\frac{L_r}{C_s}} + \frac{V_0 - V_{C_{r, \max}}}{n} + V_{C_c} \quad (15)$$

#### 4.4 Loss assessment

The energy losses of different components have been estimated using the standard equations and the parameters provided in the datasheet of each component. The switching energy loss and conduction energy loss in metal oxide semiconductor field effect transistor (MOSFET) are calculated by using the following equations:

$$E_{\text{sw}} = E_{\text{on}} + E_{\text{off}} = \frac{1}{2} V_{DC} I_D (t_{\text{on}} + t_{\text{off}}), \quad (16)$$

$$E_{\text{cond}, M} = R_{DS, \text{on}} I_{D, \text{rms}}^2 t_{\text{cond}, M}, \quad (17)$$

where  $t_{\text{on}}$ ,  $t_{\text{off}}$ , and  $t_{\text{cond}, M}$  are the turn-on, turn-off and conduction times of the switch while  $R_{DS, \text{on}}$  is the resistance of the switch.

The switching energy losses in the diode is mainly because of the reverse recovery process which is given by (18) and the conduction loss by (19)

$$E_{\text{sw}, D} = \frac{1}{4} V_{DC} Q_{rr}, \quad (18)$$

$$E_{\text{cond}, D} = (V_{DC} I_{D, \text{avg}} + R_D I_{D, \text{rms}}^2) t_{\text{cond}, D}, \quad (19)$$

where  $Q_{rr}$  and  $R_d$  are the reverse recovery charge and diode resistance, respectively.  $t_{\text{cond}, D}$  is the conduction period of the diode.

## 5 Simulation studies

A simulation study is carried out in PSIM 9.1.1 and MATLAB/Simulink R2014b for the proposed 250 W converter. A simulation parameter is considered based on design equations explained in Section 4 and the parameters available in the data sheet provided by the manufacturer. The switching frequency is selected 100 kHz and the SiC MOSFET manufactured by Rohm Semiconductor part no. SCT3080AL is selected as the switching devices reported in Table 2.

### 5.1 Below resonance operation result ( $DT_s > 0.5T_{r1}$ )

Below resonance operation in the proposed converter is suitable for higher-efficiency operation. Voltage gain is quite significant compared with conventional as shown in Table 1. As it ensures low-conduction loss of switch as well as other components, the efficiency is higher in the low-duty ratio range for the proposed converter. Based on the literature survey, conventional converter and proposed converter usage are important in the low duty ratio with achievement in voltage gain as clearly mentioned in Table 1. Fig. 4 shows the switching pulse, voltage, and current of the

**Table 2** Design parameters and components used of the proposed converter

Parameters	Value	Selected component
transformer	turns ratio	1:5
	mag. inductance	100 $\mu$ H
	leakage inductance	3 $\mu$ H
main switch ( $S_1$ )	current (max.)	22 A
	voltage (max.)	150 V
auxiliary switch ( $S_2$ )	current (max.)	22 A
	voltage (max.)	150 V
snubber inductor ( $L_s$ )	4 $\mu$ H	ferrite core FE16
snubber capacitor ( $C_s$ )	50 nF	125LD10-R
output capacitor ( $C_o$ )	2.2 $\mu$ H	ECA-2GHG2R2
resonant capacitor ( $C_r$ )	100 nF	MKT 369
input inductor ( $L_i$ )	150 $\mu$ H	ferrite core PQ 32/30

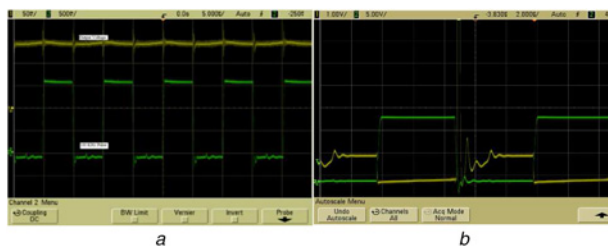
main switch and current in diode  $D_2$ . The main switch is turning on as ZCS while turning off as ZVS, which are reported in Fig. 5. Fig. 6 shows the simulation results of the energy recovery process because of the auxiliary circuit added to the proposed converter. Loss associated with the energy recovery circuit is quite less because of low on time of the auxiliary switch as shown in Fig. 2b. When auxiliary switch  $S_2$  is on then extra energy stored in leakage inductance in the transformer, which is recovered and by that process, it reduces the stress created on the main switch during the turn-off process. In Fig. 6, input voltage and input current waveforms prove that during the turn-off process energy is supplied back to DC source which improves conversion efficiency.

### 5.2 Above resonance operation result ( $DT_s < 0.5T_{rL}$ )

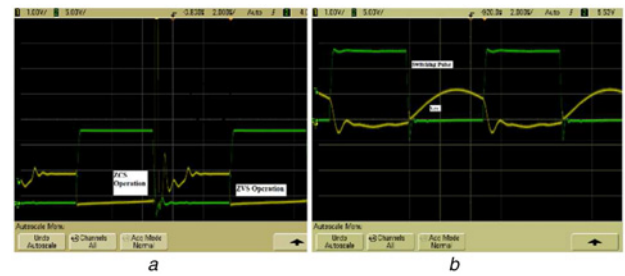
Although converter gain is more in the above resonance operation in all the existing topologies but in work as peak input current increases during the operation which leads to increase in conduction losses. Again, the voltage stress of the main switch increases and converter efficiency deteriorates. Due to these limitations, further investigations are not performed for the above resonance operation.

## 6 Experimental evaluation

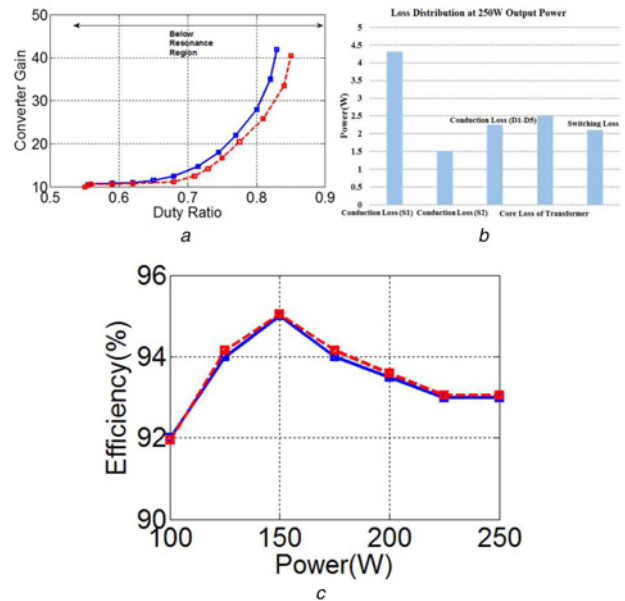
A prototype is designed for the proposed converter and tested for varying the load resistance and duty cycle in the range of  $0.2 < D < 0.4$  and  $D > 0.5$ . The performance of the proposed converter is superior for below resonance operation as mentioned in the simulation analysis and hence the experimental verification has been performed only for the below resonance operation. The gate signals of MOSFET switches are generated through module 9401 of NI c-Rio 9082 in Field Programmable Gate Array (FPGA) interface with the Programmed in Lab-VIEW as demonstrated in the Appendix. The SiC MOSFET is a fast response semiconductor device and hence it requires a high-speed gate driver circuit. Therefore, a driver circuit part no. NCP-5304 is selected which is manufactured by ON semiconductor. Moreover, two driver circuits are used for two MOSFETs, which are controlled by the NI c-Rio 9082. The waveforms of gate signals and the converter output voltage are shown in Fig. 7a. The experimental results show that the main switch turning on as ZCS while turning off as ZVS, which are shown in Fig. 7b. Although the current spike is quite high during commutation at that time voltage is significantly low or equivalent to zero and hence overall losses are zero. As shown in Fig. 8b voltage stress across the main switch of the converter is quite less because during off time snubber capacitor  $C_s$  lifts some voltage with  $L_s$ , which reduces peak reverse voltage. Again, auxiliary switch  $S_2$  is turned-on after dead time which further reduces reverse voltage appears across the main switch. Thus, switching stress is quite less in the proposed converter than conventional converters. At 100 kHz switching frequency, for a given turn ratio (1:5), the gain of the converter versus duty ratio considering load resistance 360  $\Omega$  is shown in Fig. 9a theoretically as well as



**Fig. 7** Soft switching  
a Waveforms of switching signals (green) and output voltage (yellow)  
b Voltage (green) and currents (yellow) waveforms of the main switch (ZCS turn-on and ZVS turn-off)



**Fig. 8** Converter switching waveform  
a ZCS turn-on and ZVS turn-off  
b Snubber capacitor voltage ( $V_{cs}$ )



**Fig. 9** Converter performance  
a Voltage gain versus duty ratio of proposed converter [blue solid line shows theoretical results while red dashed line shows the experimental results]  
b Loss components of MOSFET and diodes at 250 W output power  
c Output power versus efficiency (red dashed line shows theoretical efficiency while blue solid line shows experimental value)

practically. It is observed from Fig. 9a, there is a marginal difference between theoretical gain and experimental gain of the converter with the variation of the duty ratio up to 0.7.

Various loss components of the proposed converter for below resonance operation are calculated using the formulae in previous sections, which are shown in the bar chart of Fig. 9b for 250 W. It is observed from the bar chart that the conduction loss  $S_1$  is higher than  $S_2$  because of a large conduction period. Another significant finding is that the switching losses are comparatively low because of proper soft switching.

The efficiency of the prototype is estimated by measuring input power and output power as shown in Fig. 9c. The red dashed line shows the computational efficiency while the blue solid line shows the experimental value. The variation between computational and experimental data is very negligible which validates the theoretical findings. Initially, the effect of a magnetic loss component on the switching transformer is less, therefore efficiency is increased up to 150 W and reached the maximum value 95%, where flux resetting is properly achieved. Then the efficiency of the proposed converter starts decreasing up to 225 W and settles down at 93% constant efficiency. The reason of decrement in efficiency is the significant effect of the magnetic loss component on the switching transformer.

## 7 Conclusion

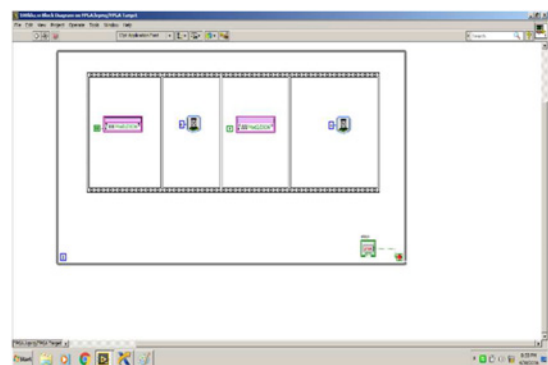
This study proposes a novel single stage isolated high-frequency link boost converter. A comprehensive circuit analysis in CCM with design procedure considering non-idealities are analysed. Leakage inductance is used for secondary side resonance which ensures a low loss in a high-frequency switching transformer. An energy recovery circuit helps in recovering floating capacitor energy and also it reduces switching voltage stress across the main switch. True ZCS turn-on and ZVS turn-off are achieved in the main switch by a loss-less snubber circuit connected to the primary winding of a high-frequency transformer. In addition, secondary side diodes  $D_1$  and  $D_2$  are turned-off under ZCS conditions. All theoretical findings are verified through the designed prototype of a 250 W converter. This converter is particularly useful where high voltage gain and higher efficiency application are required at a low-duty ratio. Furthermore, reduction in switching voltage stress enhances the reliability of the proposed converter.

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## 9 Appendix

The NI c-Rio 9082 in the FPGA interface is used to generate the signal for the MOSFET driver circuit. The increased processing power of the c-Rio 9082 is useful and well suited to perform advanced processing tasks required. Programme in Lab-VIEW for 0.4 duty ratio at 100 kHz is shown in Fig. 10.



**Fig. 10** Programming in FPGA mode (programme for 0.4 duty ratio at 100 kHz)