Natural-air-cooled 5 kVA single-phase GaN inverter with paralleled multilayer PCB magnetics

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Published in *The Journal of Engineering*; Received on 21st August 2017; Revised on 24th November 2017; Accepted on 6th December 2017

Abstract: In this study, a systematic approach to the design and development of a high-efficiency, natural-air-cooled, single-phase inverter with a multilayer high-current printed-circuit board (PCB) magnetics is presented. The size and efficiency of inverters implemented with the silicon transistor technology have almost reached a certain limit. The use of wide bandgap power semiconductors, such as the silicon carbide metal–oxide–semiconductor field-effect transistor and the gallium nitride (GaN) enhancement-mode (e-mode) transistor not only pushes further the efficiency limits, but also shrinks the inverter size. A new approach is proposed here in order to obtain a high-efficiency inverter which relies basically upon the derivation of analytical expressions for the inverter losses as a function of the inverter modulation index, for the optimum transistor and highest switching frequency pair selection, and the design of the output filter based on a paralleled, multilayer PCB magnetics. In the developed 5 kVA single-phase full-bridge inverter, GaN e-mode transistors are used to minimise the inverter losses and to decrease the cooling requirement, and size of the system. The proposed systematic design approach has been verified on the implemented 5 kVA, 50 kHz, naturally-cooled GaN inverter, with a power density of 2.7 W/cm^3 (44.3 W/inch^3), and a full-load efficiency of 98%.

1 Introduction

The efficiency of power converters has been a major concern for the industry and academia for years. It has reached the theoretical limits with silicon power metal–oxide–semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) [1, 2]. Thanks to the advances in power semiconductor technology, wide bandgap power semiconductors, such as the silicon carbide (SiC) MOSFET and the gallium nitride enhancement mode (GaN e-mode) transistors, make now possible the design of power converters at higher switching frequencies, lower size, and hence higher power densities. Among these, single-phase inverters share a considerable part in small-size uninterruptible power supplies, household applications, photovoltaic energy conversion systems, and so on. Reduction in the size and weight of the single-phase inverter increases the applicability and modularity of the whole system.

Power converters using wide bandgap devices have been paid great attention due to the increased switching frequencies. In [3], a boost converter application using SiC MOSFET at 300 kHz switching frequency and at a power level of 1.2 kW is reported. Similarly, for the same topology, higher converter efficiencies can be reached using SiC MOSFETs instead of Si MOSFETs [4]. For the single-phase inverters, Google Little Box Challenge [5] has contributed to the inverter volume shrinking issue. In this contest, utilisation of wide bandgap power semiconductors, power decoupling methods, and proper mechanical integration of components lead to the design of compact single-phase inverters. Power density can be further increased by using forced-air cooling. However, in practice, fans used in forced-air cooling have limited lifetime, in the order of a few ten thousands of hours only [6]. To overcome the undesirable effects of forced-air cooling which reduces the reliability and applicability of the system, research work has been carried out to increase the power density of the natural-air-cooled single-phase inverters with the GaN e-mode transistor-based full-bridge circuit, by applying interleaved switching with modified modulation techniques, and some active power decoupling methods [7]. On the other hand, a T-type, single-phase inverter has been implemented with Si IGBT, SiC MOSFET, and GaN transistors for performance comparison in [8]. DC-link capacitors constitute one of the major components affecting the total inverter volume, which can be reduced by using active power decoupling [9], at the expense of extra power losses, and reduced overall efficiency of the single-phase inverter [10].

In this research and development work, a new design approach is proposed for a natural-air-cooled, high power density, high-efficiency, single-phase GaN inverter. Systematic design steps to achieve the volume and efficiency targets of the inverter are described. First, analytical calculation of transistor losses as a function of the inverter modulation index, m, enables the selection of optimum transistor and highest switching frequency pair for a given application, without running time consuming computer simulations. Then, a new multilayer high-current printed-circuit board (PCB) magnetics design methodology is presented for the output filter inductor, to minimise the weight and volume, at a smaller temperature rise as compared to the conventional wired inductor designs. The proposed design approach is verified on the developed, natural-air-cooled, 5 kVA, 50 kHz, single-phase GaN inverter. The practical aspects of the implementation and the associated experimental results are given in detail.

2 Systematic design approach

The systematic design of the single-phase, naturally-cooled, 5 kVA, full-bridge inverter in Fig. 1 will be initiated by selecting the most suitable power transistor among the wide bandgap power semiconductors and new generation Si MOSFET alternatives, in order to meet the target efficiency and volume specifications at the highest possible switching frequency. This will be achieved first by means of the proposed analytical transistor loss calculation method, instead of running time consuming computer simulations, and then by applying a new, paralleled multilayer PCB magnetics design approach for a natural-air-cooled output filter inductor.

2.1 System description

Technical specifications of the single-phase inverter to be designed are given in Table 1. In this circuit topology, active power

doi: 10.1049/joe.2017.0355

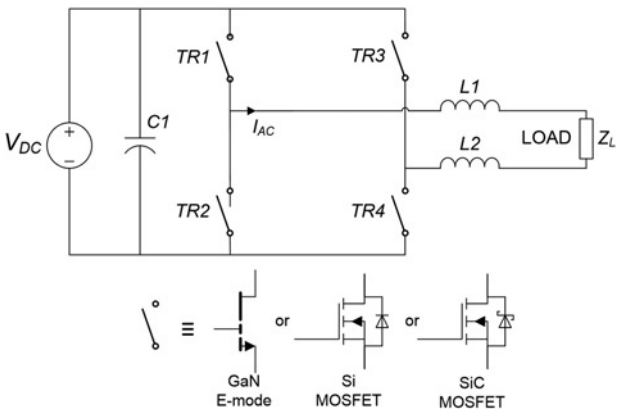

Fig. 1 *Single-phase full-bridge inverter circuit*

Table 1 Single-phase inverter technical specifications

Parameter	Value
input voltage	370 V ± 30 V DC
output power	5 kVA
output voltage	230 V RMS, 50 Hz
output current	30 A peak
output current ripple	10% peak
target efficiency	98%
target power density	2.5 W/cm^3
target volume	2 lt

decoupling methods have not been used in order to maximise the efficiency. In order to avoid the common-mode currents, bipolar pulse width modulation method is applied to the full-bridge circuit, with a precaution taken against the common-mode currents by the symmetry of the AC line connections. For this purpose, the output filter inductor is split into two identical filter inductors $L1$ and $L2$ in the power stage, as shown in Fig. 1. The main components determining the size of the inverter are, (i) output filter inductors $L1$ and $L2$, (ii) power transistors $TR1$, $TR2$, $TR3$, $TR4$ and their cooling heat sinks, and (iii) DC-link capacitor, $C1$. Minimum inverter size will be achieved via the proper selection and design of these main components.

2.2 *Analytical approach for power transistor loss calculation*

The total loss limit is found to be 102 W for the target efficiency in Table 1. The target power transistor loss contribution to total inverter loss can be initially set to nearly 60%, as shown by design for similar power ratings [11]. Hence, total transistor loss budget is calculated as 61.2 W, which means that 15.3 W maximum power loss is allowed for each power transistor. The next step is to determine the candidate power transistors for this application, by taking the technical specifications given in Table 1 into account. For a single-phase inverter with 370 V DC input, Si CoolMOS C7 series, SiC MOSFET, and GaN e-mode transistors (with 650 V or above breakdown voltage levels) are the most possible options for a high-efficiency design. Electrical ratings of three such up-to-date power transistor candidates are given in Table 2.

The transistor power loss components, the conduction loss, P_{cond}, and the switching loss, P_{sw}, for each of the Si MOSFET, SiC MOSFET, and GaN e-mode transistors are to be expressed analytically for a quick systematic design. Note that all three power transistors have reverse conduction capability via their conducting channels. On the other hand, during the negative cycle of the phase current, the anti-parallel diode conducts only during the dead-time period. Si and SiC MOSFETs anti-parallel body diode with a specified forward voltage drop is active in the dead-time period, and the characteristics of the diode do not change with varying gate-to-source voltage. On the other hand, GaN e-mode transistor behaves like a diode, whose threshold voltage, $V_{\text{D0}}(V_{\text{GS}})$, and effective resistance, $R_{\text{DSoff}}(V_{\text{GS}})$, varies with the OFF-state gate-to-source voltage (reverse-conduction operation mode). Hence, for the conduction loss calculation, the GaN e-mode transistor should be handled separately.

For an accurate analytical calculation of conduction losses, transistor root mean square (RMS) current, I_{Drms}, the reverse average current, I_{Rav}, and the reverse RMS current, I_{Rrms}, expressions should be derived. Also, body diode losses during dead time should be calculated using the threshold voltage, V_{D0}, and the effective resistance of the body diode, R_{D}. Total conduction loss expressions, P_{cond}, of all transistors are given in Table 3.

For switching loss calculation, turn-on and turn-off parameters of transistors specified in the datasheets should be scaled according to the operating conditions of the inverter. The transistor parameters given in Table 2, such as the rise time t_{r}, fall time, t_{f}, drain-to-source resistance, R_{DSon}, and reverse recovery charge Q_{rr}, are used in the calculation of P_{sw}. I_{DS} and V_{DS} in Table 3 denote the transistor peak current and peak voltage values, respectively, for one period of the fundamental output current and voltage waveforms. For the

Table 2 Candidate transistors' technical specifications

	Silicon Infineon IPW65R019C7	SiC ROHM SCT3030AL	GaN e-mode Gansystems GS66516T
breakdown voltage	650 V	650 V	650 V
continuous current	75 A (25°C)	70 A (25°C)	60 A (25°C)
on-state resistance	19 mΩ	30 mΩ	25 mΩ
total gate charge	215 nC	104 nC	12.1 nC
recovery charge	20 µC	130 nC	0
package	TO-247	TO-247-3	GaN PX

Table 3 Transistor power loss expressions

	Si MOSFET	SiC MOSFET	GaN e-mode
P_{cond}	$R_{\text{DSon}}I_{\text{Drms}}^2 + V_{\text{D0}}I_{\text{Rav}} + R_{\text{D}}I_{\text{Rrms}}^2$		$R_{\text{DSon}}I_{\text{Drms}}^2 + V_{\text{D0}}I_{\text{Rav}} + R_{\text{DSoff}}I_{\text{Rrms}}^2$
P_{sw}	$\left(\frac{I_{\text{DS}}}{\pi}V_{\text{DS}}(t_{\text{r}}+t_{\text{f}}) + Q_{\text{rr}}V_{\text{DS}}\right)f_{\text{sw}} + 0.25Q_{\text{rr}}V_{\text{DS}}f_{\text{sw}}$		$\left(\frac{I_{\text{DS}}}{\pi}V_{\text{DS}}(t_{\text{r}}+t_{\text{f}})\right)f_{\text{sw}}$

GaN transistor, Q_{rr}, is zero, and thus not included in the switching loss calculation.

In order to derive an analytical expression for the RMS current values in Table 3, first an exaggerated waveform of the transistor current in conjunction with the AC output current will be considered as shown in Fig. 2. In this plot, the transistor current is shown to be composed of a few pulses only for the sake of illustration, due to the difficulty in representing the current pulses at relatively high switching frequencies, f_{sw}, in practice. Also, it should be noted that the transistor current waveform given in Fig. 2 is valid for reverse conducting power switches. As illustrated in Fig. 2, k stands for the pulse number. In one fundamental period, T_s, of the output current, there exist N pulses, as calculated from the following equation:

$$N = \frac{T_s}{T_{sw}} \tag{1}$$

where T_{sw} is the switching period. The approach in this derivation relies upon the fact that the square root of the sum of mean-square values of pulses from 1 to N is equal to the RMS value of the transistor current, I_{Drms}, as expressed in the following equation:

$$I_{Drms} = \sqrt{I_{1rms}^2 + I_{2rms}^2 \cdots + I_{krms}^2 \cdots + I_{Nrms}^2} \tag{2}$$

Here, the mean-square value of the kth pulse can be calculated from the following equation:

$$I_{krms}^2 = \frac{1}{T_s}\int_{t}^{t+d(t)T_{sw}} I^2 \sin^2(wx+\theta)\,dx \tag{3}$$

where θ stands for the phase angle between the fundamental phase voltage and current waveforms. The integral limits here are t and $t + d(t)T_{sw}$, where $d(t)$ is the duty cycle of the transistors, and m is the modulation index calculated from the following equation:

$$m = \frac{V_{out}}{V_{DC}} \tag{4}$$

where V_{out} is the inverter peak output voltage and V_{DC} is the inverter DC input voltage.

The duty cycle can then be expressed as given in the following equation:

$$d(t) = \frac{1 + m\sin(wt)}{2} \tag{5}$$

In (5), $\omega = 2\pi f_s$ where f_s is the inverter output frequency. Since, $T_s = NT_{sw}$, t in (3) can be replaced by kT_{sw}, resulting in the following equation:

$$\begin{aligned} I_{krms}^2 &= \frac{1}{T_s}\int_{kT_{sw}}^{(k+d(kT_{sw}))T_{sw}} I^2\sin^2(wx+\theta)\,dx \\ &= \frac{I^2}{2T_s}\int_{kT_{sw}}^{(k+d(kT_{sw}))T_{sw}} [1-\cos(2wx+2\theta)]\,dx \\ &= \frac{I^2}{2T_s}\left[d(kT_{sw})T_{sw} - \frac{1}{2w}\left[\sin(2w(k+d(kT_{sw}))T_{sw}\right.\right. \\ &\quad \left.\left. +2\theta) - \sin(2wkT_{sw}+2\theta)\right]\right] \end{aligned} \tag{6}$$

Finally, by substituting $d(t)$ in (6), the analytical expression of I_{Drms} in terms of m and θ is obtained as in (7). This RMS current calculation approach is also verified by computer simulations

$$\begin{aligned} I_{Drms} = \left(\sum_{k=1}^{k=N}\frac{I^2}{2T_s}\left[\frac{1+m\sin(wkT_{sw})}{2}T_{sw}\right.\right. \\ -\frac{1}{2w}\left[\sin(wT_{sw}(2k+1+m\sin(wkT_{sw}))+2\theta)\right. \\ \left.\left.\left.-\sin(2wkT_{sw}+2\theta)\right]\right]\right)^{1/2} \end{aligned} \tag{7}$$

A single-phase inverter simulation model is constructed in MATLAB-Simulink by using the technical specifications of the sample inverter given in Section 2.1. From the simulation model, transistor RMS current is tabulated for one switching period, T_{sw}, using both the MATLAB RMS function block and the derived transistor RMS current, as shown in Table 4. Almost the same transistor RMS current is obtained from both computer simulations and analytical calculations, the small difference being attributed to the small high-frequency ripple on the output current, which is neglected in the analytical calculations.

Additionally, the reverse conduction RMS current, I_{Rrms}, can be expressed analytically as in (8), by using the approach followed in I_{Drms} calculation. In the I_{Rrms} expression, T_d stands for the dead-time period. Also, for the reverse conduction loss, average current flowing through the Si and SiC MOSFETs can be derived as given in (9). I_{Rav} can be expressed similar to the I_{Rrms} case, and

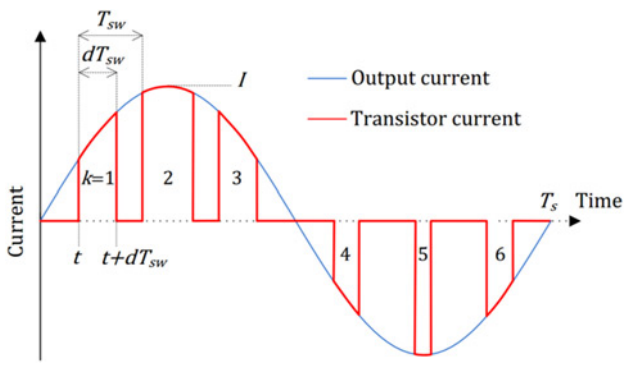

Fig. 2 *Single-phase inverter transistor current waveform*

Table 4 RMS calculation comparison

Time, ms	Computer simulation, A	Analytical calculation, A
1	7.57	8.02
2	15.69	16.24
3	22.98	23.20
4	28.05	28.24
5	29.92	29.99
6	28.19	28.11
7	23.24	22.97
8	16.04	15.58
9	7.94	7.39
10	0.49	0.42
11	4.65	5.69
12	7.56	8.02
13	7.39	7.40
14	4.61	4.47
15	2.06	0
16	4.50	4.47
17	7.58	7.58
18	7.98	7.98
19	5.40	5.40
20	0.26	0.10

doi: 10.1049/joe.2017.0355

has negligibly small magnitude, since the MOSFET body diodes conduct during dead-time periods only

$$I_{\mathrm{Rrms}} = \left(\sum_{k=1}^{k=N/2} \frac{I^2}{2T_{\mathrm{s}}} \left[-\frac{1}{2w} \left[\sin\left(2wkT_{\mathrm{sw}} + 2\theta + 2wT_{\mathrm{d}}\right) - \sin\left(2wkT_{\mathrm{sw}} + 2\theta\right) \right] \right] \right)^{1/2} \quad (8)$$

$$I_{\mathrm{Rav}} = \sum_{k=1}^{k=N/2} \frac{I}{2\pi} \left[\cos\left(wkT_{\mathrm{sw}} + \theta + wT_{\mathrm{d}}\right) - \cos\left(wkT_{\mathrm{sw}} + \theta\right) \right] \quad (9)$$

In order to select the highest transistor switching frequency within the power loss budget, total power loss of each candidate transistor should be calculated, from the analytical expressions. Using the loss relations in Table 3, and the analytical expressions for RMS and average currents in (7)–(9), each candidate transistor's conduction, switching, and total loss plot can be obtained as a function of the switching frequency and operating current as in Fig. 3. Peak output current is swept from 0 to 50 A, and switching frequency from 5 to 80 kHz, for the sake of illustration. Switching power loss is computed from the expressions given in Table 3, by linearly scaling the switching turn-on and turn-off energies with respect to the operating voltage and current. It should be noted that although Si MOSFET has the lowest conduction loss for all operating points, GaN e-mode transistor is the best in terms of switching loss. The total power loss curves in Fig. 3*c* show that the GaN e-mode transistor gives the best overall performance for this sample design. Considering the total loss plot, among three power transistor candidates, GaN e-mode transistor loss curve crosses the power loss limit curve at a higher switching frequency point for all current levels, as seen from Fig. 3*d*. Therefore, GaN e-mode transistor should be selected for this application, to meet the efficiency and volume targets.

Maximum switching frequency for GaN e-mode transistor is 52 kHz under 15.3 W power loss limit, as shown in Fig. 3*d*. Hence, for this application, switching frequency is set to 50 kHz. A loss comparison for all three power transistors at 50 kHz, is given in Table 5. For this single-phase inverter application, the majority of the total loss is due to switching, for Si and SiC MOSFETs. GaN transistor creates a difference in reducing the switching loss by three times with respect to SiC MOSFET and ~20 times with respect to Si MOSFET, while showing a closer performance with others in terms of conduction loss. Total GaN transistor loss is found to be nearly one-half of the SiC MOSFET loss, and more than one-tenth of Si MOSFET loss for this application.

For the positive half-cycle of the line current, the high-side transistor carries a forward current while the low-side transistor a reverse current, consecutively in each switching cycle, and vice versa for the negative half cycle. During reverse conduction, the effective resistance of GaN transistor is the same as that of forward conduction, R_{DSon}. As a result, in the calculation of RMS transistor current, both the positive and negative cycles should be taken into account. The only exception is the dead-time period. During this period, the GaN transistor conducts a reverse current with an equivalent voltage drop, V_{D0}, and a resistance, R_{DSoff}, which are much higher than those in the case of forward conduction. As a result, the RMS current and hence the power loss should be handled separately during the dead-time period. For this purpose, I_{Rrms} in (8) and I_{Rav} in (9) are derived. Since the dead-time period of GaN transistor is negligibly small, the corresponding power loss is in the order of 0.1% of the total transistor conduction loss.

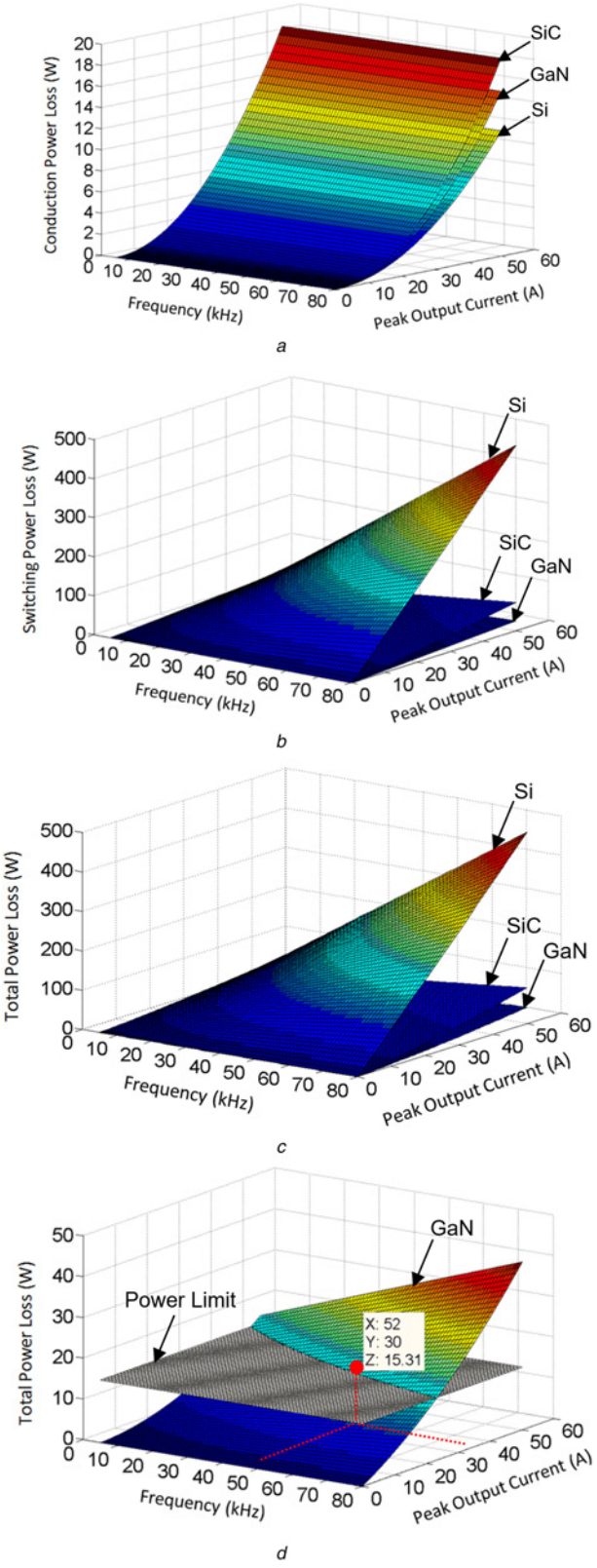

Fig. 3 *Candidate transistor power loss plots*
a Conduction power loss
b Switching power loss
c Total power loss
d GaN transistor total power loss

2.3 Multilayer high current PCB magnetics design procedure

A major component of the single-phase inverter, which determines the total size, is the output filter inductor. In this application, an L-type output filter will be designed for the sake of reduced complexity. The design is initiated by determining the area product of the required inductor, with the filter loss distribution between core and copper losses chosen as 50% each for optimum design, initially.

doi: 10.1049/joe.2017.0355

Table 5 Total power loss with GaN e-mode transistor

Transistor	Switching loss, W	Conduction loss, W	Total power loss, W
IPW65R019C7	177.68	4.87	182.55
SCT3030AL	27.10	7.68	34.78
GS66516T	8.77	6.40	15.17

For a few kVA applications, planar inductor designs with copper foil conductors are being used as the state-of-the-art technique, instead of the classical wired inductor design. In this work, a new approach has been proposed for the output inductor design of a few tens of amperes, called the paralleled multilayer, high current PCB magnetics. The multilayer PCB approach brings flexibility in the design, and standardisation and ease in the manufacturing process. The thickness of traces forming the winding can be adjusted by choosing the trace widths in the PCB. In particular, copper foil or Litz-wire like designs can be implemented easier, and hence high-frequency effects, such as the skin and proximity effects can be suppressed better. Furthermore, due to the layer by layer design, the copper density is distributed through the layers of the PCB, and a lower thermal resistance is obtained. Parallel connection of multilayer PCBs further contributes to the cooling and current rating of the windings.

In the sample design, the output filter inductance is calculated from the ripple current, $\Delta I_{\max}$, which is selected as 10% peak with respect to 30 A peak output current, at 50 kHz. Hence, the required total inductance is calculated as 600 µH from the following equation:

$$L = \frac{V_{\mathrm{DC}}}{4 f_{\mathrm{sw}} \Delta I_{\max}} \tag{10}$$

Taking common-mode current minimisation into account, the inductance is shared between the phase legs, and 600 µH inductance is split into two 300 µH inductances on both of the inverter phase legs ($L1$ and $L2$ in Fig. 1). The design of the output filter inductor is initiated by the area product method [12], using the following equation:

$$LI I_{\mathrm{RMS}} = k_{\mathrm{cu}} J_{\mathrm{RMS}} \hat{B} A_{\mathrm{W}} A_{\mathrm{core}} \tag{11}$$

where I is the peak inductor current, I_{RMS} is the inductor RMS current, k_{cu} is copper fill factor, J_{RMS} is the RMS current density, $\hat{B}$ is the peak flux density, A_{w} is the winding area of the core, and A_{core} is the core cross-sectional area.

2.3.1 Magnetic core design: For the inductor design, among different core material alternatives such as the Molybdenum Permalloy Powder (MPP), High Flux, XFlux, and Kool Mu [13], Kool Mu has been chosen for the best trade-off between core loss and saturation flux density. The required area product can be calculated for Kool Mu by setting peak core flux density to 0.75 T. In the design, peak ripple current is selected as 3 A. The copper fill factor of the PCB winding is assumed to be 0.15, and the current density is selected as 6 A/mm^2. By substituting these values into (11), the required area product, $A_{\mathrm{w}}A_{\mathrm{core}}$, is calculated as 31.09 cm^4. Since the core will be used with PCB windings, E or U core shapes are preferable. In the case optimum core sizing cannot be achieved with standard E or U cores, the required area product can be constructed with some commercially available core blocks. By this way, optimum core sizing can be achieved for various magnetics designs.

In the design approach, initially it is assumed that nearly 40% of the total loss comes from the output inductors, which corresponds to a loss budget of 40.8 W for inductors. Since the inductor is split into two equal parts, the loss limit is 20.4 W, for each. For maximum efficiency, target copper and core losses will be equally distributed for each inductor. Therefore, for each associated core, the core loss limit is 10.2 W. For optimum core sizing, each inductor's core has been constructed by using Magnetics Kool Mu rectangular core blocks (product number: 00K6030B090), since the dimensions of the E- or U-shaped standard cores satisfying the required area product, were over-sized. The size of a full core block is 60 mm × 30 mm × 15 mm, as shown in Fig. 4*b*. Full size Kool Mu blocks are used in the horizontal sections of the core, whereas, half-size cores, in the vertical sections by dividing each full-block into two equal parts. To assemble the core blocks, epoxy-based Loctite® ESP-109 adhesive is employed. The core and winding areas thus obtained are calculated as $A_{\mathrm{core}} = 4.5$ cm^2, and $A_{\mathrm{w}} = 9$ cm^2, respectively. Hence, the area product of the core can be calculated as $A_{\mathrm{w}}A_{\mathrm{core}} = 40.5$ cm^4, which is greater than the required 31.09 cm^4, with a safety margin of 30%. Subsequently,

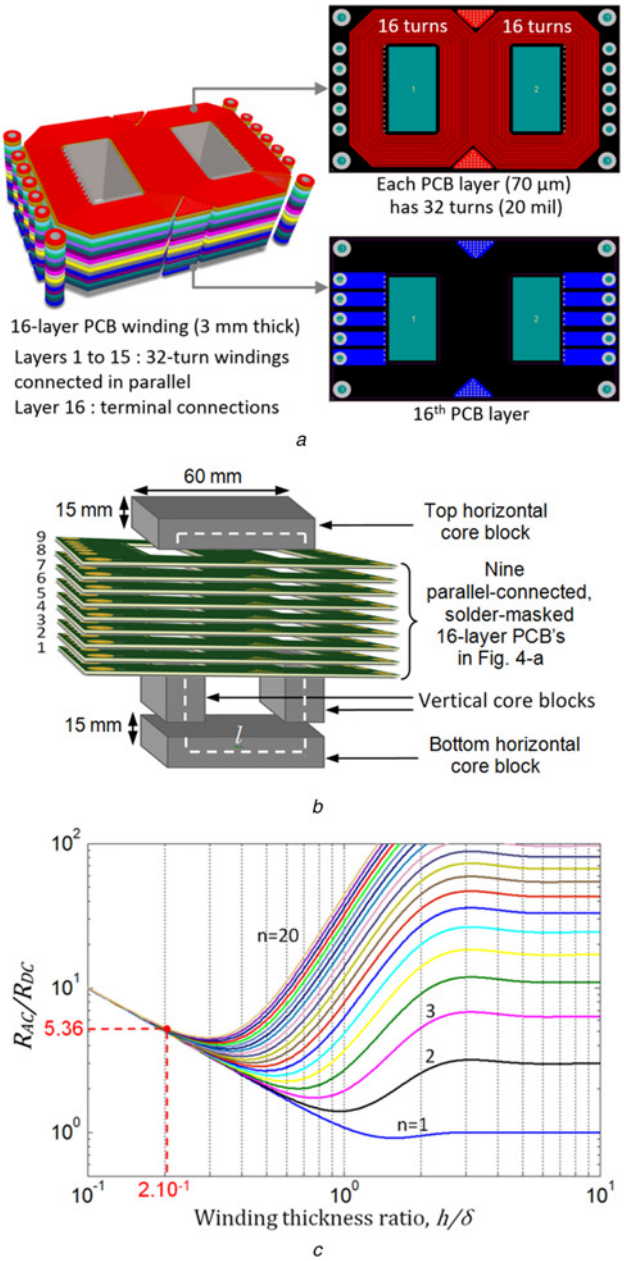

Fig. 4 *Paralleled multilayer PCB magnetics design*
a Winding structure in a multilayer PCB
b Parallel-connected multilayer PCB based inductor design with 1 mm air duct between PCBs
c High-frequency AC loss curves

doi: 10.1049/joe.2017.0355

the number of turns of the inductor, N, is calculated as 32, by using (12), where l is the mean core length, and μ is the core permeability

$$N = \sqrt{\frac{Ll}{\mu A_{\text{core}}}} \tag{12}$$

After determining the core dimensions and number of turns, core loss should be calculated and checked with the target value. It is composed of 50 and 50 kHz components. The peak values of flux density swing, B_{ac}, are calculated separately for both the 50 Hz and the 50 kHz components, as 0.65 and 0.065 T, respectively, from the following equation:

$$B_{\text{ac}} = \frac{N\Delta I_{\max}\mu}{l} \tag{13}$$

The total volume of the custom core is 81 cm^3. Core loss per unit volume in W/cm^3 is obtained from (14), as specified by the manufacturer [13]

$$P_{\text{core/vol}} = 193B_{\text{ac}}^{2.01}f^{1.29} \tag{14}$$

The 10% peak flux density ripple of 0.065 T at 50 kHz and the peak flux density of 0.65 T at 50 Hz yield to a total core loss, $P_{\text{core}} = 10.14$ W, which meets the target value of 10.2 W.

2.3.2 Multilayer high-current PCB winding design: In the design of the copper winding structure, the skin effect, proximity effect, and DC resistance should be considered. Although the high-frequency ripple is small, skin depth, δ, will be taken into account in the selection of the trace thickness, and in the calculation of high-frequency losses. For the 50 kHz component, the skin depth, δ, can be approximately calculated from [14] as 0.34 mm. Following design steps will then be sequentially carried out:

- *First, calculate the PCB trace width and thickness by using the manufacturing tolerances, and skin depth, δ*: The trace width of the windings is determined by considering the mechanical constraints of the core winding area. 1 mm (39.37 mil) mechanical tolerance in addition to 1.27 mm (50 mil) PCB keep out from both edges are subtracted from the 30 mm (1181 mil) window width to obtain the effective window width of the custom-designed core as 25.46 mm (1002 mil). For the sake of low leakage and symmetry, 16 turns will be distributed to each leg to obtain $N = 32$ turns. For each winding, the available space is 0.84 mm (33 mil). By assuming 10 mil PCB manufacturing clearance, it is possible to use traces with 20 mil width, utmost. The thickness of the copper in each layer is selected as 70 µm, with the available low-cost PCB manufacturing facilities. This value can be increased up to 230 µm, at the expense of extra cost.
- *Design the multilayer PCB winding and determine the number of PCBs in parallel to reduce copper loss*: Maximum PCB thickness and maximum number of layers are dictated by the PCB manufacturer, which are specified to be 3 mm, and 16 layers, respectively, for the local manufacturers. The number of PCB winding layers is therefore selected as 15, and the remaining one layer is used for terminal outputs. As seen from Fig. 4*a*, the winding structure is repeated in 15 layers of the PCB. Nine such solder-masked PCBs are connected in parallel in order to increase the effective copper thickness, as shown in Fig. 4*c*. 1 mm air duct is put between the multilayer PCBs for a better cooling, since effective cooling surface of the windings is increased. The corresponding total copper cross-sectional area is then calculated as 4.8 mm^2, from the following equation:

$$A_{\text{copper}} = t_{\text{w}}t_{\text{t}}np \tag{15}$$

where t_{w} is the trace width, t_{t} is the trace thickness, n is the number of layers in one PCB and p is the number of parallel-connected multilayer PCBs. Hence, for the 21.2 A RMS rated current, the corresponding current density is calculated as 4.42 A/mm^2. The mean length of the winding for one turn is 15 cm. This corresponds to 4.8 m for $N = 32$ turns. Hence, the DC resistance, R_{DC}, of the winding can be calculated as 19.5 mΩ. Consequently, total DC loss, P_{DC} is equal to 8.8 W, at rated current.

- *Determine the high-frequency losses arising from the proximity and skin effects*: The high-frequency loss at the operating point can be determined by plotting the high-frequency resistance multiplier, $R_{\text{AC}}/R_{\text{DC}}$, as a function of winding thickness ratio, h/δ [15], where h is the winding thickness. AC resistance for this 16-layer high-current PCB design is found to be $\sim 5.36R_{\text{DC}}$, as indicated in Fig. 4*c*. Note that, the winding thickness ratio, $h/\delta = 0.2$, is much smaller than unity. The AC loss, P_{AChf}, can be calculated as 0.54 W from (16), which is much less than the DC loss due to the small magnitude of high-frequency current ripple, as expected

$$P_{\text{AChf}} = \Delta I_{\text{rms}}^2 R_{\text{AC}} \tag{16}$$

where ΔI_{rms} is the RMS value of the high-frequency ripple superimposed on the fundamental AC current.

- *Calculate total loss and temperature rise*: The total loss, P_{T}, is calculated from (17) as 19.48 W

$$P_{\text{T}} = P_{\text{core}} + P_{\text{DC}} + P_{\text{AChf}} \tag{17}$$

Finally, thermal performance of the design is checked by using the empirical expression [13] given in the following equation:

$$\Delta T = (P_{\text{T}}/\text{SA})^{0.833} \tag{18}$$

where P_{T} is in mW and SA denotes the surface area of the filter in cm^2. SA is calculated as 162 cm^2. Hence, the inductor temperature rise corresponding to this surface area is estimated as $\Delta T = 54$°C. Since the operational limit for PCB temperature is specified as 105°C, one can conclude that both the core and the PCB will remain within the safe operating range, for a maximum ambient temperature of 40°C.

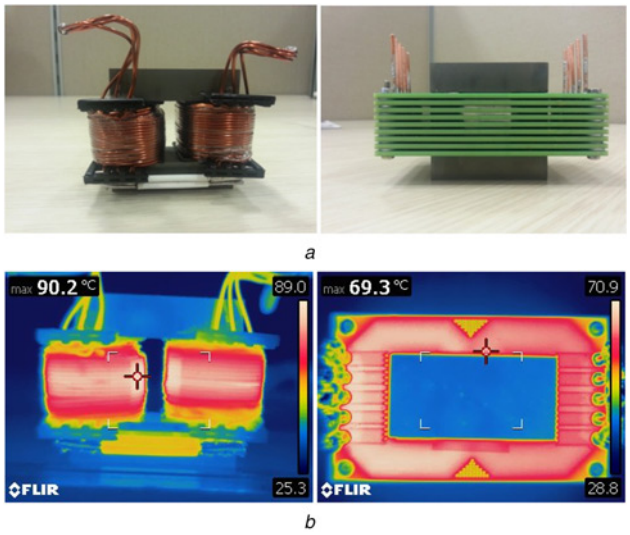

Fig. 5 *Thermal images of conventional wired inductor (left), paralleled multilayer high-current PCB inductor (right)*
a Implemented inductors
b Thermal images of front view for wired design, and top view for the multilayer high-current PCB design

3 Implementation of GaN inverter

3.1 Multilayer high-current PCB inductor

The thermal performance of this multilayer high-current PCB magnetics design, for the output inductor with 300 µH – 21.2 A RMS ratings, has been compared with that of the wired inductor design, using the same cores. The multilayer high-current PCB inductor and the wired inductor are presented in Fig. 5*a*. The measured parameters of both inductors are as given in Table 6. Both using the multilayer PCB and wired design approaches, same inductance values are obtained, with a higher but acceptable parasitic capacitance of the multilayer PCB winding design.

Nevertheless, wired design results in a lower DC resistance which corresponds to lower losses. In order to observe the temperature variation for both winding designs, a constant current of 30 A DC is supplied during 20 min to both inductors for the sake of thermal balance, and the temperature rise is observed. In order to be able to measure maximum temperature values, side view is taken for the wired inductor, while top view for the multilayer high-current PCB inductor.

As seen from Fig. 5*b*, the wired inductor reaches to a maximum temperature of $T_{ind} = 90°C$, at the ambient temperature of $T_{amb} = 24\,°C$, whereas the PCB inductor temperature reaches to only 69.3°C. Although both inductors are similar in dimensions, due to the increased surface area and air ducts between parallel-connected PCBs, the multilayer PCB inductor is expected to have a lower thermal resistance. Experimental verification indicates indeed that the temperature rise of the windings can be reduced by 32%, when the multilayer, high-current PCB magnetics design method is used. Note that, a lower temperature rise is obtained with the multilayer PCB winding even though higher power is dissipated. When the peak operating temperature values are considered for the worst-case ambient temperature, forced-air cooling would be required for the wired inductor, while natural-air-cooling is sufficient for the multilayer PCB design. Hence, by using the proposed multilayer PCB design, fan space is saved and system complexity is reduced, resulting in increased reliability and modularity.

Table 6 Inductor parameters comparison

	Resistance, mΩ	Inductance, µH	ΔT, °C	Parasitic capacitance, pF
wired inductor	14.0	301	66.2	30
PCB inductor	23.5	324	45.3	360

3.2 High-efficiency single-phase inverter

Before the implementation, three-dimensional (3D) model of the whole single-phase inverter is drawn in the Altium Designer PCB

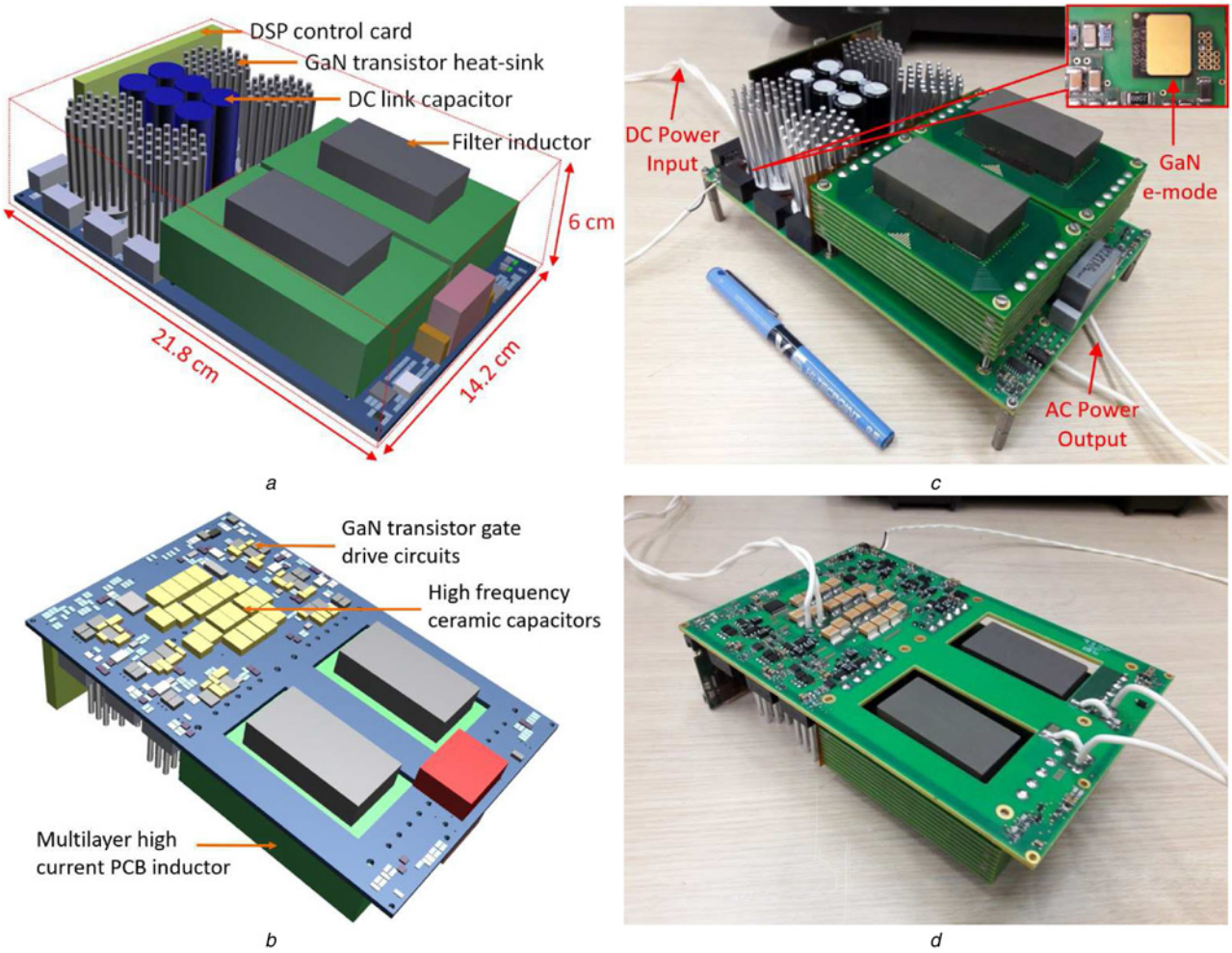

Fig. 6 *Implemented single-phase 5 kVA GaN inverter*
a 3D model top view
b 3D model bottom view
c Implemented inverter top view
d Implemented inverter bottom view

doi: 10.1049/joe.2017.0355

design computer program, as shown in Figs. 6*a* and *b*. In the top layer, DSP control card, GaN transistors (just under the heat sinks), DC-link capacitors, and PCB filter inductors are placed. Texas Instruments F28377D digital signal processor board is used as the microcontroller in the DSP control card. On the bottom side, electronic circuitry for GaN e-mode transistor gate drive and snubber capacitors is placed. Maximum dimensions of the resulting inverter are measured as 14.2 cm × 21.8 cm × 6 cm, which correspond to 2.7 W/cm^3 (44.3 W/inch^3) power density for a 5 kVA rated output power.

The implemented single-phase, 5 kVA GaN inverter and its dimensions are shown in Figs. 6*c* and *d*. Its mass is 2.3 kg. As seen from Fig. 6, a heat sink is used for the natural-air cooling of the GaN transistor, which is placed just on the top of each GaN transistor. The power loss for each transistor at 5 kVA output power, and 50 kHz switching frequency is 15.2 W. A heat sink with 4.5 K/W thermal resistance (Fischer Elektronik, ICK S R40 × 50) is selected to cool down the GaN transistor. Additionally, copper fills at the drain and source terminals of the GaN transistor supported with multiple via an electrical connection on the multilayer PCB further contributes cooling of the transistors. For this design, six pieces of 450 V, 220 µF electrolytic capacitors (Rubycon, 450VXG220MEFCSN30X30) are used in parallel to obtain the DC-link capacitor bank, which corresponds to a total input capacitance of $C1 = 1.32$ mF. Electrolytic capactiors cannot handle high-speed switching currents of the GaN transistor. For that purpose, 10 × 2 high-frequency ceramic capacitors (EPCOS, B58031I5105M2) are used in parallel with the electrolytic capacitors, as shown in Fig. 6*b*. Each high-frequency ceramic capacitor has 12 mΩ ESR and 2.5 nH ESL values. In the layout and trace connection phase of the PCB, a special effort is made to place high-frequency capacitors as close as possible to GaN transistors and connect them to the transistors with traces with the lowest impedance.

4 Experimental results

Technical specifications of the implemented system are given in Table 1. The associated measurements are taken by using Tektronix DPO 3034 oscilloscope. The current waveforms are measured using Tektronix TCP202 current probe, and the drain-to-source and gate-to-source voltages are measured by using 500 MHz voltage probes. For noise immunity of the measurements at high frequencies, the voltage probes are used with a tip ground clip connection. In addition to these, the dead-time value is set to 100 ns in order to minimise the power loss on GaN transistors, and the harmonic distortion on the output current waveform. AC output current and voltage waveforms are observed as shown in Fig. 7*a*, at full-load. Note that the single-phase inverter operates at a low-current total harmonic distortion value of 0.85%.

Inverter DC input voltage and current are also recorded in conjunction with the AC output voltage and current as shown in Fig. 7*b*. As seen from waveforms, there exists an oscillation superimposed on the DC current at double the output frequency (100 Hz). Due to these double line frequency oscillations at the DC input current, a voltage fluctuation is observed on the input voltage. With the properly chosen DC-link capacitance value, voltage oscillations are kept at operationally acceptable levels (<5% of 370 V DC). In order to illustrate the high switching speed and to calculate the transistor losses, switching waveforms of the GaN e-mode transistor are also observed. Turn-on and turn-off switching waveforms are presented in Figs. 7*c* and *d*, respectively. As seen from these waveforms, the drain-to-source voltage fall time during turn-on is 40 ns, while the drain-to-source

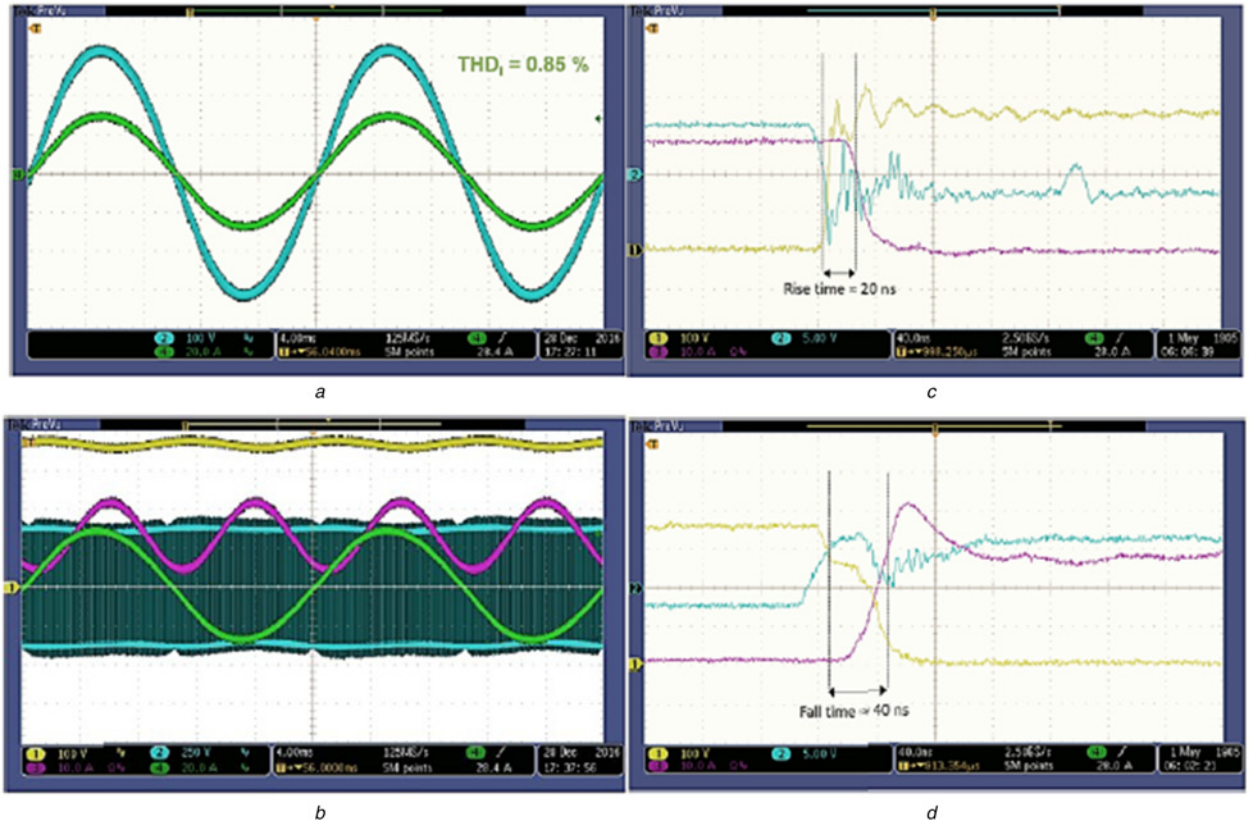

Fig. 7 *Single-phase GaN inverter electrical waveforms at full load*
a CH2: AC output voltage (100 V/div), CH4: AC output current (20 A/div)
b CH1: input voltage (100 V/div), CH2: leg-to-leg output voltage (250 V/div), CH3: input current (10 A/div), and CH4: output current (20 A/div)
c GaN transistor turn-off, CH1: drain-to-source voltage (100 V/div), CH2: gate-to-source voltage (5 V/div), CH3: drain current (10 A/div)
d GaN transistor turn-on, CH1: drain-to-source voltage (100 V/div), CH2: gate-to-source voltage (5 V/div), CH3: drain current (10 A/div)

doi: 10.1049/joe.2017.0355

voltage rise time during turn-off is around 20 ns. The difference in fall and rise times is a result of the asymmetrical gate drive circuitry. Turn-on is performed slower in order to limit the dv/dt and parasitic turn-on of the off-transistor due to the Miller effect. Still, dv/dt at turn-on and turn-off are 9.25 and 18.5 kV/µs, respectively. Switching energy loss is measured from the multiplication, and then integration of the drain current and drain-to-source voltage, during turn-on and turn-off. For turn-on, switching energy is measured as $E_{on} = 203$ µJ, and turn-off switching energy as $E_{off} = 62$ µJ, from Figs. 7*c* and *d*, respectively. The total loss for GaN transistors was calculated as 61.6 W. For the full-bridge inverter configuration, this corresponds to 15.4 W for each GaN transistor. Since the switching loss is taken as linearly proportional to the drain current for the same operating voltage, the experimental P_{SW} can be determined from (19), for 30 A peak AC output current. Using (19), for each cycle of AC output current, turn-on and turn-off losses for the k-pulses are summed up to find $P_{SW} = 8.5$ W for $f_{sw} = 50$ kHz and $f_s = 50$ Hz

$$P_{SW} = \sum_{k=0}^{k=f_{sw}/(2f_s)} (E_{on} + E_{off}) f_{sw} \sin(wk/f_{sw}) \quad (19)$$

Table 7 GaN transistor experimental loss breakdown

Transistor	Switching loss, W	Conduction loss, W	Total loss, W
GS66516T	8.5	6.9	15.4

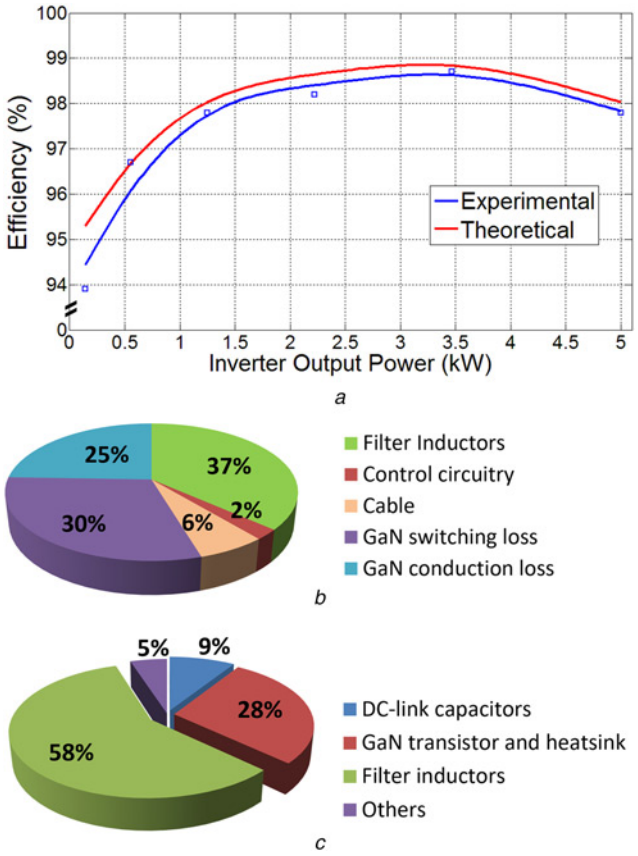

Fig. 8 *Performance parameters of the implemented 5 kVA single-phase GaN inverter*
a Inverter efficiency versus power plot
b Inverter loss distribution at full load
c Inverter volume distribution

The resulting loss breakdown for one transistor is given in Table 7. The small difference in conduction loss value between analytical calculations given in Table 5 and the implemented system is attributed to the R_{DSon} variation of the GaN transistor as a function of temperature. Thus, a verification of the RMS current and conduction loss expressions has been carried out. The inverter is operated at different load levels, and the corresponding efficiency values obtained are plotted in comparison with the theoretical values, as shown in Fig. 8*a*. At the full load, measured efficiency was 97.8%, which corresponds to a total loss of 112.5 W at 5 kVA output power. The graphical representation of the experimental loss distribution at full load is also plotted as given in Fig. 8*b*. In addition, inverter volume distribution is shown in Fig. 8*c*. The filter inductors and GaN transistor heat sinks constitute the major components that determine the total volume distribution.

5 Conclusion

In this paper, a high-efficiency, 5 kVA single-phase GaN inverter equipped with a new multilayer, high-current PCB magnetics, has been designed and implemented. For this purpose, a new design methodology has been proposed, which is based first on the analytical calculation of the transistor losses for the selection of optimum transistor and highest switching frequency pair in order to meet the target volume and efficiency, without running time-consuming computer simulations. Then, the multilayer, high-current PCB magnetics design concept has been introduced for a better cooling, easier manufacturing and standardisation of the output filter magnetics, as compared to the conventional wired magnetics design techniques. In this approach, multilayer PCBs are connected in parallel for the winding design by taking into account the skin and proximity effects, which are then combined with a sufficient number of core blocks joint together to form an application-specific, high-current, high-frequency magnetics design solution.

The proposed approach has been validated on the developed, natural-air-cooled, 5 kVA single-phase inverter operating at 230 V AC output voltage, with a power density of 2.7 W/cm^3 (44.3 W/inch^3), and a full-load efficiency of 98%. Fifty-five per cent of the total loss comes from GaN transistors, and 37% from the output filter. Note that more than half of the total inverter volume is occupied by the output filter, and nearly one third by the GaN transistors and their heat sinks. It has been also experimentally verified that the temperature rise of the magnetics design is reduced by 32% with the application of the proposed multilayer, high-current PCB magnetics. As a result, natural-convection cooling is found to be adequate with the proposed magnetics design concept, while forced-air cooling would be required in the case of a conventional wired inductor design approach in order to meet the target power density for this application.

6 Acknowledgments

The authors acknowledge Aselsan Incorporation and Hacettepe University Scientific Research Projects Coordination Unit for the financial support given to this project (project no. FHD-2016–10910).

7 References

[1] Xue Y., Divya K. C., Griepentrog G., *ET AL.*: 'Towards next generation photovoltaic inverters'. 2011 IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, USA, 2011, pp. 2467–2474
[2] Seki Y., Hosen T., Yamazoe M.: 'The current status and future outlook for power semiconductors', *FUJI Electr. Rev.*, 2010, **56**, (2), pp. 47–50
[3] Kim T., Jang M., Agelidis V.G.: 'Practical implementation of a silicon carbide-based 300 kHz, 1.2 kW hard-switching boost-converter and comparative thermal performance evaluation', *IET Power Electron.*, 2015, **8**, (3), pp. 333–341
[4] León-Masich A., Valderrama-Blavi H., Bosque-Moncusí J.M., *ET AL.*: 'Efficiency comparison between Si and SiC-based implementations

in a high gain DC–DC boost converter', *IET Power Electronics*, 2015, **8**, (6), pp. 869–878
[5] 'Little Box challenge', https://www.littleboxchallenge.com, accessed 1 February 2017
[6] 'Compact fans- ebmpapst Products', 2016, http://www.ebmpapst.com/media/content/infocenter/downloads_10/catalogs/compactfansen2011/Compact_fans_for_AC_and_DC_2016_01_US.pdf
[7] Morsy A.S., Bayern M., Enjeti P.: 'High power density single phase inverter using GaN FETS and active power decoupling for google little box challenge'. 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, USA, 2015, pp. 323–327
[8] Gurpinar E., Castellazzi A.: 'Single-phase T-type inverter performance benchmark using Si IGBTs, SiC MOSFETs, and GaN HEMTs', *IEEE Trans. Power Electron.*, 2016, **31**, (10), pp. 7148–7160
[9] Morsy A.S., Enjeti P.N.: 'Comparison of active power decoupling methods for high-power-density single-phase inverters using wide-bandgap FETs for google little box challenge', *IEEE J. Emerg. Sel. Topics Power Electron.*, 2016, **4**, (3), pp. 790–798
[10] Hu H., Harb S., Kutkut N., *ET AL.*: 'A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems', *IEEE Trans. Power Electron.*, 2013, **28**, (6), pp. 2711–2726
[11] Gu B., Dominic J., Lai J.S., *ET AL.*: 'High reliability and efficiency single-phase transformerless inverter for grid-connected photovoltaic systems', *IEEE Trans. Power Electron.*, 2013, **28**, (5), pp. 2235–2245
[12] Mohan N., Undeland T.M., Robbins W.P.: 'Power electronics: converters, applications and design', Chapter 30, section 30-5-1, page 760, Equation (30-23) (Wiley Press, 2003, 3rd edn.)
[13] '2015 magnetics powder core catalog', http://www.mag-inc.com/../2015-Magnetics-Powder-Core-Catalog.pdf, accessed 1 February 2017
[14] Hu J., Sullivan C.R.: 'AC resistance of planar power inductors and the quasi distributed gap technique', *IEEE Trans. Power Electron.*, 2001, **16**, (4), pp. 558–567
[15] Iyer K.V., Robbins W.P., Mohan N.: 'Design and comparison of high frequency transformers using foil and round windings'. 2014 Int. Power Electronics Conf. (IPEC-Hiroshima 2014 – ECCE ASIA), Hiroshima, Japan, 2014, pp. 3037–3043