QCA circuit design of *n*-bit non-restoring binary array divider

Amjad F. Almatrood, Harpreet Singh

Department of Electrical and Computer Engineering, Wayne State University, Detroit, MI 48202, USA
E-mail: amjad.almatrood@wayne.edu

Published in *The Journal of Engineering*; Received on 6th September 2017; Revised on 5th March 2018; Accepted on 7th March 2018

Abstract: The physical limitations of complementary metal-oxide semiconductor (CMOS) technology have led many researchers to consider other alternative technologies. Quantum-dot cellular automate (QCA) is one of the nanotechnologies that is being considered as possible replacements for CMOS. In this paper, a QCA circuit for an *n*-bit non-restoring binary array divider (NRD) is designed. The proposed divider is developed using multi-layer and a QCA structure of the three-input XOR function. Compared to the previously proposed QCA designs for NRD, the proposed design provides further reduction in cell count, latency, and area. The results for a 3 × 3 NRD show that the proposed design enables 14.8, 14.8, and 20.3% reductions in cell count, latency, and area, respectively. In addition, the proposed 4 × 4 divider achieves 5.5, 18.8, and 33.1% reductions in cell count, latency, and area, respectively, compared to the existing designs.

1 Introduction

The complementary metal-oxide semiconductor (CMOS) technology has played a vital role in constructing integrated systems for the past four decades. This technology has provided the requirements of implementing high-density, high-speed, and low-power very large-scale integrated systems. However, the fundamental physical limits of this technology have been reached [1]. Many researches have introduced different nanotechnologies such as quantum-dot cellular automate (QCA) [2–7]. QCA technology is being considered as possible replacements for CMOS technology and is expected to provide further scaling down of feature sizes and other features of integrated systems.

In QCA technology, the process of computation and information transformation is done using a new paradigm. The binary values are encoded depending on the charge configurations of the QCA cells. In a QCA cell, there are two possible polarisations of charge configurations. These polarisations are used to represent logic 0 and 1. In CMOS technology, logic NAND, NOR, and NOT gates are the basic units used to implement circuits. However, QCA uses majority gates and inverters as the circuit primitives. The QCA capability that results in high-speed, high-density, and ultralow-power integrated systems has attracted many researchers to consider such a technology.

The implementation of QCA-based circuits for various arithmetic logic units have been investigated. Up to date, several papers have proposed different QCA designs for different arithmetic units such as squarer [8], square rooting circuit [9], divider [10], and multiplier [11]. However, due to the major impact of the divider circuits on the overall performance of any arithmetic processor, they are the most complicated units. Different QCA designs for divider circuits such as restoring binary array divider (RD) [12–14] and non-restoring divider (NRD) [14–17] have been proposed. The designs of NRDs show that they are better compared to RDs because of the drawbacks of RDs such as resorting process and realising control logic, which cause more delay, unnecessary power dissipation, and larger sizes.

In the literature, several QCA-based circuits for the non-restoring binary array divider have been introduced based on different techniques [14–17]. The dividers in [14, 15, 17] were designed with a single-layer QCA as in [15] or multi-layer as in [14, 17] based on only majority gates and inverters. Recently, a QCA design for NRD was proposed based on the QCA structure of the XOR function [16]. In this design, the Boolean functions are realised using XOR gates, majority gates, and inverters. However, this divider is designed using a single layer. In this paper, a QCA design of *n*-bit non-restoring binary array divider using multi-layer is proposed. In addition, the design is developed based on a QCA structure of the three-input XOR function. Different papers have introduced different QCA structures of the three-input XOR function [18–20]. However, the proposed design of non-restoring binary array is developed using the XOR structure given in [18]. This structure is designed in a single layer and it requires less number of QCA cells, less clock cycles, and smaller area. This leads to a QCA design of non-restoring binary array divider with better results in view of cell count, latency, and area, compared to the existing designs.

The remainder of this paper is organised as follows. In the next section, some background material of QCA technology, non-restoring binary array divider, and the fundamental unit of NRD are given. The proposed QCA design is discussed in detail in Section 3. The simulation results and a comparison between the proposed design and the existing designs are given in Section 4. Lastly, the conclusion remarks are given in Section 5.

2 Background material

2.1 QCA technology

In QCA, the fundamental unit used for implementing circuits is QCA cell. This cell contains four quantum dots located at corners of a square which can be charged with two free electrons that tunnel between the dots. These electrons occupy diagonal sites because of Coulombic interactions. Thus, there are only two configurations of an electron pair that are energetically stable states in a QCA cell. These two configurations are indicated as cell polarisation $P = +1$ and $P = -1$ to represent logic 1 and logic 0, respectively. A QCA cell and its two possible electrons configurations are shown in Fig. 1.

The fundamental devices used for implementing logic circuits in QCA are QCA wire, QCA inverter, and QCA majority logic gate. A QCA wire is constructed of a group of QCA cells placed next to each other as shown in Fig. 2*a*. The binary signal propagates along the wire form input which is the leftmost cell with a fixed polarisation to the rightmost cell which is the output [21]. The signal flow can be directed based on QCA clock [22].

A QCA inverter is implemented by placing cells diagonal to each other. This special structure results in reverse polarisations of these cells. The layout of a QCA inverter is shown in Fig. 2*b*.

A QCA majority gate implements a three-input logic function as given in (1). This function produces logic 1 as an output if two or more of its inputs are 1. Otherwise, it produces an output 0. Fig. 2*c*

doi: 10.1049/joe.2017.0375

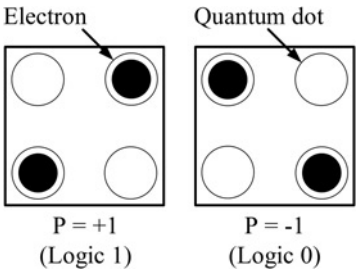

Fig. 1 *QCA cell with its possible electrons configurations*

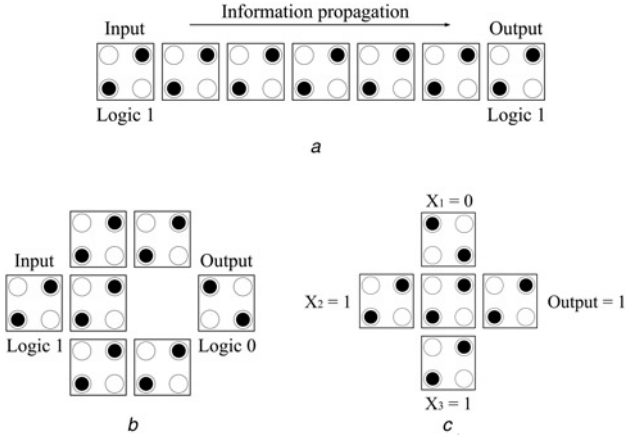

Fig. 2 *QCA devices*
a QCA wire
b QCA inverter
c QCA majority gate

shows the simple diagram of a QCA majority gate. The polarisation of the cell in the middle is determined by the surrounding inputs cells. In other words, the middle cell follows the majority polarisations of surrounding inputs cells because it represents the lowest energy state. The signal is then transferred to the output cell

$$M(x_1, x_2, x_3) = x_1x_2 + x_1x_3 + x_2x_3 \tag{1}$$

2.2 Complement adder/subtractor cell

The basic unit in the non-restoring binary array divider is the complement adder/subtractor (CAS) cell. In this cell, there are four inputs: A_i, B_i, P, and C_i, and two outputs: S_i and C_0 as shown in Fig. 3. The functions of this cell can be expressed by

$$\left.\begin{aligned} S_i &= A_i \oplus (B_i \oplus P) \oplus C_i \\ C_0 &= A_i(B_i \oplus P) + A_iC_i + (B_i \oplus P)C_i \end{aligned}\right\} \tag{2}$$

From these expressions, it can be noted that the CAS unit is basically an XOR function and a 1-bit full adder. The first two inputs of the full adder are A_i, C_i and the third input is the output of $B_i \oplus P$. As for the outputs of the CAS cell, they are S_i for the sum and C_0 for the carry.

2.3 Non-restoring binary array divider

The division process of the non-restoring binary array is done by calculating the partial reminders by subtracting or adding the dividend and the right-shifted versions of the divisor. Based on the sign

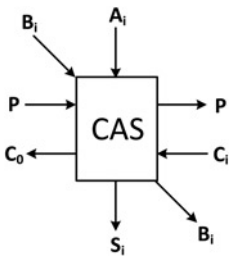

Fig. 3 *CAS cell*

of the calculated partial reminder, the quotient bit is determined. The sign of the partial reminder is also used to decide whether the shifted divisor has to be added or subtracted in the next cycle. The process of NRD is defined in [15, 23] as follows:

$$q_{i+1} = \begin{cases} 1 & \text{if } R_i > 0 \\ 0 & \text{if } R_i < 0 \end{cases} \tag{3}$$

$$R_{i+1} = \begin{cases} 2R_i - y & \text{if } R_i > 0 \\ 2R_i + y & \text{if } R_i < 0 \end{cases} \tag{4}$$

$$r = \begin{cases} 2^{-n} \cdot R_n & \text{if } R_i > 0 \\ 2^{-n} \cdot (R_n + y) & \text{if } R_i < 0 \end{cases} \tag{5}$$

where n is the number of bits, i the iteration index : $\{i \to 1, 2, \ldots, n-1\}$, q_i the quotient set, R_i the partial reminder after ith iteration, y the divisor, and r the final reminder.

By a two-dimensional array of pipelined CAS cells, the NRD can be designed to perform the division operation for any number of bits. For an n-bit NRD, the array requires n^2 CAS cells. Fig. 4 shows a 5×5 non-restoring binary divider. This array can divide an 8-bit number $(x_1x_2x_3x_4x_5x_6x_7x_8)$ by a 4-bit number $(y_1y_2y_3y_4)$. For the result, a 5-bit quotient $(q_0q_1q_2q_3q_4)$ is produced at the left side of the array and a 5-bit reminder $(r_4r_5r_6r_7r_8)$ is produced at the bottom of the array.

3 Design and implementation

As mentioned earlier, the basic unit in QCA technology is a majority gate. Therefore, in order to implement a logic circuit in QCA, the Boolean function has to be converted into its equivalent majority logic circuit. Different majority logic circuit synthesis methods have been introduced. However, for some cases, when converting a Boolean function into its equivalent majority-based circuit, the circuit requires more gates and levels compared to its original

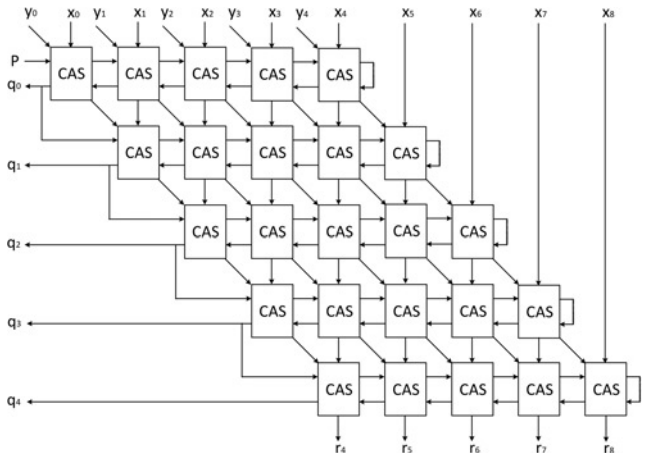

Fig. 4 *5 × 5 non-restoring binary array divider*

doi: 10.1049/joe.2017.0375

Boolean function. In any QCA circuit, the number of gates and levels are the most important factors that affect the performance of the circuit since they determine the complexity and latency. Therefore, in order to have an efficient QCA design of non-restoring binary divider, the numbers of gates and levels have to be reduced.

In this paper, the proposed QCA design for non-resorting divider is developed using a QCA structure of the three-input XOR function introduced in [18]. Using this structure with majority gates to design a QCA circuit can provide further reduction in cell count, latency, and area. For example, consider the three-input XOR function, i.e. $F = x_1x_2x_3 + x_1'x_2'x_3 + x_1x_2'x_3' + x_1'x_2x_3'$. In order to implement this function in QCA, three majority gates and three inverters are required, i.e. $F = M(M(x_1', x_2, x_3), M(x_1, x_2', x_3), x_3')$ [24]. However, this function can be directly implemented in QCA using only one gate as shown in Fig. 5. In addition, this structure requires one level, whereas the equivalent majority circuit requires two levels.

As given in the previous section, a CAS cell is essentially an XOR function and a 1-bit full adder. Since the carry of the full adder is a majority function, the CAS cell can be realised using two XOR gates and one majority gate as shown in Fig. 6*a*. This circuit can be directly implemented in QCA using the same number of gates and levels. It can be noted that the XOR function of inputs B_i and P can be realised using the three-input XOR gate by fixing the third input to logic 0. Fig. 6*b* shows the QCA design of the CAS cell.

In the CAS circuit, the longer path is from inputs B_i and P and output C_0. This path is basically the majority function of A_i, C_i, and the output of XOR function of B_i and P, i.e. $M(A_i, C_i, (B_i \oplus P))$. From Fig. 6*b*, it can be noted that this path requires 0.5 clock cycle for the XOR gate and 0.25 for the majority gate. Therefore, the overall delay of this circuit is 0.75 clock cycle.

In this paper, the proposed QCA designs for CAS cell and divider are developed using multi-layer QCA. For most cases, circuits designed in QCA using multi-layer require more QCA cells compared to that designed with a single-layer. However, multi-layer can provide better results in view of area and latency. In addition, due to the routing complexity of the single layer, multi-layer can give better designs that require less cells, especially while designing large circuits. The QCA design of the CAS cell given in Fig. 6*b* is developed using three different layers, i.e. main layer, layer 1, and layer 2. These layers are shown in Figs. 7*a*–*c*, respectively.

Based on the QCA design of the CAS cell, the non-restoring binary array divider can be implemented to perform the division operation for any number of bits. Fig. 8 shows the proposed QCA design of a 3 × 3 NRD. From the design, it can be noted that two CAS cells named red and white are used as shown in the red rectangles. These cells are designed with different clocks in order to have less clock cycles of the divider. To illustrate this point, consider the QCA design of CAS cell given in Fig. 6*b*. The inputs of this cell are given in the first quarter of the clock cycle (clock 0) and the outputs are received in the third quarter (clock 2). Therefore, in order to connect this cell to another cell with the same clocks, there is an additional 0.25 clock cycle required. However, by designing the next cell to receive the inputs in the third quarter, the output of the previous cell can be directly connected to the next cell. Based on that, the divider is designed by placing and connecting these cells to each other such that none of these cells is connected to another cell with the same clocks. In addition, the first cell in each row (the most right cell)

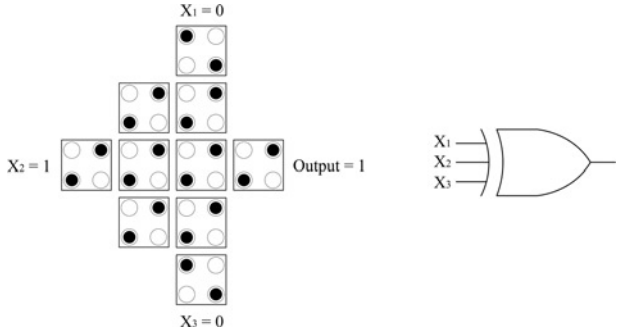

Fig. 5 *QCA three-input XOR gate*

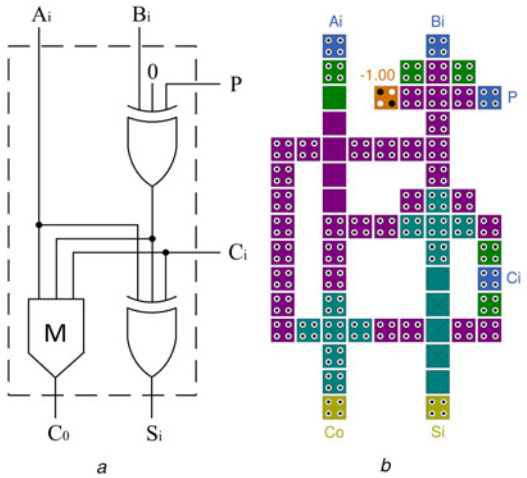

Fig. 6 *CAS cell*
a Logic diagram
b QCA layout

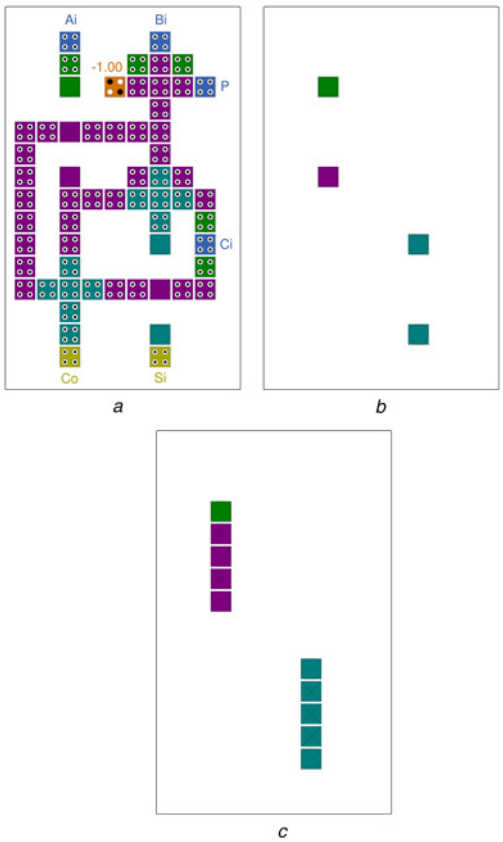

Fig. 7 *Multi-layer QCA for CAS cell*
a Main layer
b Layer 1
c Layer 2

doi: 10.1049/joe.2017.0375

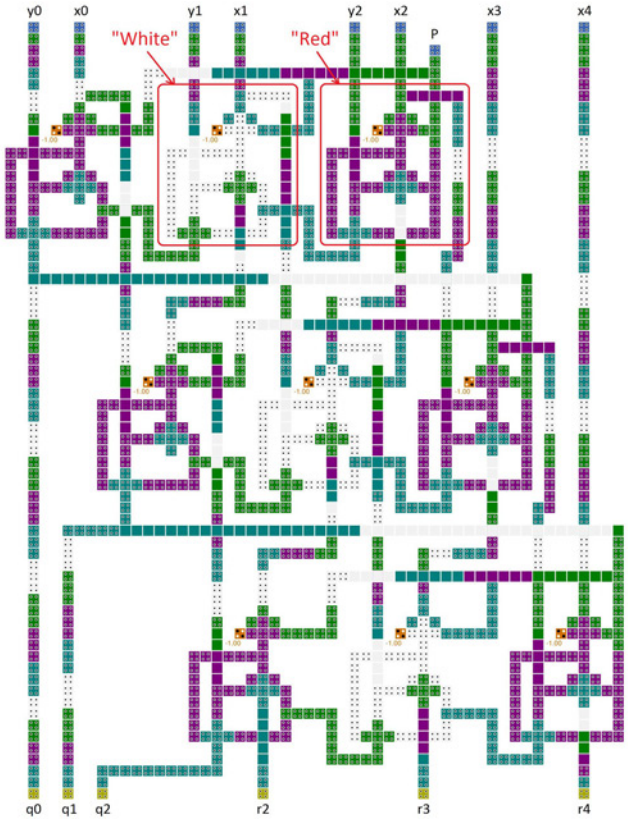

Fig. 8 *QCA layout for a* 3 × 3 *NRD*

should have the same clocks of the last cell of the previous row (the most left cell), whereas the first cell in the first row is always red. This provides 0.5 clock cycle for connecting q_i to the next row, while one full cycle is required if these two cells have the same clock cycles. Fig. 9 shows the patterns of CAS cells for 3-, 4-, 5-, and 8-bit NRD. To illustrate the implementation of the proposed divider, we have considered the implementation of 4×4 and 5×5 NRD as shown in Figs. 10*a* and *b*.

The latency of an n-bit restoring and non-restoring binary array divider can be determined by $4n^2 + 1$ [12] and $3n^2 - 0.75$, respectively. Recently, a QCA NRD was proposed with a latency of $3n^2/4$ [16]. In the proposed design, the QCA divider for an n-bit array achieves an overall latency of

$$\text{Delay} = \frac{2n(n+1)-1}{4}. \tag{6}$$

In the implemented NRDs, $n = 3$, $n = 4$, and $n = 5$. Thus, the overall delay of these dividers are 5.75, 9.75, and 14.74 clock cycles, respectively. Fig. 11 shows the latency of restoring divider, NRD, and the proposed divider.

4 Results and comparison

In this paper, the designs and simulation are done using QCADesigner version 2.0.3 [25]. The layers properties used in the designs are as follows: the cells area is 18 nm × 18 nm, and the diameter of the dots is 5 nm. The parameters used for a simulation engine in the bistable approximation are as follows: the number of samples is 12,800, convergence tolerance is 0.001, radius of effect is 65 nm, relative permittivity is 12.9, clock high and clock low are 9.8×10^{-22} and 3.8×10^{-23} J, respectively, clock amplitude factor is 2, layer separation is 11.5 nm, and maximum iterations per sample is 100. For the coherence vector engine, the parameters are as follows: temperature is 1 K, relaxation time is 1.0×10^{-15} s, time step is 1.0×10^{-16} s, clock high and clock low are 9.8×10^{-22} and 3.8×10^{-23} J, respectively, clock shift is 0, clock amplitude factor is 2.0, radius of effect is 80 nm, relative permittivity is 12.9, and layer separation is 11.5 nm.

Fig. 12 shows the simulation results for the CAS cell. From the figure, it can be observed that the signals are received at the output cells after 0.75 clock cycle. Compared to the existing QCA dividers, this delay is the same as the best existing design in [16]. The proposed QCA design of CAS cell has a total of 74 QCA cells and an area of 0.07 μm^2. A comparison of QCA specifications between the proposed design and the best existing designs for the CAS unit is given in Table 1. From the table, it can be noted that since the proposed CAS unit is designed using multi-layer, the QCA circuit has a total of 74 cells, whereas the best existing design has 60 cells. However, the proposed design has a smaller area, i.e. 0.07 μm^2.

Even though the proposed CAS unit requires more QCA cells compared to the single-layer design, the overall design of

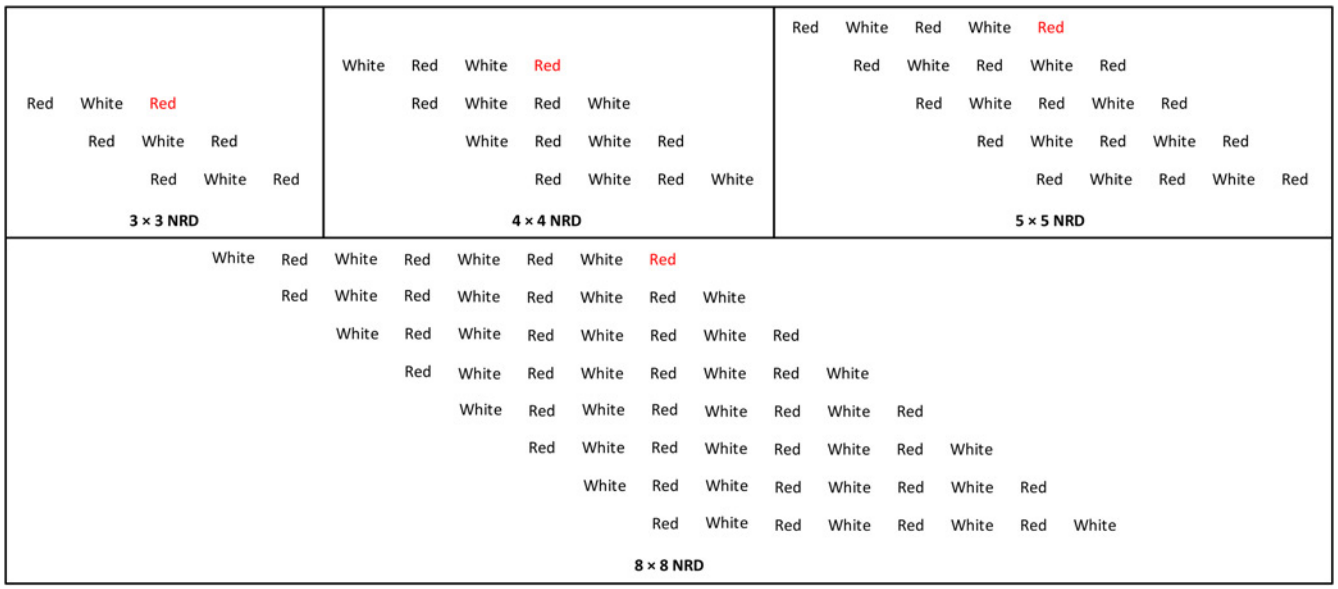

Fig. 9 *Pattern of CAS cells for different sizes of NRD*

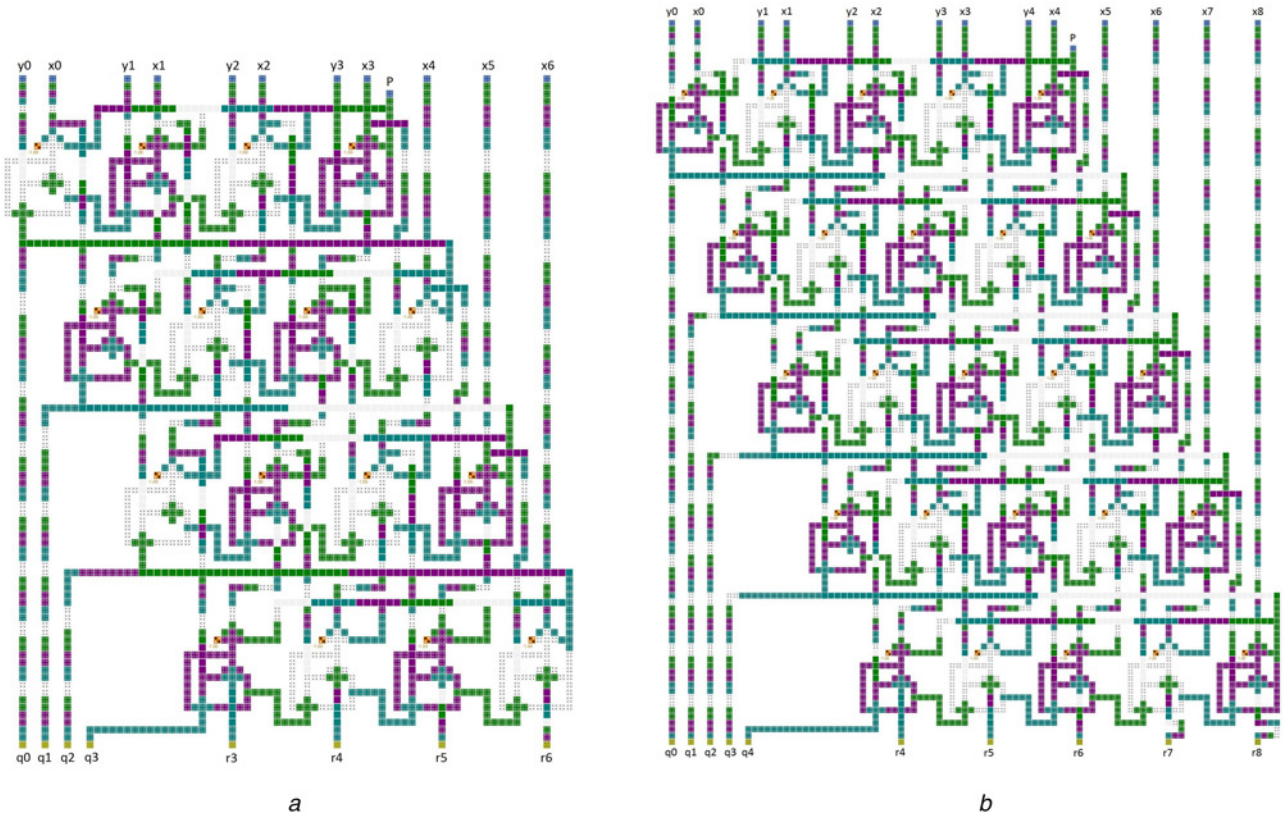

Fig. 10 *QCA layout for*
a 4 × 4 NRD
b 5 × 5 NRD

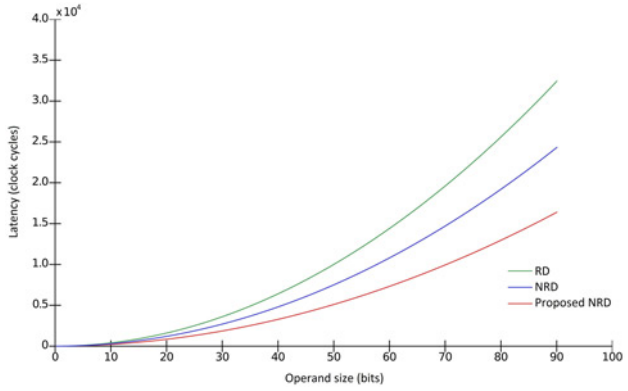

Fig. 11 *Latency of RD, NRD, and the proposed NRD*

non-restoring binary array divider requires fewer QCA cells, clock zones, and smaller area. The proposed designs of 3 × 3 and 4 × 4 dividers have a total of 1436 and 2791 QCA cells and area of 1.53 and 2.81 μm^2, respectively. In Table 2, a comparison between the proposed non-restoring binary dividers and the best existing designs are given. From the table, it can be observed that the proposed design has better results in view of cell count, latency, and area. Compared to the designs in [16, 17], the proposed 3 × 3 divider achieves 14.8, 14.8, and 20.3% reductions in cell count, latency, and area, respectively. In addition, the proposed 4 × 4 divider achieves 5.5, 18.8, and 33.1% reductions in cell count, latency, and area, respectively. In the same table, the QCA specifications for 5 × 5 divider are also given. This design has a total of 4313 QCA cells and an area of 4.58 μm^2.

Fig. 12 *Simulation results for the CAS cell*

doi: 10.1049/joe.2017.0375

Table 1 Comparison of QCA designs for a CAS cell

CAS cell	Cell count	Latency	Area, μm^2	Layer type
[14]	235	1.75	0.35	multi-layer
[15]	147	2.25	0.27	coplanar
[16]	60	0.75	0.08	coplanar
proposed	74	0.75	0.07	multi-layer
reduction % (w.r.t [16])	−23.3%	00.0%	12.5%	—

Table 2 Comparison of QCA designs for different dividers

Divider array	Cell count	Latency	Area, μm^2	Layer type
3 × 3 RD [12]	6451	37	15.05	coplanar
3 × 3 NRD [15]	3742	26.25	6.22	coplanar
3 × 3 NRD [16]	1686	6.75	3.4	coplanar
3 × 3 NRD [17]	1852	31	1.92	multi-layer
proposed 3 × 3	1436	5.75	1.53	multi-layer
reduction % (w.r.t [16])	14.8%	14.8%	55.0%	—
reduction % (w.r.t [17])	22.5%	81.5%	20.3%	—
4 × 4 RD [14]	5351	16.5	15.51	multi-layer
4 × 4 NRD [14]	5124	15.25	9.99	multi-layer
4 × 4 NRD [15]	6865	47.25	10.95	coplanar
4 × 4 NRD [16]	3180	12	6.5	coplanar
4 × 4 NRD [17]	2954	44	4.2	multi-layer
proposed 4 × 4	2791	9.75	2.81	multi-layer
reduction % (w.r.t [16])	12.2%	18.8%	56.8%	—
reduction % (w.r.t [17])	5.5%	77.8%	33.1%	—
proposed 5 × 5	4313	14.75	4.58	multi-layer

5 Conclusion

Owing to the physical limitations of CMOS technology, many emerging nanoscale technologies such as QCA have been proposed and considered as possible replacements for CMOS. In this paper, a QCA design for an *n*-bit non-restoring binary array divider is presented. The divider is developed based on a QCA structure of the three-input XOR function in order to have a QCA design with less number of gates and levels. In addition, the proposed divider is designed using multi-layer QCA. Compared to the existing QCA design of NRD, the proposed design results in less number of QCA cells, less clock frequency, and smaller area.

6 References

[1] '2013 International technology roadmap for semiconductors (ITRS)'. Available at: www.semiconductors.org

[2] Lent C.S., Tougaw P.D., Porod W., *ET AL.*: 'Quantum cellular automata', *Nanotechnology*, 1993, **4**, (1), p. 49

[3] Tougaw P.D., Lent C.S.: 'Logical devices implemented using quantum cellular automata', *J. Appl. Phys.*, 1994, **75**, (3), pp. 1818–1825

[4] Lent C.S., Tougaw P.D.: 'A device architecture for computing with quantum dots', *IEEE Proc.*, 1997, **85**, (4), pp. 541–557

[5] Porod W.: 'Quantum-dot devices and quantum-dot cellular automata', *Int. J. Bifurcation Chaos*, 1997, **7**, (10), pp. 2199–2218

[6] Snider G., Orlov A., Amlani I., *ET AL.*: 'Quantum-dot cellular automata: review and recent experiments', *J. Appl. Phys.*, 1999, **85**, (8), pp. 4283–4285

[7] Walus K., Jullien G.A., Dimitrov V.S.: 'Computer arithmetic structures for quantum cellular automata'. Proc. 37th Asilomar Conf. Signals, Systems and Computers, November 2003, pp. 1435–1439

[8] Giannou O., Vergos H.T., Bakalis D.: 'Squarers in QCA nanotechnology'. Proc. 12th IEEE. Conf. Nanotechnology (IEEE-NANO), Birmingham, UK, August 2012, pp. 1–6

[9] Jahangir M., Sheikhfaal S., Angizi S., *ET AL.*: 'Designing nanoelectronic-compatible 8-bit square root circuit by quantum-dot cellular automata'. IEEE Int. Symp., Nanoelectronic and Information Systems (iNIS), Indore, India, 2015, pp. 23–28

[10] Kong I., Kim S-W., Swartzlander E.: 'Design of Goldschmidt dividers with quantum-dot cellular automata', *IEEE Trans. Comput.*, 2014, **63**, (10), pp. 2620–2625

[11] Cho H., Swartzlander E.E.: 'Adder and multiplier design in quantum-dot cellular automata', *IEEE Trans. Comput.*, 2009, **58**, (6), pp. 721–727

[12] Kim S-W., Swartzlander E.E.: 'Restoring divider design for quantum-dot cellular automata'. Proc. 11th IEEE. Conf. Nanotechnology (IEEE-NANO), Portland, OR, USA, 2011, pp. 1295–1300

[13] Almatrood A, Singh H.: 'Design of generalized pipeline cellular array in quantum-dot cellular automata', *IEEE Comput. Arch. Lett.*, 2018, **17**, (1), pp. 29–32, doi: 10.1109/LCA.2017.2719021

[14] Sayedsalehi S., Azghadi M.R., Angizi S., *ET AL.*: 'Restoring and non-restoring array divider designs in quantum-dot cellular automata', *Inf. Sci.*, 2015, **311**, pp. 86–101

[15] Cui H., Cai L., Yang X., *ET AL.*: 'Design of non-restoring binary array divider in quantum-dot cellular automata', *Micro Nano Lett.*, 2014, **9**, (7), pp. 464–467

[16] Sasamal T.N., Singh A.K., Ghanekar U.: 'Design of non-restoring binary array divider in majority logic-based QCA', *Electron. Lett.*, 2016, **52**, (24), pp. 2001–2003

[17] Mohammadi M., Gorgin S., Mohammadi M.: 'Design of non-restoring divider in quantum-dot cellular automata technology', *IET Circuits Devices Syst.*, 2017, **11**, (2), pp. 135–141

[18] Ahmad F., Bhat G.M., Khademolhosseini H., *ET AL.*: 'Towards single layer quantum-dot cellular automata adders based on explicit interaction of cells', *J. Comput. Sci.*, 2016, **16**, pp. 8–15

[19] Bahar A.N., Waheed S., Hossain N., *ET AL.*: 'A novel 3-input XOR function implementation in quantum dot-cellular automata with energy dissipation analysis', *Alexandria Eng. J.*, 2017, doi: 10.1016/j.aej.2017.01.022

[20] Chabi A.M., Roohi A., DeMara R.F., *ET AL.*: 'Cost-efficient QCA reversible combinational circuits based on a new reversible gate'. 18th CSI Int. Symp. on Computer Architecture and Digital Systems, IEEE, Tehran, Iran, 2015, pp. 1–6

[21] Orlov A.O., Amlani I., Toth G., *ET AL.*: 'Experimental demonstration of a binary wire for quantum-dot cellular automata', *Appl. Phys. Lett.*, 1999, **74**, (19), pp. 2875–2877

[22] Orlov A.O., Amlani I., Kummamuru R.K., *ET AL.*: 'Experimental demonstration of clocked single-electron switching in quantum-dot cellular automata', *Appl. Phys. Lett.*, 2000, **77**, (2), pp. 295–297

[23] Cappa M., Hamacher V.C.: 'An augmented iterative array for high-speed binary division', *IEEE Trans. Comput.*, 1973, **100**, (2), pp. 172–175

[24] Zhang R., Walus K., Wang W., *ET AL.*: 'A method of majority logic reduction for quantum cellular automata', *IEEE Trans. Nanotech.*, 2004, **3**, (4), pp. 443–450

[25] Walus K., Dysart T.J., Jullien G.A., *ET AL.*: 'QCA designer: a rapid design and simulation tool for quantum-dot cellular automata', *IEEE Trans. Nanotech.*, 2004, **3**, (1), pp. 26–31