One current adaptive switching strategy for DC/DC converter with spike limitation

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Abstract: In this study, a new current adaptive switching strategy with the spike limitation applied in DC/DC converter is proposed. With this switching strategy, the switching speed of the power switch can be regulated adaptively with the change of the load. The turn-on/turn-off current is inversely proportional to the load. So, at the light load, the switching speed of the power switch is faster and the switching losses are lower. In addition, all of the control should be based on one principle that the current/voltage spike across power switch under a smaller load cannot exceed that under a rated load. The switching characteristics of power switch with the proposed switching strategy and the relationship between current/voltage spike, turn-on/turn-off current and power loop stray inductance during the switching transition is discussed in this study. Moreover, the drive circuit is designed in detail. Finally, a boost converter prototype with 200 V_{DC} input voltage/380 V output voltage/1 kW output power is established to verify the proposed method. The tested results show that the efficiency of the converter adopted the proposed method rises by 1.5% comparing with that used a conventional switching strategy at the light load.

1 Introduction

As it forms a crucial and integral part of a power converter, the gate-driver should be paid more attention to. It has a great influence on the switching speed, switching losses, current and voltage variations (di/dt and du/dt), the efficiency and electromagnetic interference (EMI) of the converter [1–3]. In recent years, a lot of work regarding the gate-drivers has been done and it mainly focuses on the drive capability, drive speed, isolated power supply and effective switching in [4–8], which most commonly utilises the conventional voltage source drivers (VSDs). However, VSDs have a defect that all the gate-drive energy dissipated through the drive resistance R_g and the fixed-drive voltage could not optimise the power losses of the power switch.

As the frequency of power switch increases, the power losses of the drive circuit cannot be ignored, so different resonant gate-drivers (RGDs) [9, 10] have been proposed to recycle gate energy losses in the VSDs. The review on the RGD techniques and its assessment in low-power DC/DC converters are presented in [11, 12]. The design method and general circuit are proposed in [13, 14]. The RGDs are especially impactful for the synchronous rectifier (SR) of buck converters, because the SR is designed with large gate charge to reduce the conduction losses. Nevertheless, it is noted that the RGDs emphasise to reduce the gate losses, while they can hardly reduce the dominant switching losses for high-frequency converter, so the efficiency improvement potentials of the RGDs converter is limited.

To improve the performance of RGDs, the current-SDs (CSDs) are reported in [15, 16]. CSDs can reduce the dominant switching losses by generating the constant drive current to charge and discharge the gate capacitance of the power switch, which will accelerate the switching speed. The present CSDs usually use constant drive current and voltage. Thus, if the drive current is stronger, the switching losses will be lower. However, higher drive current normally leads to higher gate-drive circuit losses, so the switching losses reduction and gate-drive circuit losses are needed to be compromised in design of the CSDs. To optimise this issue, the 'adaptive drive current' concept is proposed to weigh the switching losses and drive circuit losses dynamically in [17, 18], but they ignore the problem that the stronger drive current not only means the faster switching speed, but also means higher spike during the switching transition, which lead to the problem of EMI. In addition, though the current/voltage variations (di/dt and du/dt) can be controlled and adjusted in [19, 20], they lose the merits of the CSD. Meanwhile, the sensing circuit and the drive logic are complex to realise. In [21, 22], a real-time variable turn-off current strategy for a power factor correction (PFC) converter with voltage spike limitation and efficiency improvement, but it only discusses the turn-off transient. Infineon has launched the slew rate control insulated gate bipolar transistor driver integrated circuit (IC) EiceDRIVER™ [23], which behaves similar as a traditional driver at level 11 and controls the voltage drop across the sense resistor; however, the turn-off gate current is also controlled with the conventional VSD.

In view of the switching losses and spike during the switching process, this paper proposes one current adaptive switching strategy, where the turn-on/turn-off current for the power switch can be regulated adaptively with the load variation to reduce the dominant switching losses. In addition, the caused spike during the switching process can be limited to a decent value. This paper is organised as follows: the operating principle of the proposed switching strategy is given in Section 2. The switching characteristics of power switch with a constant CSD are fully presented in Section 3. Section 4 shows the design consideration and the drive circuit. Then, the proposed switching strategy is compared with the VSD and tested by means of several experiments in Section 5. Finally, the conclusion is drawn in Section 6.

2 Current adaptive switching strategy

2.1 Proposed switching strategy

Taking a boost converter controlled by average current mode, for example, the proposed switching strategy is shown in Fig. 1*a*. The main circuit is marked in the dotted-line area, which consists of input voltage U_{in}, inductance L, power loop stray inductance L_s, diode D and power switch Q. C_{gs}, C_{gd} and C_{ds} are the parasitic capacitances of Q. C_D is the parasitic capacitance of diode D. The drive resistance R_g represents the inner parasitic resistance and the external series resistance. Moreover, the controller with double-loop control (voltage loop Gv and current loop Gi) and the proposed gate-driver strategy are presented at the outside of dotted-line area. As shown in Fig. 1*a*, the current reference signal i_{Lref} through

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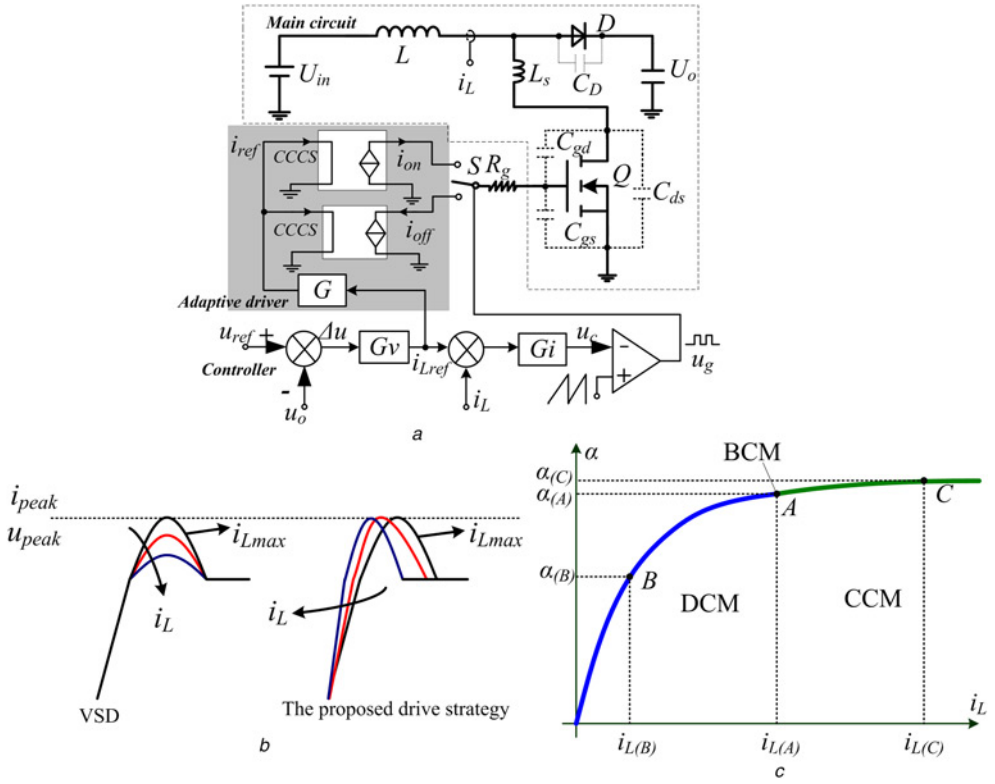

Fig. 1 *Proposed switching strategy*
a Proposed current adaptive switching strategy
b Current/voltage spike during switching transition
c Relational curve of the duty cycle α and the inductor current i_L

a reverse regulator G, forming the control current signal i_{ref}, which determines the turn-on current i_{on} and turn-off current i_{off} by the current controlled current source (CCCS). Since i_{Lref} is determined by the inductor current, also determined by the load, the drive current i_{on} and i_{off} can change adaptively with the variation of the load. Moreover, the controller outputs signal u_g determines the working state of switch Q.

2.2 Working principle

In the conventional VSDs, the switching speed keeps constant once the drive circuits are designed and the peak value of current/voltage spikes exist at the switch passing through the maximum current, correspondingly, the converter operates at full load. However, the spikes will fall down with the decrease of switch current due to the same slew rate. In that case, it implies the slew rate during switching transient can be adjusted with the variation of switch current while ensuring the spikes lower than the peak values (i_{peak}, v_{peak}), as shown in Fig. 1*b*.

Concretely, the relationship between the duty cycle α and the inductor current i_L in a high-frequency DC/DC converter as shown in Fig. 1*c*. In case the converter is working at boundary conduction mode in point A, the current of this operation point is $i_{L(A)}$ and duty cycle is $\alpha_{(A)}$. The left region of A can be defined as the discontinuous conduction mode (DCM) area and the right area of that is the continuous conduction mode (CCM) area. It can easily get that the duty cycle α increases rapidly with the increase of i_L in the DCM area, while rises slowly in the CCM area. Assuming that the converter works at the light load in point B and operates at the rated load in point C, then, $i_{L(B)} < i_{L(C)}$, which means $i_{Lref(B)} < i_{Lref(C)}$. The regulator G adjusts the signal i_{Lref} reversely and outputs i_{ref}, as a result, $i_{ref(B)} > i_{ref(C)}$. Therefore, the drive current $i_{on(B)} > i_{on(C)}$ and $i_{off(B)} > i_{off(C)}$, which implies the switching speed of the power switch in point B is faster than that in point C. The faster switching speed is, the less switching losses will be. As a result, the efficiency of the converter in the point B could be higher than that in point C. So, with this proposed switching strategy, the switching speed of switch can be regulated adaptively with the inductor current changing and the efficiency can be improved relatively.

3 Analysis of the switching characteristics of switch

The switching losses and current/voltage spike resulted from switching transient are two key factors in the design of the drive circuit. Although the analytical modelling of switching transition with CSD has been discussed in detail in [24], they neglect the parasitic capacitor of the diode, which has an influence on the switching transient in real circuit. In this paper, the switching modelling of switch [metal–oxide–semiconductor field-effect transistor (MOSFET)] considering the parasitic capacitor of freewheeling diode will be studied stage by stage. A typical boost converter is employed to clarify the switching characteristics. The equivalent turn-on/turn-off transition circuits and the qualitative waveforms of the switching transient are shown in Fig. 2.

To simplify the analysis of the operation stage, the following conditions are assumed:

(i) $C_{iss} = C_{gd} + C_{gs}$ and $C_{oss} = C_{gd} + C_{ds}$ are denoted as the input and output capacitances of the MOSFET, respectively.
(ii) In all the analytical calculations, the MOSFET has no reverse recovery and it is considered to be a resistance, an open circuit or a dependent current source whose behaviour is described by

$$i_{ch} = g_{fs}(u_{gs} - V_{TH}) \quad (1)$$

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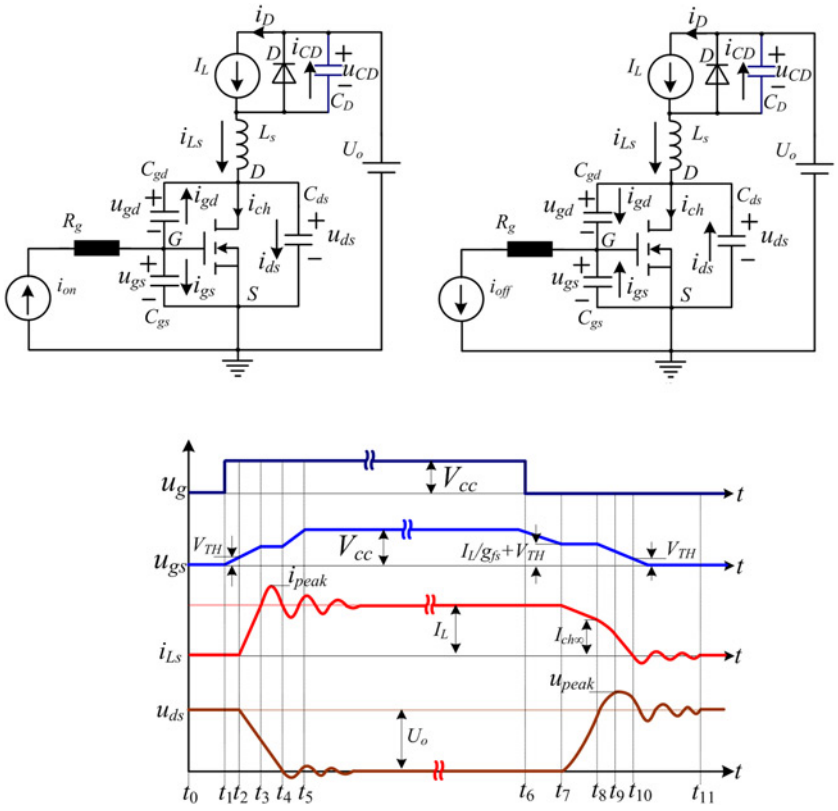

Fig. 2 *Equivalent turn-on/turn-off switching circuits and the qualitative waveforms of the switching transient*

where g_{fs} and V_{TH} are the MOSFET transconductance and the threshold voltage, respectively.

(iii) When the converter running in steady state, the inductor current is unchangeable as a constant current source I_L and the turn-on/turn-off current can be thought as constant value.

(iv) When $u_{gs} > V_{TH}$, MOSFET is ON and if $u_{gs} < V_{TH}$, MOSFET is OFF.

(v) The power loop stray inductance is L_s.

3.1 Turn-on switching transient

The turn-on transient can be divided into four different substages described in the following sections.

Substage 1 [t_1–t_2] turn-on delay time: During t_0–t_1, the power switch Q is off and the inductor current I_L flows through the diode D. At t_1, the PWM signal u_g is turned into high level. C_{iss} is charged by the drive current i_{on}. The MOSFET works in the cut-off region until the gate–source voltage u_{gs} reaches to the threshold voltage V_{TH}. I_L still circulates through the diode D while the channel current i_{ch} equals to 0. Thus, only the gate circuit should be considered and the equivalent circuit is shown in Fig. 3*a*. The gate–source voltage u_{gs} is given by

$$u_{gs}(t) = \frac{i_{on}}{C_{iss}}(t - t_1) \tag{2}$$

Substage 2 [t_2–t_3] current rise time: In this stage, when u_{gs} reaches V_{TH}, the MOSFET channel starts conducting and i_{ch} starts to increase from zero, the drain–source voltage u_{ds} simultaneously decreases due to the voltage drop induced by the rising drain current across the stray inductor L_s. This voltage drop u_{Ls} determines whether u_{ds} will drop to zero before or after i_{Ls} reaches to I_L, which will further determine the operating mode of the MOSFET in this stage and the following stages. Both of them are described as follows.

Case (I): The MOSFET works in saturation region, the channel current i_{ch} is governed by (1). Fig. 3*b* shows this stage equivalent circuit and equations can be obtained from this figure, which are as follows:

$$\begin{cases} u_{ds} = u_{gd} + u_{gs} \\ i_{on} = C_{gs}\dfrac{du_{gs}}{dt} - C_{gd}\dfrac{du_{gd}}{dt} \\ I_L = i_D + i_{Ls} \\ i_{Ls} - C_{ds}\dfrac{du_{ds}}{dt} = i_{ch} + C_{gd}\dfrac{du_{gd}}{dt} \\ U_o = L_s\dfrac{di_{Ls}}{dt} + u_{ds} \end{cases} \tag{3}$$

By solving (3), there are two possible cases.

(i) *Overdamped condition*: The stray inductor L_s is relatively large and satisfies (4). Then, the voltage u_{ds} and the drain current slew rate di_{Ls}/dt could be calculated as (5)

$$L_s > \frac{4(C_{iss}^2 C_{ds} + C_{gs}C_{gd}C_{iss})}{g_{fs}^2 C_{gd}^2} \tag{4}$$

$$\begin{cases} u_{ds}(t) = U_o - \dfrac{i_{on}g_{fs}L_s}{C_{iss}} + k_1 e^{-p_1(t-t_2)} + k_2 e^{-p_2(t-t_2)} \\ \dfrac{di_{Ls}}{dt} = \dfrac{i_{on}g_{fs}}{C_{iss}} - \dfrac{1}{L_s}[k_1 e^{-p_1(t-t_2)} + k_2 e^{-p_2(t-t_2)}] \end{cases} \tag{5}$$

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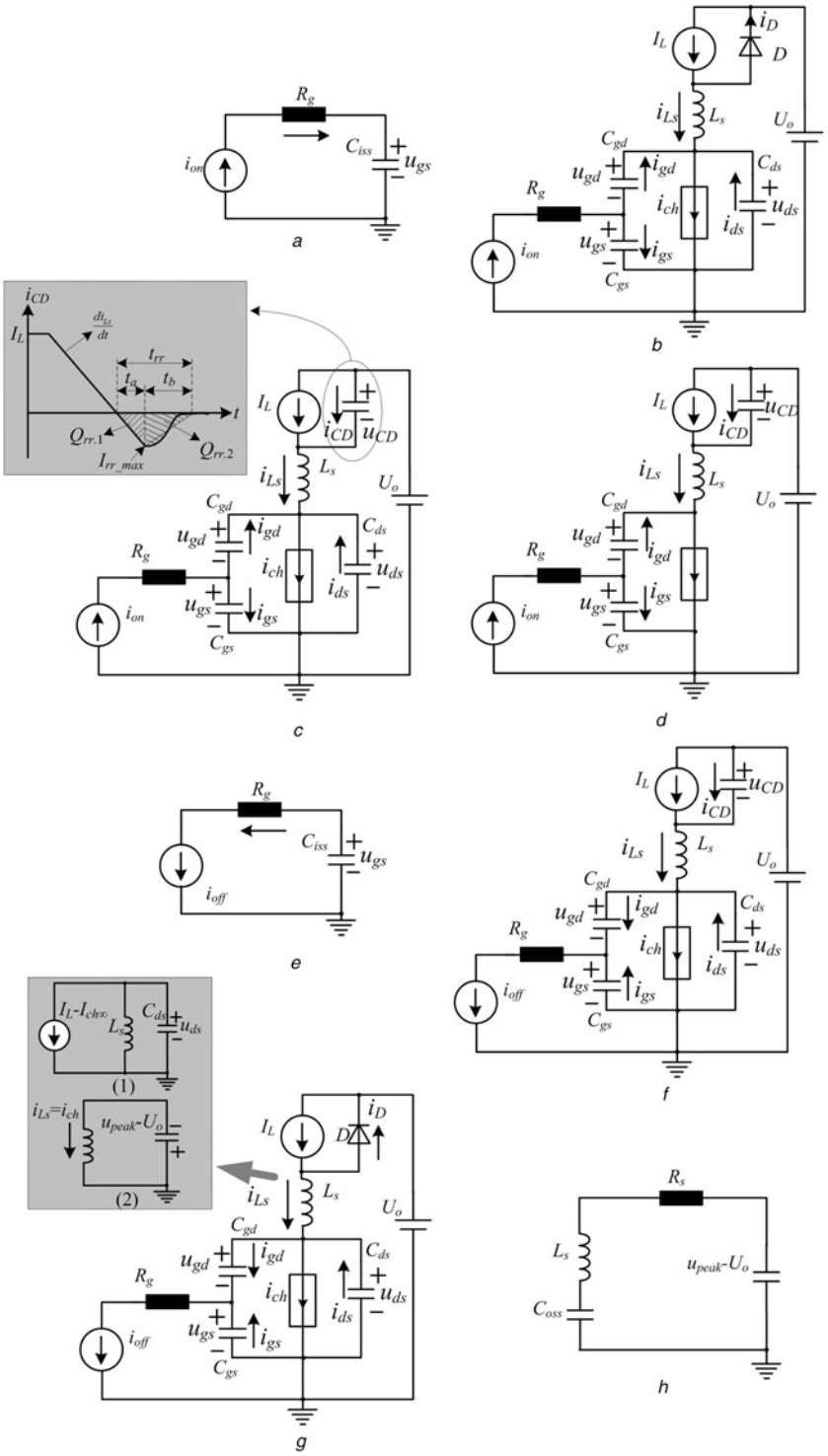

Fig. 3 *Equivalent circuit during turn-on (a–d)/turn-off (e–h) transition*
a Substage 1 [t_1–t_2]
b Substage 2 [t_2–t_3]
c Substage 3 [t_3–t_4]
d Substage 4 [t_4–t_5]
e Substage 5 [t_6–t_7]
f Substage 6 [t_7–t_8]
g Substage 7[t_8–t_{10}]
h Substage 8 [t_{10}–t_{11}]

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where
(see (6))

(ii) *Underdamped condition*: L_s is small and satisfies (7). Similarly, the u_{ds} and di_{Ls}/dt can be expressed by (8)

$$L_s < \frac{4(C_{iss}^2 C_{ds} + C_{gs}C_{gd}C_{iss})}{g_{fs}^2 C_{gd}^2} \tag{7}$$

$$\begin{cases} u_{ds}(t) = U_o - \dfrac{i_{on}g_{fs}L_s}{C_{iss}} + e^{-\alpha(t-t_2)}\{k_3\cos[\beta(t-t_2)] + k_4\sin[\beta(t-t_2)]\} \\ \dfrac{di_{Ls}}{dt} = \dfrac{i_{on}g_{fs}}{C_{iss}} - \dfrac{1}{L_s}e^{-\alpha(t-t_2)}\{k_3\cos[\beta(t-t_2)] + k_4\sin[\beta(t-t_2)]\} \end{cases} \tag{8}$$

where

$$\begin{cases} \beta = \sqrt{\omega_0^2 - \alpha^2},\ k_3 = \dfrac{i_{on}g_{fs}L_s}{C_{iss}} \\ k_4 = \dfrac{i_{on}}{\beta}\left(\dfrac{C_{gd}}{C_{oss}C_{iss} - C_{gd}^2} + \dfrac{\alpha g_{fs}L_s}{C_{iss}}\right) \end{cases} \tag{9}$$

Case (II): The MOSFET works in ohmic region, in case the drain–source voltage u_{ds} is very small and the drain current i_{Ls} will rise at a rate determined by the stray inductor instead of u_{gs}. If the voltage drop of u_{ds} is neglected, then with U_o entirely dropping on L_s and i_{Ls} will increase at a constant rate, i.e. U_o/L_s.

In fact, since *case II* appears when the stray inductance L_s is extremely large and is not likely to occur in a well-designed converter, so it will not be discussed in the following sections.

Substage 3 [t_3–t_4] *Current ringing time (diode reverse recovery time)*: At t_3, i_{Ls} reaches I_L, the diode D will change its polarity and start the reverse recovery process. The current ringing begins and the stray inductor will resonate with parasitic capacitors C_D and C_{ds}. Thus, i_{Ls} continues rising and u_{ds} decreases simultaneously. The equivalent circuit of this stage is shown in Fig. 3*c*. The equations can be established as

$$\begin{cases} i_{on} = C_{gs}\dfrac{du_{gs}}{dt} - C_{gd}\dfrac{du_{gd}}{dt} \\ i_{Ls} = g_{fs}(u_{gs} - V_{TH}) + C_{gd}\dfrac{du_{gd}}{dt} + C_{ds}\dfrac{du_{ds}}{dt} \\ i_{Ls} = I_L + C_D\dfrac{du_{CD}}{dt} \\ U_o = u_{ds} + L_s\dfrac{di_{Ls}}{dt} + u_{CD} \\ u_{ds} = u_{gs} + u_{gd} \end{cases} \tag{10}$$

By simplifying (10), the di_{Ls}/dt can be gotten
(see (11))

However, the solution of (11) is very complicated and the results are not convenient to analyse. It is necessary to scrutinise on the other hand. Here, analysis can be deduced from the principle of the reverse recovery characteristic of the diode. According to the Kirchhoff's current law, the drain current i_{Ls} is given by

$$i_{Ls}(t) = I_L + i_{CD}(t - t_3) \tag{12}$$

where i_{CD} is the reverse recovery current. The dotted-line area of Fig. 3*c* shows the characteristics of the diode reverse recovery. The reverse time t_{rr} is divided into two parts t_a and t_b, when i_{CD} rises from 0 to I_{rr_max} and then returns to 0, respectively. The reverse recovery charge Q_{rr} is also divided into $Q_{rr.1}$ and $Q_{rr.2}$. According to the reverse time, di_{Ls}/dt obtained from (5) or (8) is the current slew rate of i_{Ls} at $i_{Ls} = I_L$, which are dependent on the case MOSFET works.

Accordingly, the equations can be founded

$$\begin{cases} t_{rr} = t_a + t_b,\ m = t_b/t_a \\ I_{rr\_max} = (di_{Ls}/dt)\cdot t_a\big|_{i_{Ls}=I_L} \\ Q_{rr} = I_{rr\_max}t_{rr}/2 \end{cases} \tag{13}$$

I_{rr_max} is calculated by (13)

$$I_{rr\_max} = \sqrt{\frac{2Q_{rr}di_{Ls}/dt\big|_{i_{Ls}=I_L}}{(m+1)}} \tag{14}$$

Therefore, the maximum current i_{peak} flows through the drain of MOSFET is given by

$$i_{peak} = I_L + I_{rr\_max} = I_L + \sqrt{\frac{2Q_{rr}di_{Ls}/dt\big|_{i_{Ls}=I_L}}{(m+1)}} \tag{15}$$

At t_4, the drain–source voltage u_{ds} decreases to $U_{ds(on)}$, the MOSFET will go into the ohmic region.

Substage 4 [t_4–t_5] *current damping oscillation time*: In this stage, the MOSFET works in ohmic region and u_{ds} remains at $U_{ds(on)}$. The channel current i_{ch} is no longer controlled by u_{gs}, which keeps constant at I_L. C_{gs} continues to charge and u_{gs} goes on to charge up and will reach V_{cc}. However, the loop stray inductance L_s and parasitic capacitances C_D will keep on resonating together until the current i_{CD} arrives 0 at t_5. The equivalent circuit illustrates in Fig. 3*d*.

3.2 Turn-off switching transient

Similar to the turn-on switching process, the turn-off transient can be also divided into four substages.

Substage 5 [t_6–t_7] *turn-off delay time*: At t_6, the PWM signal u_g is set as 0 and the turn-off current i_{off} starts to discharge the input capacitance C_{iss}. The MOSFET operates in the ohmic region and i_{ch}, u_{ds} remain unchanged in this stage. The equivalent circuit is

$$\begin{cases} \alpha = \dfrac{g_{fs}C_{gd}}{2(C_{ds}C_{iss} + C_{gs}C_{gd})},\ \omega_0^2 = \dfrac{C_{iss}}{L_s(C_{ds}C_{iss} + C_{gs}C_{gd})},\ p_1 = -\alpha + \sqrt{\alpha^2 - \omega_0^2},\ p_2 = -\alpha - \sqrt{\alpha^2 - \omega_0^2} \\ k_1 = \dfrac{p_2}{p_2 - p_1}\dfrac{i_{on}g_{fs}L_s}{C_{iss}} + \dfrac{1}{p_2 - p_1}\dfrac{i_{on}C_{gd}}{C_{oss}C_{iss} - C_{gd}^2},\ k_2 = \dfrac{p_1}{p_1 - p_2}\dfrac{i_{on}g_{fs}L_s}{C_{iss}} + \dfrac{1}{p_1 - p_2}\dfrac{i_{on}C_{gd}}{C_{oss}C_{iss} - C_{gd}^2} \end{cases} \tag{6}$$

$$\left(C_{ds} + \frac{C_{gs}C_{gd}}{C_{iss}}\right)L_s\frac{di_{Ls}^3}{dt^3} + \frac{g_{fs}C_{gd}}{C_{iss}}L_s\frac{di_{Ls}^2}{dt^2} + \left(1 + \frac{C_{ds}}{C_D} + \frac{C_{gs}C_{gd}}{C_{iss}}\right)\frac{di_{Ls}}{dt} + \frac{g_{fs}C_{gd}}{C_{iss}C_D}i_{Ls} = \frac{g_{fs}}{C_{iss}}\left(i_{on} + \frac{I_LC_{gd}}{C_D}\right) \tag{11}$$

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shown in Fig. 3*e*. The u_{gs} can be expressed as

$$u_{gs}(t) = V_{cc} - \frac{i_{off}}{C_{iss}}(t - t_6) \tag{16}$$

When $u_{gs} = V_{TH} + I_L/g_{fs}$, this stage ends.

Substage 6 [t_7–t_8] *voltage rise time*: Fig. 3*f* shows the equivalent circuit during this period. The MOSFET operates in saturation region and the channel current i_{ch} drops suddenly. The excess current I_L–i_{ch}–i_{CD} charges the parasitic capacitances C_{gd} and C_{ds}. Therefore, the voltage u_{ds} starts to rise until it reaches U_o and the i_{Ls} begins to decrease from I_L. In this stage, the circuit equations can be expressed as follows:

$$\begin{cases} u_{ds} = u_{gd} + u_{gs} \\ i_{off} = -C_{gs}\dfrac{du_{gs}}{dt} + C_{gd}\dfrac{du_{gd}}{dt} \\ I_L = i_{Ls} - C_D\dfrac{du_{CD}}{dt} \\ i_{Ls} - C_{ds}\dfrac{du_{ds}}{dt} = i_{ch} + C_{gd}\dfrac{du_{gd}}{dt} \\ U_o = u_{CD} + L_s\dfrac{di_{Ls}}{dt} + u_{ds} \end{cases} \tag{17}$$

However, due to the Miller effect, there is a plateau region in u_{gs} which keeps constant, so the current i_{gs} approximates to 0 in this interval. Thus, u_{ds} and i_{Ls} are obtained from (17)

$$\begin{cases} i_{Ls}(t) = I_L + \dfrac{i_{off}C_D}{C_{gd}}\left\{\cos\left[\dfrac{1}{\sqrt{L_sC_D}}(t - t_7)\right] - 1\right\} \\ u_{ds}(t) = \dfrac{i_{off}}{C_{gd}}(t - t_7) \end{cases} \tag{18}$$

This period ends when the u_{ds} arrives at U_o at t_8. In addition, if the i_{ch} reaches 0 before u_{ds} goes to U_o, which is likely to happen if I_L is relatively small. In that case, the following stage has access to *Substage 8* directly.

Substage 7 [t_8–t_{10}] *current falling time*: At t_8, the diode D ceases to block the voltage and the I_L starts to divert from the MOSFET to D. Since the stray inductance L_s impedes a sudden change in the drain current, the drain–source voltage u_{ds} continues increasing. The equivalent circuit is shown in Fig. 3*g*. Similarly, the equations can be founded as

$$\begin{cases} i_{off} = -C_{gs}\dfrac{du_{gs}}{dt} + C_{gd}\dfrac{du_{gd}}{dt} \\ i_{Ls} = g_{fs}(u_{gs} - V_{TH}) + C_{gd}\dfrac{du_{gd}}{dt} + C_{ds}\dfrac{du_{ds}}{dt} \\ u_{ds} = U_o + L_s\dfrac{di_{Ls}}{dt} \\ u_{ds} = u_{gs} + u_{gd} \end{cases} \tag{19}$$

Similar to the expression (11), the solution of (19) is difficult to analyse. So, the analytical method in [25] is adopted here. This period can be divided into two stages and the specific demonstration is as follows.

(i) *Current falling period (I)* [t_8–t_9]: In this short stage, assume the gate voltage keeps constant and as well as the channel current. At t_8, the circuit conditions can be simplified by independent current and voltage source in the circuit and a rearrangement of the sources. Then, the final equivalent circuit can be achieved, as shown in the dotted-line area (1) of Fig. 3*g*. It is clear that the L_s and C_{ds} will resonate with each other and the u_{ds} can be easily expressed from Fig. 3*g*

$$\begin{cases} u_{ds}(t) = U_o + (I_L - I_{ch\infty})\sqrt{\dfrac{L_s}{C_{ds}}}\sin\left[\dfrac{1}{\sqrt{L_sC_{ds}}}(t - t_8)\right] \\ I_{ch\infty} = 2\left(\dfrac{I_L}{g_{fs}} + V_{TH}\right) - \dfrac{i_{off}(C_D + C_{oss})}{g_{fs}C_{gd}} \end{cases} \tag{20}$$

where the current $I_{ch\infty}$ is the initial value of the channel current, which is obtained based on the approximation, the detailed derivation is given in the Appendix.

This stage ends when the current i_{Ls} arrives at the channel current $I_{ch\infty}$ at t_9, the u_{ds} has reached its peak value u_{peak}, which can be easily calculated

$$\begin{aligned} u_{peak} &= u_{ds}(t_9) \\ &= U_o + (I_L - I_{ch\infty})\sqrt{\frac{L_s}{C_{ds}}}\sin\left[\frac{1}{\sqrt{L_sC_{ds}}}(t_9 - t_8)\right] \end{aligned} \tag{21}$$

(ii) *Current falling period (II)* [t_9–t_{10}]: During this period, the voltage u_{peak}–U_o effects on the stray inductor. The drain current will be forced to continue falling to 0. As the current difference i_{Ls}–i_{ch} charges the capacitance C_{ds}, these two values are very close during this period, so there will not be a large current charging C_{ds}. Hence, the voltage u_{ds} can be considered equal to u_{peak} approximately. To simplify this stage, the channel current i_{ch} is assumed to be controlled by the voltage U_o. The equivalent circuit of this stage is shown in the dotted-line area (2) of Fig. 3*g*, i_{ch} can be approximated as

$$i_{ch}(t) = I_{ch\infty} - \frac{u_{peak} - U_o}{L_s}(t - t_9) \tag{22}$$

At t_{10}, the channel current i_{ch} decreases to 0 and this stage ends.

Substage 8 [t_{10}–t_{11}] *voltage damping oscillation time*: After the channel current i_{ch} decreases entirely to 0, u_{gs} reduces from V_{TH} to 0 and the MOSFET works in the cut-off region. At this moment, a resonate circuit formed by L_s and C_{oss} begins to oscillate; however, the stray resistance R_s will damp the oscillation until the voltage u_{ds} reaches its steady-state value U_o. The equivalent circuit is shown in Fig. 3*h*. The voltage u_{ds} and drain current i_{Ls} can be deducted as

$$\begin{cases} u_{ds}(t) = U_o + (u_{peak} - U_o)e^{-\alpha(t - t_5)}\cos\omega_2(t - t_{10}) \\ i_{Ls}(t) = C_{oss}\dfrac{du_{ds}}{dt} = -C_{oss}(u_{peak} - U_o)e^{-\alpha(t - t_{10})} \\ \qquad \times \{\omega_2\sin[\omega_2(t - t_{10})] + \alpha\cos[\omega_2(t - t_{10})]\} \end{cases} \tag{23}$$

where

$$\begin{cases} \omega_2 = \sqrt{1/(L_sC_{oss}) - \alpha^2} \\ \alpha = -R_s/2L_s \end{cases} \tag{24}$$

This stage ends when the u_{ds} keeps a steady-state value U_o.

4 Analysis of power losses and driving circuit design

4.1 Power losses during turn-on transition

According to the analysis of turn-on process, the power losses during [t_1–t_2] and [t_2–t_3] can be easily calculated. While the power losses derivation during [t_3–t_5] could be sophisticated because the circuit is ringing. To calculate the power losses

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Table 1 Turn-on power losses under different substages

Substage	Power losses
t_1–t_2	$P_{1\_Loss} = 0$
t_2–t_3	$P_{2\_Loss} = f_s \int_{t_2}^{t_3} i_{Ls}(t-t_2)\cdot u_{ds}(t-t_2)\mathrm{d}t$
t_3–t_5	$P_{3\_Loss} = f_s U_o\left(Q_{rr} - \frac{1}{2}C_D U_o\right)$

during this interval, the perspective of energy change extensively analysed in [26] is utilised.

First, the energy losses during the period of the current i_{Ls} changing from I_L to its peak value i_{peak} are approximated to

$$E_{Loss\_1} = U_o Q_{rr.1} - \frac{1}{2}L_s(i_{peak}^2 - I_L^2) \tag{25}$$

where $Q_{rr.1}$ is the part of the reverse recovery charge Q_{rr} that is removed from the diode as shown in Fig. 3*c*.

At t_5, the circuit reaches steady state when the ringing is fully clamped. The only energy in the loop is stored in C_D, thus the energy losses in this part is

$$E_{Loss\_2} = U_o Q_{rr.2} - \frac{1}{2}C_D U_o^2 + \frac{1}{2}L_s(i_{peak}^2 - I_L^2) \tag{26}$$

With $Q_{rr.2}$ as the other part of Q_{rr} that is needed to charge the parasitic capacitance C_D. Therefore, the total energy losses in this interval can be expressed as

$$E_{Loss(t_3-t_5)} = E_{Loss\_1} + E_{Loss\_2} = U_o Q_{rr} - \frac{1}{2}C_D U_o^2 \tag{27}$$

Hence, it is easy to obtain the power losses during $[t_3$–$t_5]$

$$P_{3\_Loss} = f_s U_o\left(Q_{rr} - \frac{1}{2}C_D U_o\right) \tag{28}$$

The power losses under different substages of turn-on process are illustrated in Table 1.

4.2 *Power losses during turn-off transition*

Similarly, the power losses derivation in the periods of $[t_6$–$t_7]$, $[t_7$–$t_8]$, $[t_8$–$t_9]$ and $[t_9$–$t_{10}]$ can be gotten easily from the equivalent circuits, which are given in Table 2. Similarly, the power losses during $[t_{10}$–$t_{11}]$ can be calculated by the energy stored at the beginning and the end of this stage.

At t_{10}, the energy stored in the loop circuit is

$$E_{t_{10}} = \frac{1}{2}C_{ds}u_{peak}^2 \tag{29}$$

Table 2 Turn-off power losses under different substages

Substage	Power losses
t_6–t_7	$P_{5\_Loss} = 0$
t_7–t_8	$P_{6\_Loss} = f_s \int_{t_7}^{t_8}\left\{I_L + \frac{i_{off}C_D}{C_{gd}}[\cos\ \omega_0(t-t_7) - 1]\right\}\frac{i_{off}}{C_{gd}}(t-t_7)\mathrm{d}t$
t_8–t_9	$P_{7\_Loss} = f_s I_{ch\infty}\int_{t_8}^{t_9}[U_o + (I_L - I_{ch\infty})L_s\omega_1\ \sin\ \omega_1(t-t_8)]\mathrm{d}t$
t_9–t_{10}	$P_{8\_Loss} = f_s u_{peak}\int_{t_9}^{t_{10}} I_{ch\infty} - [(u_{peak} - U_o)(t-t_9)/L_s]\mathrm{d}t$
t_{10}–t_{11}	$P_{9\_Loss} = f_s\left[\frac{1}{2}C_{ds}(u_{peak}^2 + U_o^2) - C_{ds}u_{peak}U_o\right]$

At the end of the stage, the energy stored is

$$E_{t_{11}} = \frac{1}{2}C_{ds}U_o^2 \tag{30}$$

Besides, the energy recovered to the source during $[t_{10}$–$t_{11}]$ is given by

$$E_s = \int_{t_{10}}^{t_{11}} U_o i_{Ls}(t)\mathrm{d}t = U_o\int_{t_{10}}^{t_{11}} i_{Ls}(t)\mathrm{d}t = U_o C_{ds}(u_{peak} - U_o) \tag{31}$$

The energy dissipated in the loop circuit can be obtained

$$\begin{aligned} E_{Loss(t_{10}-t_{11})} &= E_{t_{10}} - E_{t_{11}} - E_s = \frac{1}{2}C_{ds}u_{peak}^2 - \frac{1}{2}C_{ds}U_o^2 \\ &\quad - U_o C_{ds}(u_{peak} - U_o) \\ &= \frac{1}{2}C_{ds}(u_{peak}^2 + U_o^2) - C_{ds}u_{peak}U \end{aligned} \tag{32}$$

Therefore, the power losses can be gotten during $[t_{10}$–$t_{11}]$

$$P_{9\_Loss} = \frac{1}{2}f_s[C_{ds}(u_{peak}^2 + U_o^2) - C_{ds}u_{peak}U_o] \tag{33}$$

As depicted in Tables 1 and 2, the power losses during the turn-on and turn-off transitions are closely related to the turn-on current i_{on} and turn-off current i_{off}, respectively. It is necessary to design i_{on} and i_{off} reasonably to improve the performance of the converter.

4.3 *Design of turn-on /turn-off current with spike limitation*

According to the analysis of switching transient in Section 3, the faster the switching speed is, the lower the switching losses will be. However, as displayed in (15) and (21), larger turn-on/turn-off current may lead to a higher current/voltage spike. If the spike value is extremely large, the switch will be possible to break down. Therefore, in the design of the turn-on/turn-off current, the current/voltage spike should be treated as the most important reference.

It is easy to find that the spike value is dependent on the inductance current I_L, turn-on/turn-off current, power loop stray inductance L_s, the inherent parameters of MOSFET along with freewheeling diode (g_{fs}, C_{iss}, C_{oss}, C_{rss} and Q_{rr}). On the basis of the aforesaid analysis with the proposed switching strategy, the design principle is that the current/voltage spike under a smaller inductor current is not greater than that under a rated inductor current; meanwhile, the switching speed changes adaptively.

A typical boost converter is used to demonstrate the design procedure of the turn-on/turn-off current. The setup is as follows: the switch MOSFET is IRFP460A and the diode is RHRG1560_F085. Their relational parameters found in the datasheet are listed in Table 3. The input voltage is 200 V_{DC} and the output voltage is 380 V_{DC}. The power loop stray inductance L_s is set about 1 μH. Combined with the parameters [(15) and (21)] the

Table 3 Components and relational parameters

MOSFET (Q): IRFP460A			
C_{oss}	130 pF	C_{iss}	3100 pF
C_{rss}	7 pF	g_{fs}	11
V_{TH}	3 V		
Diode (D): RHRG1560_F085			
Q_{rr}	21 nC	C_D	30 pF
t_a	15 ns	t_b	11 ns

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relationship between the current/voltage spike (i.e. i_{peak}/u_{peak}) inductor current and the turn-on/turn-off current (i.e. i_{on}/i_{off}) is shown in Fig. 4. It can be intuitively gotten that the turn-on/turn-off current will increase with the decreasing of inductor current I_L if the spike value is fixed constant. From the relation curve in Fig. 4, the turn-on/turn-off current (i.e. i_{on}/i_{off}) can be approximately designed as

$$i_{on}(i_{off}) = N_1 - N_2 \cdot I_L \tag{34}$$

where N_1, N_2 being two constants, which are different under turn-on and turn-off conditions.

4.4 Drive circuit

Fig. 5 shows the turn-on/turn-off drive circuit which is not limited to this kind of method. Here, the UC3854A is employed to control the boost converter. The CCCS shown in Fig. 1*a* that consists of the CAOUT pin signal and voltage control current source (VCCS) shown in Fig. 5*b* are used to adjust the turn-on/turn-off current, adaptively. The turn-on adaptive drive circuit includes VCCS-1, R_1–R_3, T_1–T_2, D_1–D_4 and a comparator IC1, while the turn-off circuit is composed of Q_1, T_3 and T_4. If the u_{pwm} is high level, the i_{on} will charge the C_{iss} to turn-on MOSFET, while if the u_{pwm} is low level, the i_{off} will discharge the C_{iss} to turn-off the MOSFET by the mirror current source. The VCCS consists of the LT3086 produced by *linear* company and its peripheral circuit, which is explained at length in the datasheet [27], as shown in Fig. 5*b*. In addition, the CAOUT and V_{REF} are two pins of the UC3854A. If the signal in CAOUT is u_c, the inductor current I_L is similar proportional to Hu_c according to the analysis in Section 2.2. Moreover, the VCCS could be expressed by $i_{on}(i_{off}) = Ku_r$, where u_r is the adjustable signal in the TRACK pin. Therefore, if $R_5 = R_6 = R_7$, and D_5 is IN4733, the drive signal current is given by

$$i_{on}(i_{off}) = \frac{10.2R_9K}{R_8 + R_9} - \frac{R_9HK}{R_8 + R_9} \cdot I_L \tag{35}$$

where K and H are two constants, but R_8 and R_9 are different in VCCS-1 and VCCS-2, obviously (35) matches with (34).

5 Experimental verification

To verify the proposed adaptive drive strategy, one boost converter with 200 V input, 380 V/1 kW output and 150 kHz was built and other specifications are listed in Table 3. The control IC is UC3854A and the adaptive drive circuit is shown in Fig. 5. It is noted that the smaller the loop stray inductance (is), the better the performance of converter will be. However, in this prototype, to reflect the principle of the proposed adaptive drive strategy, the

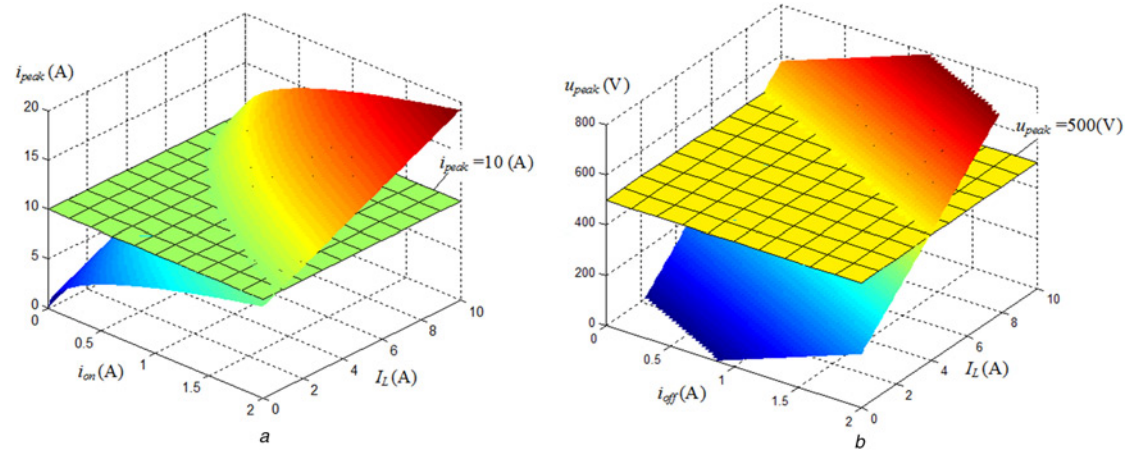

Fig. 4 *Design of turn-on/turn-off current with spike limitation*
a Relational curve between i_{peak}, I_L, i_{on} and $i_{peak} = 10$ A
b Relational curve between u_{peak}, I_L, i_{off} and $u_{peak} = 500$ V

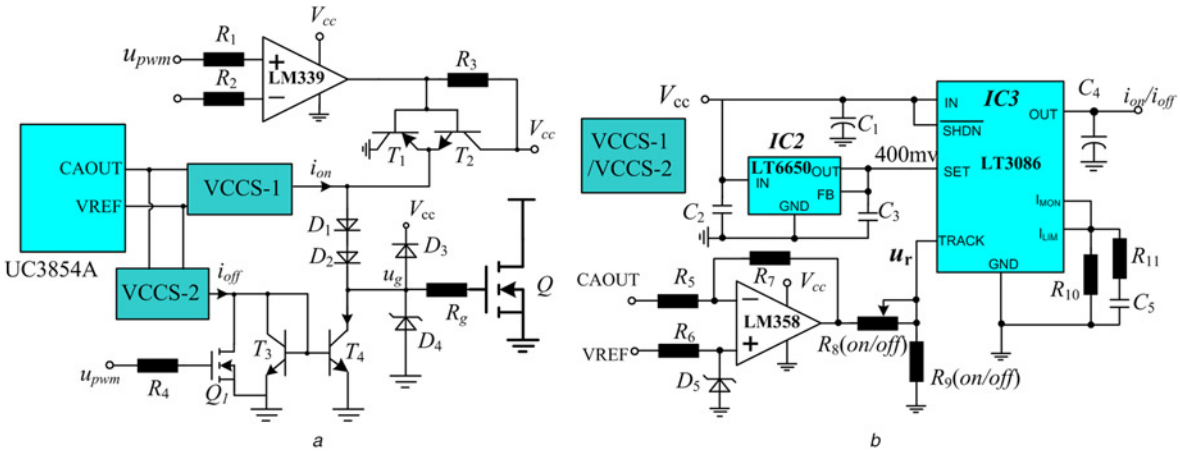

Fig. 5 *Drive circuit*
a Turn-on/turn-off driving circuit
b VCCS

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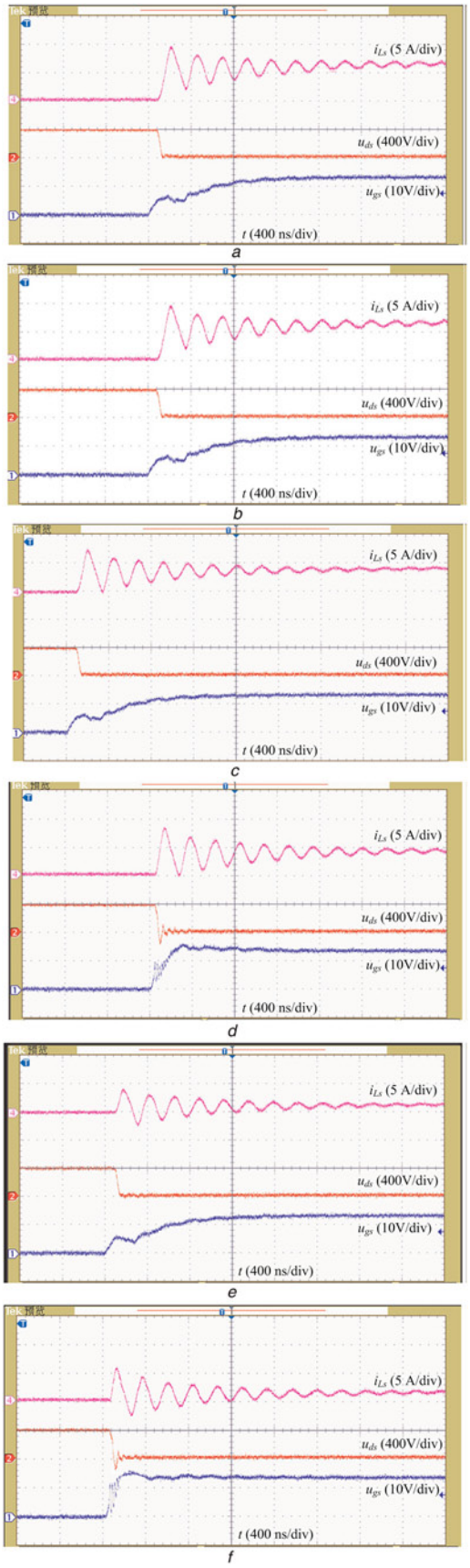

Fig. 6 *Waveforms of the drain current i_{Ls}, drain–source voltage u_{ds} and gate–source voltage u_{gs} under different loads during turn-on transient. (a)–(b) Under full load; (c)–(d) Under half-full load; and (e)–(f) Under 20% load*
a, *c*, *e* For the VSD method
b, *d*, *f* For the proposed adaptive drive method

loop stray inductance is set about 1 μH. From Fig. 4, if the current/voltage spikes are limited to 10 A and 500 V, respectively, during the switching process, the turn-on current i_{on} can be set within 0.3–2 A modulating adaptively, while the turn-off current within 0.5–2 A, which can be realised by (35). In circuit application, in order to achieve the better control effect, the turn-on or turn-off current can be adjusted within certain realms by regulating R_8 and R_9 in Fig. 5*b*.

In real experimental process, the i_{on} and i_{off} were regulated within 0.3–1.2 and 0.5–1.4 A changing adaptively, respectively, and have attained better performance. The key drive specifications are: T_1: C2655, T_2: A1020, T_3–T_4: C2655, D_1–D_3: 1N4148, D_4: 1N4742, Q_1: AO3404A, $R_{8(on)}$: 410 kΩ, $R_{9(on)}$: 20 kΩ; $R_{8(off)}$: 356 kΩ and $R_{9(off)}$: 20 kΩ.

By contrast, the prototype was tested with the proposed drive strategy and the conventional VSD strategy. Figs. 6 and 7 show the key experimental waveforms during turn-on transition and turn-off transition under different loads, respectively.

Figs. 6*a* and *b* give the waveforms of the drain current i_{Ls}, drain–source voltage u_{ds} and gate–source voltage u_{gs} at full load with the conventional VSD and the proposed method, respectively. It is obviously seen that they show a similar transient process because they are designed as the same turn-on speed at full load. The current spike is limited at 10 A and the duration of t_1–t_5 shown in Fig. 2 is near 800 ns. As seen in Figs. 6*d* and *f*, the turn-on duration of t_1–t_5 is about 320 ns at the half-full load and is near 200 ns at 20% full load with the proposed drive method. The current spike does not exceed the set value 10 A. However, since the parameters of the drive circuit remain unchangeable in the conventional VSD, the time of turn-on process is fixed, which are illustrated in Figs. 6*c* and *e*. Accordingly, by the proposed drive strategy, the turn-on speed is adaptively adjusted and the current spike is limited to the reference value with the change of the load. The overlap area of the drain current and the drain–source voltage is narrowed, so the power losses can be reduced in turn-on transient.

Fig. 7 illustrates the comparison of the typical waveforms during turn-off transient with the conventional VSD and the proposed strategy. From Figs. 7*a* and *b*, both the voltage spikes are limited to about 500 V and the turn-off duration of t_6–t_{10} shown in Fig. 2 is ~320 ns. With the load decreasing, the turn-off speed can be adjusted by the proposed strategy, while it remains unchanged by the conventional driving method, which can be seen in Figs. 7*c*–*f*. As shown in Figs. 7*d* and *f*, the duration of t_6–t_{10} decreases from 240 ns at half-load to 120 ns at 20% full load by the proposed drive strategy; meanwhile, the voltage spike would not exceed 500 V. However, the turn-off duration maintains constant, which can be reflected in Figs. 7*a*, *c* and *e*. Hence, the turn-off power losses can be reduced with the proposed driving strategy. In addition, from Fig. 7*a*–*f*, it can be seen one duration that u_{gs} is reduced and hold as constant, i_{Ls} is still high and u_{ds} is still low. This is caused by the reverse recovery of the power MOSFET, but it has no influence on the spikes and switching losses, so this stage has not been marked in Fig. 2.

Fig. 8 shows the efficiency comparison of the proposed drive strategy and the conventional drive method. It is shown that the converter efficiency using the proposed switching strategy under light load rises by more than 1.5% that in the conventional drive method.

6 Conclusion

This paper presents a new current adaptive switching strategy applied in DC/DC converter, which can limit the current/voltage spike as the switching speed is regulated with the change of load. First, the working principle of the proposed switching strategy is analysed. Then, a circuit-level model, in consideration of MOSFET capacitances, the circuit loop stray inductance and the

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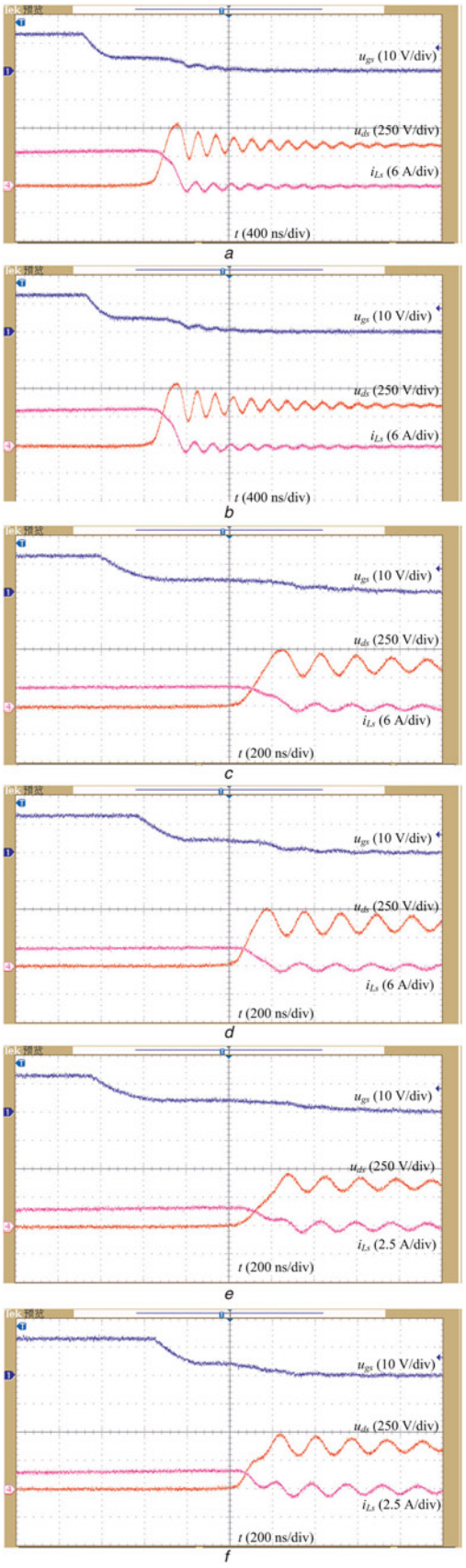

Fig. 7 *Waveforms of the drain current i_{Ls}, drain–source voltage u_{ds} and gate–source voltage u_{gs} under different load during turn-off transient. (a)–(b) Under full load; (c)–(d) Under half-full load; and (e)–(f) under 20% load*
a, *c*, *e* For the VSD method
b, *d*, *f* For the proposed adaptive drive method

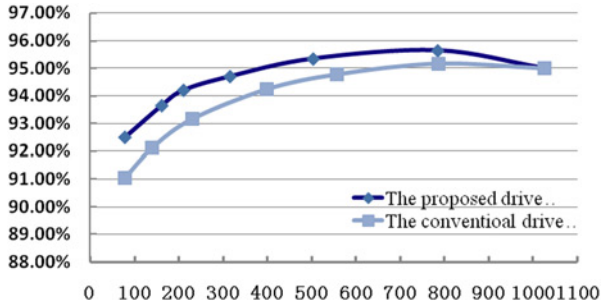

Fig. 8 *Efficiency comparison*

reverse current of the diode, has been built to scrutinise the turn-on/turn-off process of the MOSFET with a constant current driving. The expressions of the current/voltage spike can be obtained from the analysis of the switching transition. The relationship between the drain current, the inductor current and turn-on/turn-off current is discussed in detail to design the drive circuit. Finally, the prototype with a boost converter has been established to verify the proposed switching strategy. Besides, the conventional drive method (VSD) has also been tested to be compared with the proposed method. The experimental results show that theoretical analysis is correct and the converter with the proposed switching strategy has a higher efficiency than that with the conventional drive method under a light load.

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9 Appendix

Derivation of current $I_{ch\infty}$ in Section 3 substage 7

At t_7, the initial conditions are

$$\begin{cases} u'_{gs(0)} = V_{TH} + I_L/g_{fs} \\ u'_{gd(0)} = -(V_{TH} + I_L/g_{fs}) \\ u'_{ds(0)} = 0 \\ u'_{CD(0)} = U_o \\ i'_{Ls(0)} = I_L \end{cases} \tag{36}$$

From Fig. 7*b*, the following expressions in *S-domain* could be found:

$$\begin{cases} u_{ds}(s) = u_{gd}(s) + u_{gs}(s) \\ \dfrac{I_{off}}{s} = C_{gd}[su_{gd}(s) + (V_{TH} + I_L/g_{fs})] - C_{gs}[su_{gs}(s) - (V_{TH} + I_L/g_{fs})] \\ \dfrac{I_L}{s} = i_{Ls}(s) - C_D(su_{CD}(s) - U_o) \\ i_{Ls}(s) = g_{fs}\left(u_{gs}(s) - \dfrac{V_{TH}}{s}\right) + C_{gd}[su_{gd}(s) + (V_{TH} + I_L/g_{fs})] + sC_{ds}u_{ds}(s) \\ \dfrac{U_o}{s} = u_{CD}(s) + L[si_{Ls}(s) - I_L] + u_{ds}(s) \end{cases} \tag{37}$$

These equations can be solved directly to find $u_{gs}(s)$ (see (38))

where

$$\begin{cases} A = C_{oss}C_{iss}L_sC_D - C_{gd}^2L_sC_D, \quad B = C_{iss}C_D + C_{oss}C_{iss} - C_{gd}^2 \\ M = V_{TH} + \dfrac{I_L}{g_{fs}}, \quad N = g_{fs}V_{TH}C_{gd} \end{cases} \tag{39}$$

By the approximate method in [25], using the final value theorem to obtain the current $I_{ch\infty}$

$$\begin{aligned} I_{ch\infty} &= \lim_{t\to\infty} i_{ch} = \lim_{t\to\infty} g_{fs}u_{gs}(t) = \lim_{s\to 0} su_{gs}(s) + \frac{I_L}{g_{fs}} + V_{TH} \\ &= 2\left(\frac{I_L}{g_{fs}} + V_{TH}\right) - \frac{i_{off}(C_D + C_{oss})}{g_{fs}C_{gd}} \end{aligned} \tag{40}$$

$$u_{gs}(s) = \frac{1}{s}\frac{\mathrm{AM}s^3 + (I_LC_{gd} - I_{off}C_{oss} + N)L_sC_Ds^2 + \mathrm{BM}s + I_LC_{gd} - I_{off}(C_D + C_{oss}) + N}{As^3 + g_{fs}C_{gd}L_sC_Ds^2 + Bs + g_{fs}C_{gd}} \tag{38}$$

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