Indirect boost matrix converter and low-voltage generator for direct drive wind turbines

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Abstract: Here, a new topology for direct drive wind turbines (DDWTs) with a new power electronics interface and a low-voltage generator is presented. In the presented power electronics interface, the grid-side converter is replaced by a boost current source inverter (CSI) which eliminates the required dc-bus capacitors, resulting in an increase in the system lifetime. The inherently required dc-link inductor for this topology is eliminated by utilising the synchronous inductance of the permanent magnet synchronous generator. The control technique used for the developed DDWT is described here. The boost CSI enables conversion of a low dc voltage to a higher line-to-line voltage creating an indirect boost matrix converter, and thus, enabling the implementation of a low-voltage generator. This further enables a reduction in the number poles required in direct drive wind generators. The feasibility of the proposed generator-converter topology for DDWTs and its controllers are verified through simulations and experimental results on a laboratory scale 1.5 kW, 240 V set-up.

1 Introduction

In 2015, the global wind power capacity increased by 63 GW, adding up to a global total of 433 GW [1]. In the USA, wind energy is the leading renewable source with an installed capacity of 74.5 GW, of which 8.6 GW alone was added in 2015 [1]. As more companies join the wind power market, the need for cutting-edge technologies that increase the system reliability while reducing capital and maintenance costs becomes a relevant concern among researchers and industries. The most common wind turbine topology is the indirect drive wind turbine where the rotor shaft is connected to the generator through a gearbox [2]. Most commonly used indirect drive wind turbine topology is with doubly-fed induction generator (DFIG). In this system, the stator of the induction generator is connected directly to the grid and the rotor circuit is connected to the grid through the power electronics converters. The power electronics interface between the rotor circuit and the grid comprises a two bidirectional converters connected at the dc-bus, formed by electrolytic capacitors. In a DFIG configuration, the power converters are not rated for full power and they share only a fraction of the power produced. Another wind turbine topology is with a permanent magnet synchronous generator (PMSG), and back-to-back voltage source converter (VSC) forming the power electronics interface. Unlike the DFIG configuration, this topology utilises a full power rated power electronics interface, and therefore, the need for a gearbox can be avoided. It has been shown that the gearboxes cause more downtime than any other component in a wind turbine [3–5]. It is worth noting that, although responsible for 20% of total wind turbine down time, gearboxes only account for 10% of wind turbine failures [6]. The direct drive wind turbine (DDWT) has the turbine rotor shaft directly connected to the generator shaft without any gearbox, thus eliminating the high operation and maintenance costs associated with gearboxes. However, the DDWTs are still not as popular as DFIGs due to the high cost of PMSGs. Fig. 1*a* shows the most common DDWT topology, comprising PMSG connected to the grid through back-to-back connected VSCs [7, 8]. The dc-bus between the VSCs is formed by electrolytic capacitors in order to have a stable and constant dc-bus voltage. In some cases, the power electronics interface can be a back-to-back connection of multilevel converters. These multilevel converters can be a neutral-point-clamped back-to-back converter, or H-bridge back-to-back converter [9]. All the power electronics interfaces mentioned above have electrolytic capacitors forming the dc-bus. The electrolytic capacitors are one of the most failure-prone components and decrease the system reliability. The failure of these capacitors can have huge impact on the system maintenance costs, particularly in the case of offshore wind turbines [10]. Additionally, the PMSGs used in DDWTs are large in size as the generator shaft rotates at the same speed as the turbine rotor shaft [11, 12]. This results in a very high number of poles in the PMSG contributing to the high cost and volume of the generator.

The most common, power electronics interface configuration for DDWTs comprises two VSCs connected back-to-back at the dc-bus, formed by electrolytic capacitors. In this paper, a new power converter configuration formed by cascaded connection of a VSC and boost current source inverter (CSI) is presented. The CSI topology enables elimination of the most vulnerable component in the existing topology of direct drive wind turbines, i.e. dc-bus electrolytic capacitor without any additional component at the dc-bus [13, 14]. The boost CSI can convert a low dc voltage to higher three-phase ac with a relatively high boost ratio which facilitates the implementation of low-voltage PMSG with lower weight and volume. The reduced weight and size of the PM generator leads to a reduction in the capital cost associated with the DDWTs. The current market of rare earth metals, which are used to make the PM material (NdFeB), is highly unstable and the rare earth metals have very high cost. A reduced cost generator with the more reliable converter system will have a huge commercial impact on promoting the widespread deployment of the DDWTs [15].

In addition to the introduction, this paper has four more sections. In Section 2, the topology of the indirect boost matrix converter is described. Section 3 presents the switching pattern of phasor pulse width modulation (PPWM) for three-phase boost inverter. The feasibility of the developed topology and its controllers is demonstrated in Section 4 through simulation of a grid-tied system, with and without wind speed variation. In this section, the steady-state operation of the proposed system is verified through some experimental results. Section 5 presents the conclusion of the paper.

2 Proposed topology and control

In this section, first the proposed topology for DDWTs is introduced. The power electronics interface, the low-voltage PMSG,

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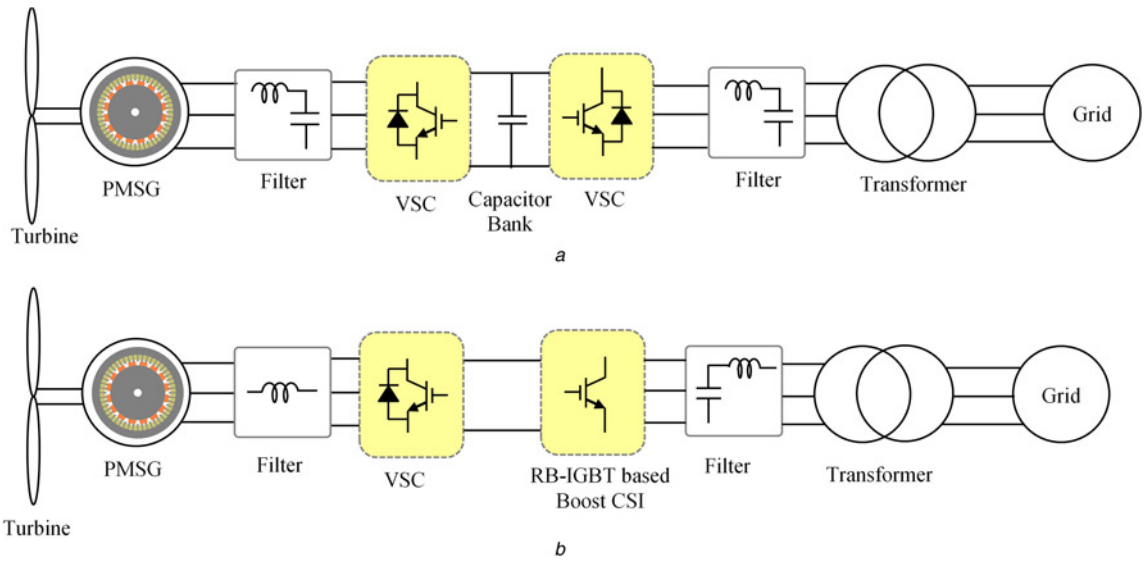

Fig. 1 *DDWT topology with*
a PMSG connected to back-to-back VSCs as existing systems
b PMSG connected to a VSC and the boost CSI as the proposed system

and the control schemes forming the developed system are described.

2.1 Topology

The proposed topology for the DDWTs is shown in Fig. 1*b*. In this wind turbine system, the rotor shaft is connected directly to the PMSG. The turbine injects power to the grid through a fully rated power electronics interface, as can be seen in Fig. 1*b*. The power converter configuration and the flexibility provided by them in the PMSG design are described next.

2.1.1 Power converter: In a traditional DDWT, the power electronics interface is formed by two VSCs connected back-to-back at a dc-bus formed by dc-bus electrolytic capacitors, as shown in Fig. 1*a*. In the developed system, the grid-side VSC is replaced by a boost CSI, and the obtained circuit topology of the power converters is shown in Fig. 1*b*. The boost CSI is formed by reverse-blocking insulated-gate bipolar transistors (IGBTs) (RB-IGBTs), and the topology eliminates the need for dc-bus capacitors. The CSI topology inherently needs dc-link inductors which is replaced by the per-phase synchronous inductance of the PMSG. In order to maintain the quality of the output voltage and current waveforms from the boost CSI, as needed for grid connection according to IEEE 1547, the inverter must operate in continuous conduction mode (CCM). While any CSI requires a dc-link inductor, the proposed DDWT avoids the need for a dc-link inductor by utilising the generator synchronous inductance, L_s. In order to achieve a low total harmonic distortion (THD) in the current waveforms at the inverter output, the boost CSI must operate in CCM. The synchronous inductance, L_s, will be less than a conventional dc-link inductor, L_{dc}, i.e. $L_s = \sqrt{3/2}\, L_{dc}$, since the Thevenin's equivalent inductance of the generator-converter from the dc-bus is almost $(3/2)L_s$ and $I_{rms} \simeq \sqrt{2/3}\, I_{dc}$. The low dc-side voltage required by the boost CSI enables a low-voltage requirement from the PMSG for the same power output. The PMSG design flexibility achieved through this is discussed next.

2.1.2 Low-voltage PMSG: The power electronics interface presented in the previous subsection allows a low-voltage PMSG to be used in the DDWT. For a traditional topology of DDWT, in order to obtain three-phase rms line-to-line voltage of 690 V at the output of the converters, the line-to-line voltage output needed by the PMSG is ~750 V. By using the developed power converter topology discussed in the previous subsection, the same 690 V three-phase line-to-line voltage can be achieved by PMSG output voltage of ~400 V.

For simplicity of the analysis, consider the emf equation of $E \propto N_{ph} p \omega_m \phi_p$, where E is the peak of induced voltage per phase, N_{ph} the number of turns per phase, ω_m is the mechanical angular velocity, p the total number of poles, and ϕ_p the maximum magnetic flux per pole [16]. The ω_m are governed by the wind speed, and the fundamental magnetic flux per pole is obtained from $\phi_p \cong (4/\pi)(2\pi/p)(D/2)l = 4Dl/p$, where D is the mid-airgap diameter, and l is the stack length. Accordingly, one can say $E \propto N_{ph} Dl$ means that a generator with a lower output voltage requires a lower value of $N_{ph}Dl$. On the other hand, the minimum synchronous inductance, required for the boost CSI to operate in CCM, restricts the maximum number of poles, since $L_s \propto (Dl/l_g)(N_{ph}/p)^2$ [16]. Hence, the desired values of the generator output voltage, $(E^2 - (\omega_s L_s I)^2)^{1/2} \cong E$ and synchronous inductance, L_s, are herein used as the PMSG design inputs for a given rated power.

2.2 Control technique

In this subsection, the control technique developed for modulation of the developed power converter topology is explained. The block diagram of the developed controller is shown in Fig. 2. The controller for the developed system is a two-part controller with first controller for the VSC and the second for the boost CSI. The VSC controller is used for maximum power point tracking (MPPT) and it delivers the maximum power available dependent on the generator speed (governed by the wind speed) to the dc-side. The boost CSI controller is used to maintain a constant average dc-side voltage while controlling the reactive power injected into the grid. Thus, the VSC controller modulates the active power injected into the grid, while the boost CSI controller modulates the reactive power injected into the grid.

2.2.1 VSC controllers: The VSC controller receives the generator line-to-line voltages, line currents, dc-side voltage, and dc-side current as input signals. The three-phase quantities are then transferred to the *dqo* reference frame, rotating at generator electrical speed, ω_{gen}. The measured power on the dc-side is compared to the desired active power signal, P^*, and the error is forced to zero

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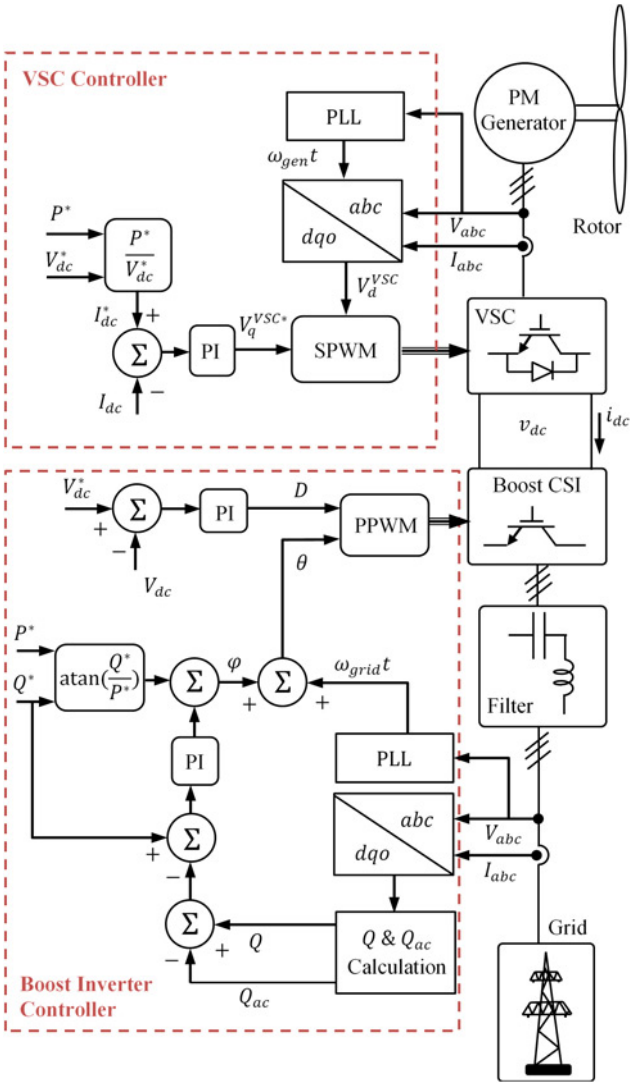

Fig. 2 *Block diagram of controller for the power electronics interface*

through a proportional integral (PI) controller, while generating the desired q-axis voltage, $V_q^{\mathrm{VSC}*}$, for the converter input. The desired active power, P^*, signal is generated from the generator rotor speed, using the an existing MPPT technique, where $P^* = K_{\mathrm{opt}}\omega_R^3$, [17, 18]. The generated $V_q^{\mathrm{VSC}*}$ and the measured V_d^{VSC} are used to compute the reference signals for generating the switching signals for the VSC using sine pulse width modulation (PWM) switching technique.

2.2.2 Boost CSI controller: The boost CSI controller receives the line-to-line voltages at the point of common coupling, line current injected into the grid, and dc-side voltage as inputs. The average dc-side voltage, V_{dc}, is compared to the desired dc-side voltage, V_{dc}^*, and the error is forced to zero through a PI controller, see Fig. 2. This generates the modulation index, D, required for implementing the PPWM switching technique as described in Section 3. The measured three-phase quantities are transferred to the *dqo* frame of reference, rotating at grid frequency. The measured reactive power injected into the grid, Q, is corrected by the amount of reactive power compensated by the ac filter capacitors, Q_{ac}, and then compared to the desired reactive power, Q^*. A PI controller is then used to make the error zero while generating the correction factor for the phase shift between inverter and grid voltages, φ, as can be seen in Fig. 2. This generates the boost CSI reference angle, θ, which is needed for generating the PPWM switching pattern. The verification of these developed controllers is presented in Section 4.

3 PPWM-based boost inverter

The PPWM switching pattern for the boost inverter is presented in this section. In spite of similarities between PPWM for the boost inverter and state vector PWM (SVPWM) for VSI, there are fundamental differences [19, 20]. These differences can be herein summarised as:

- PPWM is formulated based on phasor quantities (line-to-line voltages), not space-vectors.
- In SVPWM, six main switching states, and two zeroes exist with three switches conducting at any given instant; however, in PPWM, six discharging and three charging states are present, with only two switches conducting at any given instant,
- In SVPWM, six vectors based on six switching states are stationary, and the desired space vector is formed by switching between these states and zeroes, while in PPWM, a stationary V_{dc} is known and line-to-line voltage phasors are formed by switching the dc-link current.

For further clarification, the charging and discharging states are described below.

State ***C***: In this state, the dc circuit is shorted through two switches from a same leg. For example, in sector I (refer to Table 1) S_{ap} and S_{an}, are closed and the dc-link inductor is being charged over t_{c}. Fig. 3*a* shows the equivalent circuit of the converter and path of the dc-link current for this state in which voltage across L_{dc} equals V_{dc}. Fig. 4 shows the dc-link inductor voltage waveform over the charging time, t_{c}. Furthermore, Fig. 5 demonstrates the experimentally obtained dc-link inductor current and voltage waveforms from the case study 208 V, 1.5 kW, 60–90 $\mathrm{V_{dc}}$ boost inverter.

State ***D1***: During the first discharging time-interval, t_{d1}, the inductor current is directed into phase A and returned from phase B in sector I (refer to Table 1), when S_{ap} and S_{bn} are closed. Fig. 3*b* depicts the equivalent circuit of the boost inverter during t_{d1} when the voltage across L_{dc} equals to $V_{\mathrm{dc}} - V_1 = V_{\mathrm{dc}} - v_{ab}$, as shown in Fig. 4.

State ***D2***: During the second discharging time-interval, t_{d2}, the inductor current is directed into phase A and returned from ***C***, when S_{ap} and S_{cn} are closed. Fig. 3*c* depicts the equivalent circuit of the boost inverter during t_{d2} when voltage across L_{dc} equals to $V_{\mathrm{dc}} - V_2 = V_{\mathrm{dc}} - v_{ac}$, as shown in Fig. 4.

From the voltage–second balance law for the dc-link inductor voltage at steady-state conditions, one can write $V_{\mathrm{dc}}T_{\mathrm{s}} = V_1 t_{d_1} + V_2 t_{d_2}$ (refer to Fig. 4), where V_1 and V_2 are different line-to-line voltages in each sector, as shown in Table 1. Dividing this equation by T_{s}, yields:

$$V_{\mathrm{dc}} = V_1 d_1 + V_2 d_2 \tag{1}$$

where $d_{\mathrm{c}} = t_{\mathrm{c}}/T_{\mathrm{s}}$, $d_1 = t_{d1}/T_{\mathrm{s}}$, and $d_2 = t_{d2}/T_{\mathrm{s}}$ are the charging and discharging duty ratios, which are related as follows:

$$d_{\mathrm{c}} = 1 - (d_1 + d_2) \tag{2}$$

The discharging ratios, d_1 and d_2, are obtained from the law of sines as $d_1 = m\ \sin(\pi/3 - \theta)$ and $d_2 = m\ \sin(\theta)$. Using (2), d_{c} is calculated as

$$d_{\mathrm{c}} = 1 - m\ \sin\left(\theta + \frac{\pi}{3}\right) \tag{3}$$

where m is known as the modulation index. In order to improve the quality of generated ac voltages, a discretised version of PPWM is

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Table 1 Sectors and switching states in PPWM

Sector	V_1	V_2	S_{ap}	S_{an}	S_{bp}	S_{bn}	S_{cp}	S_{cn}
I	V_{ab}	V_{ac}	T_s	t_c	0	t_{d1}	0	t_{d2}
II	V_{ac}	V_{bc}	t_{d1}	0	t_{d2}	0	t_c	T_s
III	V_{bc}	V_{ba}	0	t_{d2}	T_s	t_c	0	t_{d1}
IV	V_{ba}	V_{ca}	t_c	T_s	t_{d1}	0	t_{d2}	0
V	V_{ca}	V_{cb}	0	t_{d1}	0	t_{d2}	T_s	t_c
VI	V_{cb}	V_{ab}	t_{d2}	0	t_c	T_s	t_{d1}	0

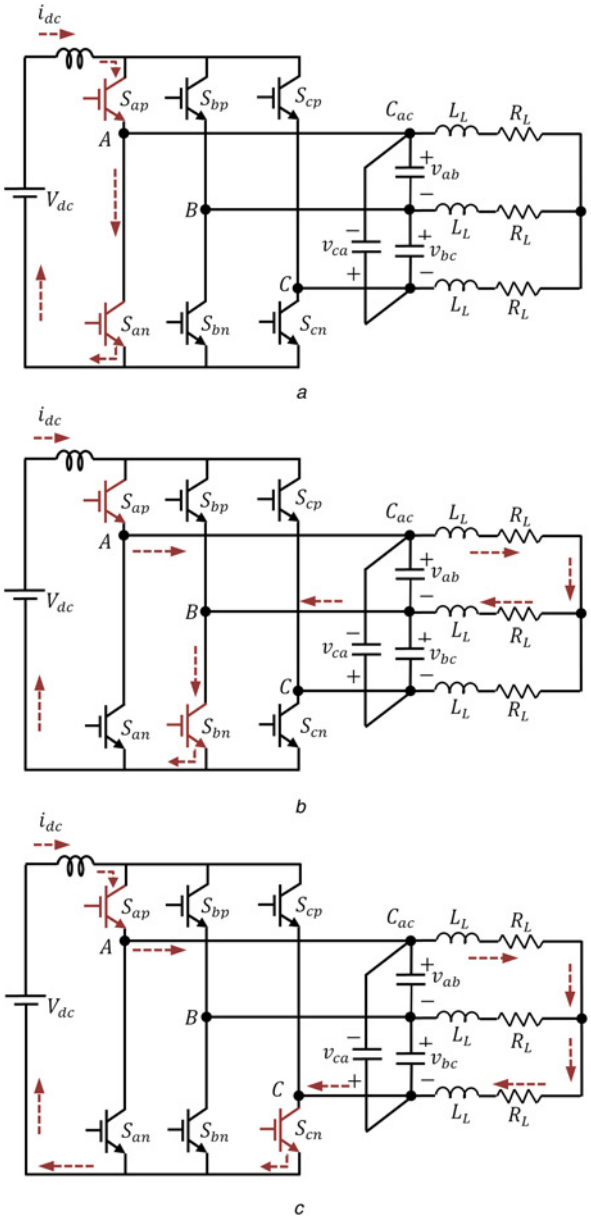

Fig. 3 *Equivalent circuit of the boost inverter during*
a State C: charging time interval
b State D1: first discharging time interval, and
c State D2: second discharging time interval of sector I

used based on constant charging time over each sector and staircase patterns for discharging time intervals. In the discretised PPWM, (i) averaged charging duty ratio, D, remains constant over each sector (one-sixth of the power cycle) and (ii) discharging times are discretised. In the discretised method, the numbers of points associated with the discharging time intervals are approximated

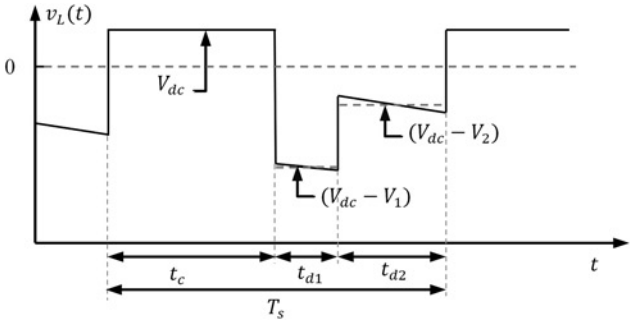

Fig. 4 *Ideal voltage waveform of the dc-link inductor in the boost inverter where V_1 and V_2 are the line-to-line output voltages as given in Table 1 for each sector*

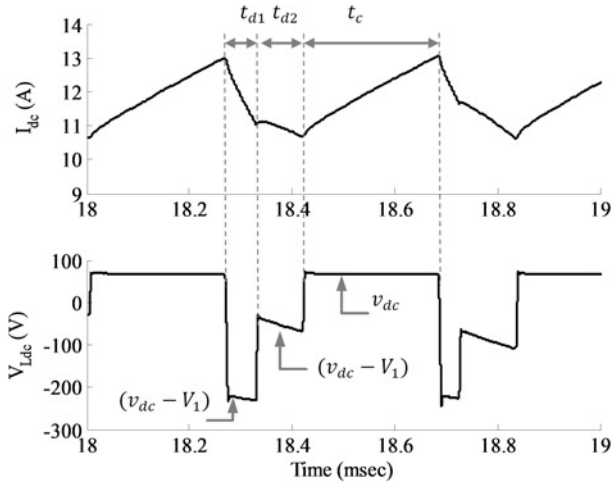

Fig. 5 *Experimentally obtained waveforms of current and voltage of the dc-link inductor in the case study 208 V, 1.5 kW, 60 V_{dc} boost inverter*

by increasing and decreasing staircase functions. In this technique, n_c is obtained as $n_c = D.N_T$ where $\lfloor\rfloor$ is the floor function, and N_T is mainly limited by the bandwidth of D/A converters when implementing PPWM on hardware. Herein, n_1, n_2, and n_c are the number of sampling points in the discharging and charging time intervals. Using (3), the relationship between m and D can be obtained by taking the average value of d_c over one sector as follows:

$$D = 1 - \frac{3}{\pi}m \tag{4}$$

The switching patterns of all switches over 18 ms, i.e. slightly more than one power cycle, are shown in Fig. 6. The selection of N_T is also very important in maintaining symmetrical switching pattern and ensuring quarter-wave symmetry in the output voltage and current waveforms. Therefore, N_T must be chosen such that $N_T/(6M)$ becomes an integer number, where M is the number of step (discretised) changes, in n_1 and n_2, over one sector. Notice, a path must always exist for the dc-link current in a boost inverter. This problem is resolved by employing an overlap-time, t_∇, i.e. a small duration when the three switches associated with a commutation process are conducting before turning off a switch.

The validity of the proposed switching pattern is evaluated through a set of simulations performed on the boost inverter. As discussed above, a proper choice of N_T can result in quarter-wave symmetry in inverter's current waveforms. Fig. 7 demonstrates the line current and its frequency spectrum for $N_T = 60$. This value of N_T provides an equal and integer number of sample points per sector, which results in quarter-wave symmetry in the inverter's

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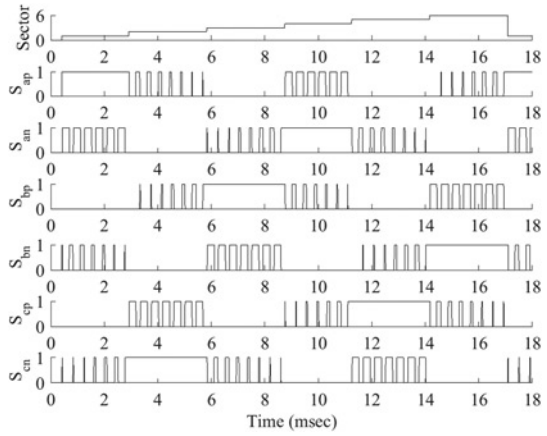

Fig. 6 *Switching pattern obtained using discretised PPWM*

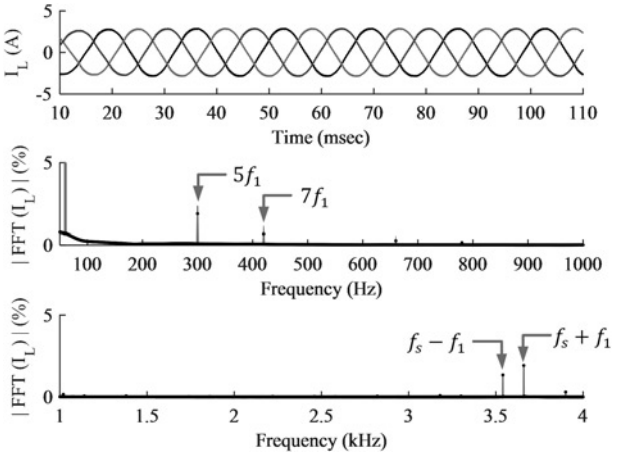

Fig. 7 *Phase current waveform for $N_T = 60$ and its FFT spectrum with THD = 3.23% for $V_{dc} = 65$ V*

current waveforms. In this study, $M = 10$ and $f_s = N_T f_1 = 3.6$ kHz, resulted in no even harmonic components in the current waveform.

The boost inverter is characterised via the operation region with respect to the charging ratio, D. As shown in Fig. 8, the family of curves are plotted for different input voltage levels or boost ratios. In the following, a formula indicating the output rms current variations by the charging ratio, D, is derived. Using the following equation [20]:

$$v_{\rm dc} = R_{\rm dc} i_{\rm dc} + L_{\rm dc} \frac{{\rm d}i_{\rm dc}}{{\rm d}t} + \frac{\sqrt{3}}{2} m v_q \tag{5}$$

where $R_{\rm dc}$ is the dc-side effective resistance, i.e. $R_{\rm dc} = R_{L\rm dc} + (1 - D)R_{\rm ON\_IGBT}$. Using (4) and (5), and neglecting the dc-link current ripple while substituting $V_q = \sqrt{2} V_{LL}$ leads to the steady-state equation of $I_{\rm dc}$ as follows:

$$I_{\rm dc} = \frac{1}{R_{\rm dc}} \left(V_{\rm dc} - \frac{\pi}{\sqrt{6}} (1 - D)\, V_{LL} \right) \tag{6}$$

One can see that the dc-link current varies with D, the input dc voltage, $V_{\rm dc} = v_{\rm dc}(t)$, and the grid voltage, V_{LL}. The fundamental component of the inverter current can be expressed by

$$I_{\rm inv}^{\rm rms}(f_1) = \frac{\pi}{3\sqrt{2}} (1 - D) I_{\rm dc} \tag{7}$$

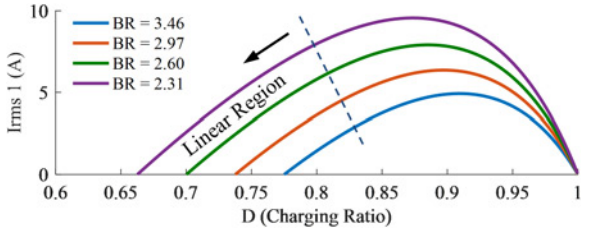

Fig. 8 *Operating region and rms current, $I_{\rm inv}^{\rm rms}(f_1)$, profiles of a $V_{LL} = 208$ V, 1.5 kW boost inverter for different boost ratios, $BR = V_{LL}/V_{dc}$ when the effective resistance of the charging path is $R_{dc} = 0.3 + 2(0.8)(1 - D)$*

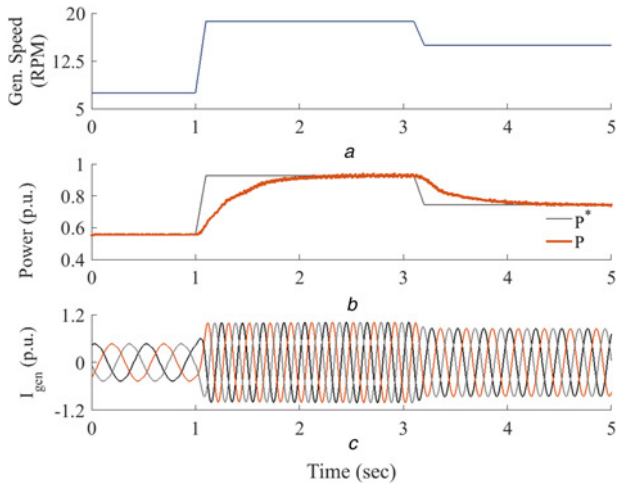

Fig. 9 *Simulation results*
a Generator speed governed by wind speed
b p.u. desired and measured power injected into grid, and
c p.u. three-phase generator line current when the wind speed is varying

By substituting (6) into (7), $I_{\rm inv}^{\rm rms}(f_1)$ can be obtained from

$$I_{\rm inv}^{\rm rms}(f_1) = \frac{\pi(1 - D)}{3\sqrt{2} R_{\rm dc}} \left(V_{\rm dc} - \frac{\pi}{\sqrt{6}} (1 - D)\, V_{LL} \right) \tag{8}$$

From (8), the minimum value of D for given input and output voltage levels can be estimated as: $D_{\rm min} \simeq 1 - (\sqrt{6}/\pi)(V_{\rm dc}/V_{LL})$, also shown in Fig. 8. The linear operational region is in the left side of the dash-line shown in Fig. 8.

4 System verifications

In this section, the controllers and switching pattern for the boost inverter described in Sections 2 and 3, respectively, are implemented and the feasibility of the entire system is demonstrated through simulation and experimental results.

4.1 Simulation results

Firstly, the developed system is implemented in MATLAB/Simulink environment, using the SimPowerSystem toolbox while using the PMSG parameters obtained in a design done by a FE machine design software [15]. The rms line-to-line grid voltage was taken as 690 V (1 p.u.) which is generally the transformer primary voltage for a DDWT connected to the grid. The controllers described in Section 2 can be verified through the results shown in Fig. 9, which demonstrates the feasibility of the proposed system for variable wind speed. The input wind speed is varied over a period of 5 s. Fig. 9*a* shows the resulting generator speed over this interval. From $t = 0$ s to $t = 1$ s, the generator speed is

7.5 rpm. At $t = 1$ s, the speed gradually increases to 18.75 rpm and at $t = 3.1$ s, the speed decreases gradually to 15 rpm. The speed profile chosen herein consists of sudden changes in the wind speed, which is used to demonstrate the robustness of the controllers. The generator speed is used to compute P^*. Fig. 9*b* shows P^* and the measured active power injected into the grid. It can be observed from Fig. 9*b* that the power injected into the grid closely matches P^*. The waveforms of the three-phase current output from the PMSG are shown in Fig. 9*c*, showing that the controllers have acceptable performance while maintaining the quality of the output waveforms. The developed system is implemented on a laboratory scale prototype and the results are presented in the next subsection.

4.2 *Experimental set-up and results*

The proposed system is implemented on 1.5 kW, 240 V, laboratory scale set-up shown in Fig. 10. The wind turbine is emulated using a servo motor and programmable control drive to control the speed. This acts as the wind turbine rotor and is coupled with an eight-pole PMSG. The PMSG is connected to a VSC which is SiC-based three-phase converter, formed by CREE CCS020M12CM2 and CREE CGD15FB45P. The VSC is connected to boost CSI which is formed using Fuji FGW85N60RB, RB-IGBTs. The circuit parameters used for this verification are given in Table 2. The system is run to feed a stand-alone load. The generator is run at 450 rpm from the wind turbine emulator to generate ∼45 V line-to-line rms voltage. The boost CSI is controlled to maintain 208 V line-to-line rms at the load. The steady-state system output waveforms are presented in Figs. 11 and 12. The generator output line current and line-to-line voltage waveforms are shown in Figs. 11*a* and *c*. The respective fast Fourier transform (FFT) spectrum is presented in Figs. 11*b* and *d*. It can be observed from Fig. 11 that the low-order harmonics have been eliminated from the generator line current and voltage. The THD of the current is computed to be ∼3.54%. Fig. 12 shows the waveforms and FFT spectrum of the load current and load line-to-line voltage. The THD of the line current is computed to be ∼3.1%. The THD of the voltage is computed to be ∼2.9%. It can be observed from Figs. 11 and 12 that the proposed system is capable of supplying power to a load from a low-voltage generator without any component on the dc-side.

The results presented in this section establish the feasibility of the developed DDWT topology and its controllers. Furthermore, the absence of dc-bus capacitors or dc-link inductor does not compromise the quality of the system output. It can be observed from the presented results that the generator used for the validation is a low-voltage generator rated for 0.652 p.u. with the grid being at 1.0 p.u. voltage. Notice that the existing topologies of DDWTs require the generator to be rated at ∼1.2 p.u. in order to be connected to grid at 1.0 p.u. voltage. It can be further observed from the presented results that the system output quality is not compromised in the proposed topology and thus establishing that the proposed topology of DDWTs is capable of providing similar performance as existing systems along with reduction in weight and volume of the PMSG and increased reliability. Further investigations will be needed to adopt this new technology for DDWTs.

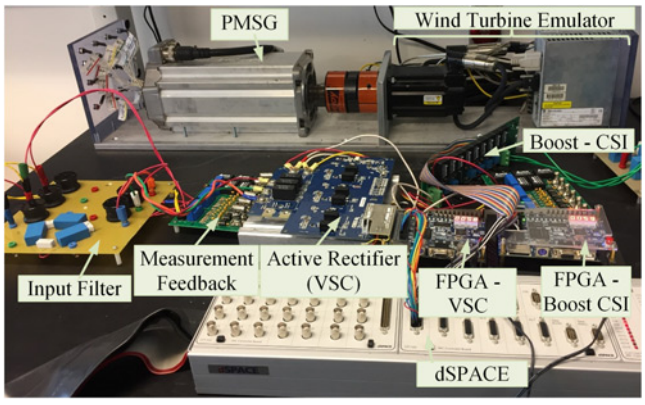

Fig. 10 *Laboratory scale 1.5 kW set-up of the proposed DDWT topology*

Table 2 Circuit parameter values for experimental verifications

L_s	C_{ac}	L_{ac}	$f_{s,VSC}$	$f_{s,CSI}$
3 mH	20 μF	5 mH	25 kHz	6 kHz

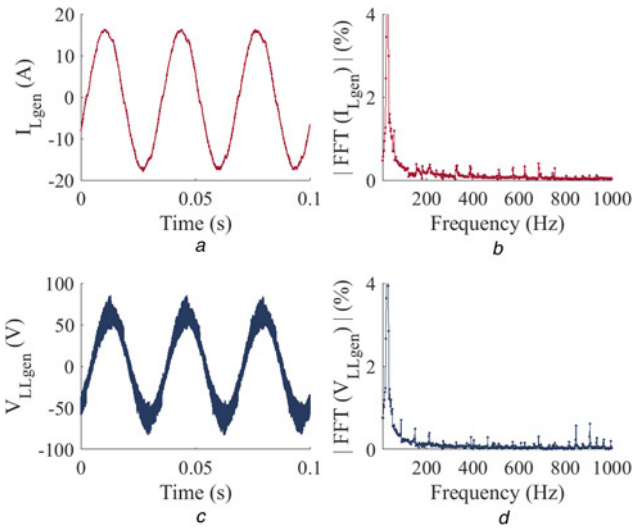

Fig. 11 *Experimentally obtained generator output*
a Line current waveform
b Line current FFT spectrum
c Line-to-line voltage waveform
d Line-to-line voltage FFT spectrum for the system when supplying ∼856 W active power to a three-phase stand-alone load

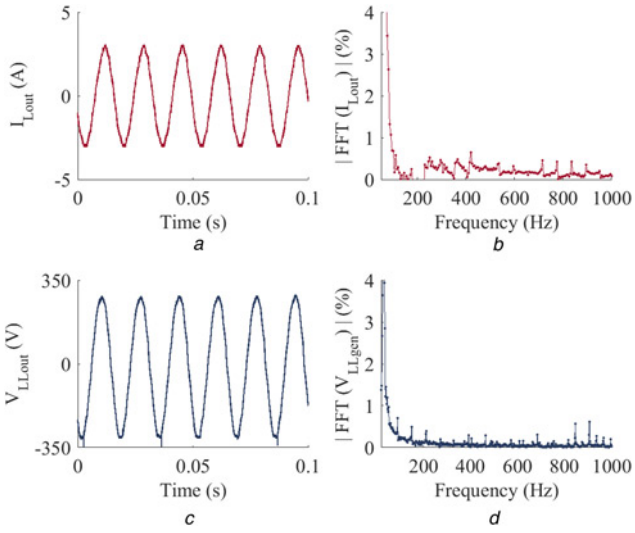

Fig. 12 *Experimentally obtained load*
a Line current waveform
b Line current FFT spectrum
c Line-to-line voltage waveform, and
d Line-to-line voltage FFT spectrum for the system when supplying ∼856 W active power to a three-phase stand-alone load

5 Conclusion

In this paper, an indirect boost matrix converter utilising the current source boost inverter and a low-voltage generator has been introduced for DDWTs. The grid-side VSC in the power electronics interface of a traditional DDWT has been replaced by the boost CSI. The CSI topology helps in the elimination of the dc-bus electrolytic capacitors while the inherently needed dc-link inductor has been eliminated by utilising the synchronous inductance of the PMSG. This will increase the reliability of the system and decrease the overall system down time that will have significant impact on the maintenance costs, especially for offshore wind turbines. The control technique for the developed power electronics interface has been developed and their operation has been verified through simulation results. Some primary verifications of the overall system performance have been presented through simulation results in this paper. The steady-state system performance has also been experimentally verified and it has been demonstrated that the quality of output waveforms is satisfactory.

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