DESIGN AND ANALYSIS OF A QUASI-PARALLEL REGULATED SWITCHED-CAPACITOR CONVERTER

by

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Abstract

In this research, a method to regulate switched-capacitor converters (SCC) by utilizing a regulated magnetic converter in a quasi-parallel configuration is proposed, analyzed, and experimentally verified for a telecommunication power supply application. The proposed quasi-parallel regulated switched-capacitor converter (SCC) has the advantages of high efficiency, high conversion ratios, and high power density typical of unregulated switched-capacitor converter while achieving both line and load regulation. The magnetics required for the regulating converter are greatly reduced in cost and physical size due to the low voltages, high switching frequency, and partial power property of the regulating converter.

This research analyses the small-signal behavior of SCC and proposes an averaged small-signal circuit model for reduced-order models of SCC. The small-signal circuit model of SCC is then utilized to provide analysis of the proposed converter. The analysis demonstrated that besides the benefit of inherent feedback due to the quasi-parallel configuration, the control strategy for the proposed converter can be designed in the same fashion as typical PWM converters either as buck or boost converters.

Datacenter power consumption makes up two percent of United States electricity consumption or 80TWhr. Roughly half of this energy is spent on cooling or lost in power conversion. Further, as data centers try to maximize compaction, the need for small and highly efficient power supplies is enhanced. Telecom power supplies often rely on large and lossy transformers to achieve large conversion ratios or to provide isolation. By utilizing a quasi-parallel regulated switched-capacitor converter, the magnetics can be removed while achieving high efficiency and power density. A 120W prototype of the proposed converter is built for a 48V to 12V telecom power supply and achieves efficiencies of 94% at 50% rated power and 93% at the full rated power. The proposed converter is shown to achieve desired load regulation and limited line regulation. The converter is experimentally shown to operate from 36V to 52V. Improvements in the efficiency, power density, and implementation of the proposed converter are included with the concluding remarks at the end of this thesis.

Keywords: switched-capacitor converter, quasi-parallel, input-series, output-parallel, sigma, small-signal analysis, MMSCC, multilevel modular switched-capacitor converter, switched-capacitor converter regulation

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Chapter 1 Introduction

1.1 Motivation

Switched-capacitor converters (SCC) offer high conversion ratios, high efficiencies, and high power density. Their primary advantage is the ability to achieve power conversion without the use of magnetics which are bulky and lossy compared to capacitors. Disadvantages of SCC are that they suffer from limited load regulation, line regulation, and discontinuous conversion ratios. Additionally, by regulating, SCC decrease their efficiency, while only unregulated SCC can achieve the high theoretical efficiencies.

Regulation strategies, such as switching frequency modulation, duty cycle modulation, sliding voltage mode control, and adaptive on-time control have been proposed for SCC. However, these strategies have all achieved limited regulation, while providing continuous conversion ratios, and retaining the high power density and high conversion ratio advantages of SCC. These regulation approaches all suffer from lower efficiencies.

In order for SCC to be competitive, a regulation strategy that does not degrade its efficiency is required. By using a regulating cascaded magnetic converter, the SCC can operate unregulated retaining all of its advantages, while still achieving line and load regulation. In a step-down converter the regulating converter will see reduced voltages allowing for higher switching frequencies and smaller sized magnetics. The disadvantage is that the regulating magnetic converter must have the same power rating as the SCC, limiting the reduction of the magnetic's size.

The approach proposed in this thesis will allow a SCC to operate unregulated while a partial-power inductor based converter provides regulation. The partial-power property implies that the converter only converts a small portion of the total output power from the input. This allows for a reduced power rating of the regulating converter enabling further reductions to the magnetic's size. This provides the advantages of high efficiency and high energy density of a SCC and achieving line and load regulation through the use of a small inductor based converter.

1.2 Datacenter Application

In 2010, datacenters consumed two percent of all United States electric usage [1]. The 2010 U.S. electrical energy consumption was roughly 4TWh according to www.eia.gov, thus approximately 80TWh was consumed by datacenters. More than half of this consumed energy is lost in power conversions, distribution, and cooling devices [2]. The primary cost of a datacenter is no longer the cost of the servers, but the cost of electricity and cooling [3]. Ten years ago large datacenters required 10MW of power, resulting in $8 million being spent on electricity and another $3-$5 million on cooling [3].

In datacenters and telecom applications, the efficiency and size of the power electronics is extremely important. With so much energy and money spent on cooling, it is important that the power supplies for servers have high power density and increased efficiency to minimize losses in power conversion and cooling costs. A major contributor to energy losses and power supply size are transformers and other magnetic devices. Switched capacitor converters (SCC) offer lightweight, small size, and high power density [4] without the use of magnetic components. Improvements in SCC topologies have reduced component stresses, capacitance, and peak current charging allowing for the design of kilowatt power SC converter [5-11]. SCC, such as the Multilevel Modular Switched Capacitor DC-DC Converter (MMSCC) [5], have achieved zero current switching (ZCS) and efficiencies above 95% in the kilowatt range [5-9].

Due to the high efficiency and large conversion ratios attainable by SCC, a telecommunications power supply is an excellent application of the QRPSCC. In most datacenters 48V (36V to 72V range) is applied to server racks, where each rack will have DC/DC converter to step down the 48V to 12V. Common sizes, in inches, for these DC/DC converters are full brick 4.6″x2.4″x0.5″, half brick 2.3″x2.4″x0.35″, and quarter brick 2.3″x1.45″x0.35″. Power ratings range from 50-720W for these sizes [12], with 720W attained in half bricks [13], 180W in an eighth brick [14]. Future telecom power supplies will require high power density (180W/in^3), high reliability, and fast transient responses [15-17].

The QPRSCC can be designed for the 48V to 12V DC/DC power converter. The use of ceramic capacitors will provide increased reliability compared to electrolytic capacitors which are known to dry out after several years. The QPRSCC will provide a highly efficient and high power density converter for the datacenter server racks.

1.3 Summary of Chapters

Chapter 1 has presented the motivation for this research. The choice of a datacenter application has been explained and the voltage requirements presented.

Chapter 2 provides the state-of-the-art review for SCC modeling, dynamic analysis, design, and regulation strategies. The limitations and merits of current regulation strategies are discussed.

In Chapter 3 the quasi-parallel regulated switched-capacitor converter is presented explaining the basic operation and advantages over other regulation approaches for SCC. The selection, design, and modeling of the SCC and the regulating magnetic converter is documented. A proposed averaged small-signal model for SCC based of a reduced-order model is presented and analyzed.

In Chapter 4 the QPRSCC is modeled and analyzed showing the steady-state and dynamic characteristics. The expected losses are calculated and presented, demonstrating the high efficiency of the QPRSCC. Steady-state and transient response simulations are performed in LTSpice and documented for the proposed converter.

Chapter 5 provides the final design choices and presents the experimental prototype. The results of steady-state, efficiency, and transients tests are presented demonstrating the promise of the QPRSCC.

Chapter 6 presents the highlights of the research and experimental results. Recommendations for future revisions are suggested in an effort to increase the power rating and efficiency.

Chapter 2 State-of-the-Art Review

There has been a renewed interested in Switched-Capacitor Converters (SCC) for power applications due to their high conversion ratios, high efficiencies, and high power density without the use of magnetics. The popularity of SCC has lead to new topologies and applications in DC-AC, AC-DC, AC-AC, and DC-DC converters [5,18,19]. The focus of this work is the application of SCC for DC-DC applications. The proposed technology provides regulation for any DC-DC converters, multiphase or two phase, however, consideration of multiphase SCC is beyond the scope of this work and proved to be more complex than necessary for the purposes of this design. The following overview and work will focus on two phase DC-DC switched-capacitor converters. A basic overview of SCC will be given through steady state and dynamic analyses, including an evaluation of losses in a SCC in section 2.1. Different regulation strategies will be presented in section 2.2 emphasizing that SCC have limited ability to be regulated and attempts to regulate them hurt their efficiency. This will provide the background information for the proposed quasi-parallel configuration for regulating a SCC.

2.1 Overview of DC-DC Switched-Capacitor Converters

Switched-capacitor converters offer lightweight, small size, and high power density [5] without the use of magnetic components. Improvements in switched-capacitor topologies have reduced component stresses, required capacitance, and peak current charging allowing for the design of kilowatt power SCC [5-11]. Switched capacitor converters, such as the Multilevel Modular Switched Capacitor DC-DC Converter (MMSCC) [5], have achieved zero current switching (ZCS) and efficiencies above 95% in the kilowatt range [5-9]. A SCC can also provide ground isolation [20] for certain applications.

The major advantage of the SCC is that it does not utilize magnetics for power conversion, which enables higher power densities. Magnetics are generally large and lossy compared to capacitors for similar power levels. A comparison of energy densities is given in Table 2.1 illustrating the advantage of capacitive energy over magnetic. Capacitors can more easily be implemented in monolithic integration. SCC can also have the advantage of being able to operate at high temperatures [5].

TABLE 2.1: SUMMARY OF INDUCTOR AND CAPACITOR ENERGY DENSITIES

Type	Manufacturer	Value	Dimensions [mm^3]	Energy Density
Ceramic Capacitor	TDK	10μF@10V	2 x 1.25 x 1.45	138μJ/mm^3
Ceramic Capacitor	TDK	10μF@50V	3.2 x 1.6 x 1.8	1206μJ/mm^3
Ceramic Capacitor	Taiyo-Yuden	1μF@35V	1.6 x 0.8 x 0.8	1196 μJ/mm^3
Electrolytic Capacitor	Nichon	330μF@10V	8(dia) x 11.7	28μJ/mm^3
Shielded SMT Inductor	Sumida	12μH@8A	14.5 x 14.5 x 8	0.23μJ/mm^3
Shielded SMT Inductor	Wurth	4.7μH@1.65A	4.8 x 4.8 x 2	0.14μJ/mm^3
Shielded SMT Inductor	Wurth	0.47μH@1A	2.29 x 1.7 x 1.48	0.041μJ/mm^3
Shielded SMT Inductor	Vishay	1μH@11A	6.86 x 6.47 x 3	0.45μJ/mm^3

The basic premise of SCC is to utilize a network of switches and capacitors that can shuttle charge from the input to the output by achieving different charging and discharging states. While some switches can be constructed with diodes, typically MOSFETs are used and with proper gate signals will form a set of subcircuits for charing and discharging. Each state is referred to as a phase. The most common topologies (e.g. series-parallel) are two-phase SCC. The series-parallel topology has two subcircuits, one which charges all the capacitors in series from the input to the output, and the second aligns the capacitors in parallel to discharge to the output. If the series-parallel SCC is unregulated each phase will have a 50% duty cycle. Depending on the number of capacitors and the direction of power flow the series-parallel can achieve a step up or step down conversion ratio that is set by the number of capacitors.

Each SCC has an ideal discrete conversion ratio that is determined by the topology, resulting in an unloaded output voltage proportional to the input voltage. Some SCC can be designed to alter their conversion ratio dynamically such as in [5-8,21]. Without regulation the output voltage will decrease with increased load, essentially acting like DC transformers with a set output resistance. The theoretical maximum efficiency achievable for a SCC is dependent on its ideal conversion ratio n:1, the input voltage, and the output voltage given as (2.1).

$$\eta_{SCC} = \frac{nV_o}{V_{in}} \tag{2.1}$$

For an unregulated SCC with increasing load the output voltage will drop due to either capacitive charging losses or resistive losses leading to decreased efficiency.

One problem with SCC as power converters is their limited regulative abilities. A SCC is most efficient when unregulated and operating at its ideal conversion ratio as evident by (2.1). Without regulation the

output voltage will vary proportionally with the input voltage and droop with high loads. Unique topologies and use of regulation techniques as in [22] and [23] provide line and load regulation but at the expense of efficiency. Regulating a SCC away from its ideal conversion ratio drastically reduces its efficiency. For example with 12V input and desired 5V output the SCC can be 83.3% efficient at best. To achieve its theoretical maximum efficiency a SCC it must be unregulated. To utilize the advantages of an unregulated SCC, some power converters implement cascaded or merged buck converters as proposed in [24] to provide regulation. These topologies suffer losses in both stages leading to decreased overall efficiency. In addition, both stages are required to have the same power rating, increasing the physical size of the converter.

2.1.1 Steady State Modeling and Analysis

The typical steady state model of a SCC is illustrated in Fig. 2.1, consists of a DC transformer with a turns ratio, n, dictated by the SCC conversion ratio followed by a series output impedance R_o.

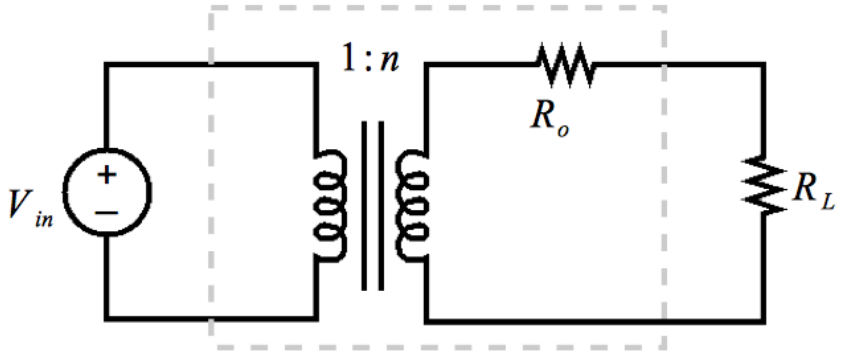


Fig. 2.1 Steady-state model of a SCC with a DC transformer and output impedance

The output impedance, R_o, is an equivalent resistance representing losses due to capacitive losses and parasitic resistances of the circuit (e.g. MOSFET on resistances, PCB trace resistance, and capacitors equivalent series resistance (ESR)). An effective, quick, and simple method for calculating this equivalent output impedance is presented in [21,25-27]. The equivalent output impedance can be determined by inspection of the SCC topology allowing for easy comparison of different SCC topologies. The design and optimization methodologies for this approach are provided in [25,27].

The equivalent output impedance has two asymptotic limits, the slow switching limit (SSL) and the fast switching limit (FSL), in relation to the switching frequency as depicted in Fig. 2.2.

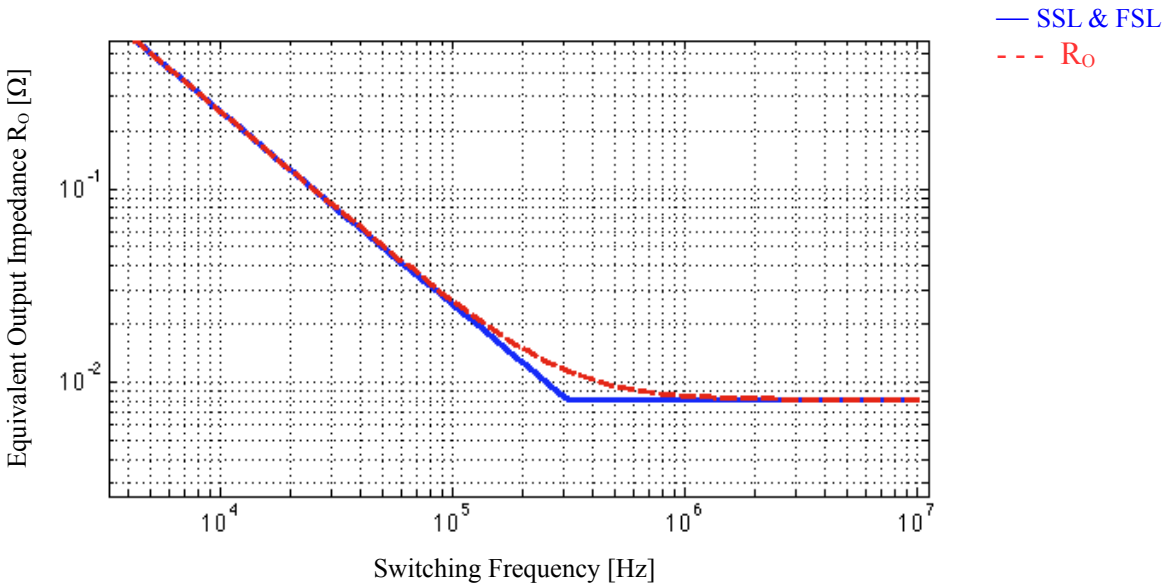


Fig. 2.2 Equivalent output impedance showing the SSL and FSL asymptotic limits

For SSL the output impedance is dominated by capacitive charging losses and is dependent on the switching frequency and the capacitance of the switching capacitors. In this limit, the capacitors are allowed to charge to voltage equilibrium within the duty cycle and the current can be modeled as an impulse. In the FSL, the output impedance is dominated by the charging and discharging resistive conduction losses. While the model presented in [25,27] only considers the switch's on-resistance the capacitor ESR and PCB trace resistances can easily be incorporated into the model, introducing minimal added complexity [28]. In the FSL, the capacitors have a constant voltage and the current is considered constant within the duty cycle.

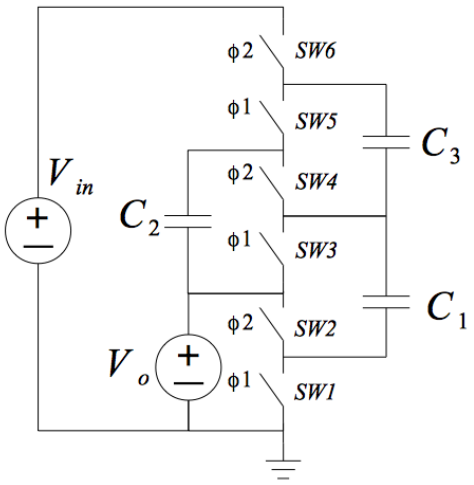
The calculation of the output impedance, R_o, in the SSL will be detailed in subsection A and the calculation of it in the FSL will be detailed in subsection B. For switching frequencies near the intersection of the asymptotic limits an approximate model is presented in [28] and will be briefly discussed in subsection C. As previously mentioned, the equivalent output impedance only represents conduction losses and does not include switching losses or gate drive loss. Such losses can be incorporated into the model as a parallel resistance as in [19]. Switching loss analysis will be covered in section 2.1.3.

A. SSL

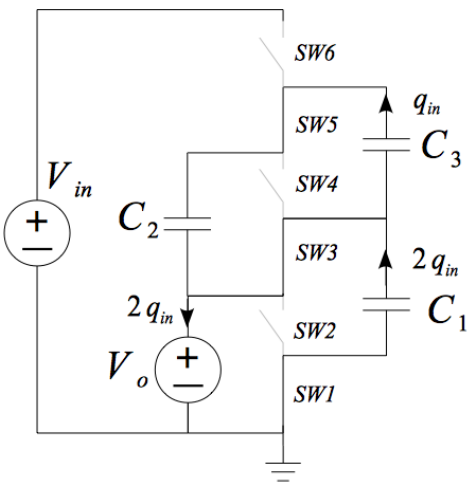
Within the asymptotic slow switching limit (SSL) the output resistance, R_{SSL}, is given by (2.2) for a properly defined *m*-phase SCC

$$R_{SSL} = \sum_{i \in caps} \sum_{j=1}^{m} \frac{\left(a_{c,i}^{j}\right)^2}{2 C_i f_{SW}} \tag{2.2}$$

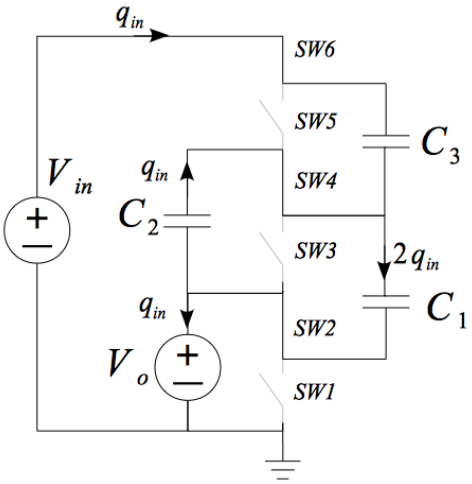
The symbol i is the number of switching capacitors, C_i is the capacitance of switching capacitor C_i, f_{SW} is the switching frequency, and $\boldsymbol{a}_{c,i}^{j}$ is called the charge multiplier vector. The charge multiplier vector $\boldsymbol{a}_{c,i}^{j}$ represents the ratio of the charge flow per switching period that flows through capacitor C_i to the charge flow to the output per switching period in the phase j. As an example, consider the simple two phase 3:1 Ladder SCC, depicted in Fig. 2.3(a). It will operate with a switching frequency of 250kHz and each phase will be given a nominal duty cycle of 50%. The phases 1 and 2 are shown in Fig. 2.3(b) and (c) respectively.



(a) 3:1 Ladder Switched-Capacitor Converter



(b) Charge flow during Phase 1



(c) Charge flow during Phase 2

Fig. 2.3 (a) Schematic of the 3:1 Ladder SCC and the charge flows in (b)Phase 1 and (c)Phase 2

The charge multiplier vectors can be derived using Kirchhoff's current law (KCL) constraints and using the fact that the charge multiplier vectors for each phase are equal and opposite as outlined in [25]. The charge vectors can also be found by inspection of the two-phase SCC by following the charge transfer and that the charge flow into a capacitor in one phase flows out in the next phase.

During phase 2, shown in Fig. 2.3(c), capacitor C_3 is charged with charge q_{in} from the input voltage source. During phase 1 capacitor C_3 will discharge q_{in} into capacitor C_2. Returning to phase 2, C_2 must discharge q_{in} resulting in a total of $2q_{in}$ transferring into capacitor C_1. At this point, analysis of each phase through KCL gives the total charge transferred to the output in one period given by (2.3).

$$q_{out} = 3\, q_{in} \tag{2.3}$$

This relation provides the normalization of the charge multiplier vector but also gives the conversion ratio of the SCC. The charges q_{in} and q_{out} are proportional to I_{in} and I_{out}, giving (2.4) and since power in must equal power out (in the ideal case) the voltage conversion ratio will be (2.5).

$$\frac{I_{out}}{I_{in}} = 3 \tag{2.4}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{3} \tag{2.5}$$

With the charge flows known, and denoted as in Fig. 2.3(b)&(c) the capacitor charge multiplier vectors can easily be written as in (2.5) and (2.6). For a two phase SCC, the capacitor charge multiplier vectors must be equal and opposite.

$$\boldsymbol{a}_c^1 = \begin{bmatrix} -2 & 1 & -1 \end{bmatrix} \frac{q_{in}}{q_{out}} = \begin{bmatrix} -\frac{2}{3} & \frac{1}{3} & -\frac{1}{3} \end{bmatrix} \tag{2.6}$$

$$\boldsymbol{a}_c^2 = \begin{bmatrix} 2 & -1 & 1 \end{bmatrix} \frac{q_{in}}{q_{out}} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & \frac{1}{3} \end{bmatrix} \tag{2.7}$$

With the capacitor charge multiplier vectors so defined, (2.2) can be solved for the expected equivalent output impedance in the SSL, R_{SSL}. If it is assumed that each switching capacitor has the same capacitance (2.2) can be simplified to (2.8)

$$R_{SSL} = \frac{1}{2\, C\, f_{SW}} \sum_{i \in caps} \sum_{j=1}^{m} \left(a_{c,i}^{j} \right)^2 \tag{2.8}$$

Solving (2.8) gives the SSL output impedance related to the capacitance and switching frequency (2.9).

$$R_{SSL}=\frac{1}{2C f_{SW}}\left[\left(\frac{4}{9}+\frac{1}{9}+\frac{1}{9}\right)+\left(\frac{4}{9}+\frac{1}{9}+\frac{1}{9}\right)\right]=\frac{2}{3C f_{SW}} \tag{2.9}$$

Calculating (2.9) with a given capacitance of 40μF for each capacitor and a 250kHz switching frequency, then R_{SSL} = 2/30 Ω.

From (2.9) it can be seen that the charge multiplier vectors from each phase, when squared, become equal. For two-phase SCC equation (2.2) can be reduced to (2.10) which is presented in [25].

$$R_{SSL}=\sum_{i\in caps}\frac{\left(a_{c,i}\right)^2}{C_i f_{SW}} \tag{2.10}$$

There is also a method to optimize the capacitance of each switching capacitor presented in [25,27,28]. For a given R_{SSL} and switching frequency each capacitance can be optimally sized to provide the lowest total capacitor energy storage. The total energy E_{TOT} is given by (2.11).

$$E_{tot}=\sum_{i\in caps}\frac{1}{2}C_i\left(v_{c,i(rated)}\right)^2 \tag{2.11}$$

The symbol $v_{c,i(rated)}$ is the rated voltage of the capacitor, which is at minimum, the voltage of the blocking voltage. In the ladder topology shown in Fig. 2.3(a), each capacitor has a steady state blocking voltage equal to the output voltage. For this example, let the output voltage be 1V. The optimally sized capacitance is then given by (2.12).

$$C_i=\left|\frac{a_{c,i}}{v_{c,i(rated)}}\right|\frac{2E_{TOT}}{\sum_{k\in caps}\left|a_{c,k}v_{c,k(rated)}\right|} \tag{2.12}$$

Using (2.12) R_{SSL} is then described by (2.13).

$$R_{SSL}=\frac{1}{2E_{TOT}f_{SW}}\left(\sum_{i\in caps}\left|a_{c,i}v_{c,i(rated)}\right|\right)^2 \tag{2.13}$$

Continuing with this example, if R_{SSL} = 2/30 Ω is the value desired, with a switching frequency of 250kHz, then from (2.13) the total energy E_{TOT} is calculated to be 4/75 μJ. Now using (2.12), the optimal sizes are C_1 = 53.3μF, C_2 = 26.7μF , and C_3 = 26.7μF. By minimizing the total energy E_{TOT}, the area taken by discrete capacitors or integrated capacitors is minimized as well. The total capacitor energy is approximately proportional to the printed circuit board (PCB) area used by discrete capacitors or to the silicon area used for integrated capacitors. This optimization methodology can be used to

achieve the smallest PCB area for a given design.

The series output impedance R_{SSL} represents the capacitive losses caused by the charging and discharging cycles. This impedance is easily obtained through inspection of the SCC and finding the capacitor charge vectors. From (2.2) it is evident that R_{SSL} is inversely proportional to the switching frequency so with increasing switching frequency the output impedance will decrease. The SCC output impedance will continue to decrease along the SSL asymptote until reaching FSL asymptote. The FSL asymptote provides the output impedance when the SCC is operating such that the conduction losses are due to the resistances of the switches, capacitors, or parasitics.

B. FSL

In the fast switching limit (FSL), the current flow between capacitors is considered to be constant and the capacitor's voltage remains constant. The circuit loss is solely due to the conduction loss in any of the modeled resistive elements (e.g. MOSFETs, parasitic resistance). The equivalent output impedance, R_{FSL}, in the asymptotic fast switching limit is given by (2.14) .

$$R_{FSL} = \sum_{i \in caps} \sum_{j \in phases} \frac{R_i}{D_j} \left(a_{r,i}^{j} \right)^2 \tag{2.14}$$

The symbol R_i is the resistance of switch S_i or other parasitic resistances, D_j is the duty ratio of the jth phase, and $\boldsymbol{a}_{r,i}^{j}$ is the resistive charge multiplier coefficient. The resistive charge multiplier coefficient, $\boldsymbol{a}_{r,i}^{j}$,is the ratio of the charge flow per period in switch S_i in phase j and the total output charge flow per period. The resistive charge multiplier vector can be found in the same manner as the capacitor charge multiplier vector $\boldsymbol{a}_{c,i}^{j}$ in the SSL. Analysis of the charge flow has already been performed for the SSL and shown in Fig. 2.3(b)&(c). Considering this as a unidirectional converter, with power flowing from input to output, the sign of each element in $\boldsymbol{a}_{r,i}^{j}$ indicates the direction of current flow with respect to the blocking voltage of the switch. Switches with negative charge flow can be implemented with a diode if the losses due to the forward voltage drop are acceptable. From Fig. 2.3(b) the phase 1 resistive charge multiplier vector is (2.15) and from Fig. 2.3(c) the phase 2 resistive charge multiplier vector is (2.16).

$$\boldsymbol{a}_r^1 = \begin{bmatrix} -\frac{2}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 \end{bmatrix} \tag{2.15}$$

$$\boldsymbol{a}_r^2 = \begin{bmatrix} 0 & -\frac{2}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} \end{bmatrix} \tag{2.16}$$

Using the resistive charge multiplier vectors just defined and assuming each phase has a duty cycle of 50% and each switch on-resistance is 10mΩ, then the asymptotic FSL output impedance can be calculated using (2.17).

$$R_{FSL} = 2\,R_{ds-on}\left(\left(\frac{4}{9}+\frac{1}{9}+\frac{1}{9}\right)+\left(\frac{4}{9}+\frac{1}{9}+\frac{1}{9}\right)\right) = 2\,R_{ds-on}\,\frac{12}{9} = \frac{8}{3}R_{ds-on} = \frac{80}{3}m\,\Omega \tag{2.17}$$

Calculation of R_{FSL} thus far has only considered the resistances of the switches. In order to model parasitic resistances, such as capacitor ESR or PCB trace resistance, another term can be added to (2.14). In [28] capacitor ESR is added to the original model giving (2.18) where R_{FSLm} is the modified FSL output impedance.

$$R_{FSLm} = R_{FSL} + \sum_{i \in caps} R_{ESR,i}\left(a_{c,i}\right)^2\left(\frac{1}{D}+\frac{1}{(1-D)}\right) \tag{2.18}$$

The modified FSL output impedance, shown in (2.18), is for only two-phase SCC but can easily be extended and written for multi-phase SCC. Other parasitic resistance such as PCB trace resistance can be modeled as resistances in series with the switches or the capacitor ESR. These resistances can then be combined eliminating the need to add other terms to (2.18).

As with the SSL there is also an optimization methodology for minimizing the total switch size. The total switch size A_{TOT} is roughly proportional to the area for integrated circuits. This may not hold true for discrete switches but the optimal resistance for each switch can still be found. Knowing the optimal resistance for each switch enables proper selection of switches by choosing either a smaller package switch or lower gate charge. From [25,27,28] the total switch size A_{TOT} is given by (2.19).

$$A_{tot} = \sum_{i \in switches} G_i\left(v_{r,i(rated)}\right)^2 \tag{2.19}$$

Where G_j is the conductance of the switch S_j and $v_{r,i(rated)}$ is the switches rated voltage, which again needs to be at least the blocking voltage. Equation (2.19) assumes standard behavior of CMOS and LDMOS switches, if the actual devices do not adhere to this assumption a modified form is available and can be investigated in [28].

If only switch resistances are considered and one assumes the SCC is a two-phase SCC with equal duty cycles of D, then the optimal switch conductance is given by (2.20).

$$G_i = \left| \frac{a_{r,i}}{v_{r,i(rated)}} \right| \frac{A_{TOT}}{\sum_{k \in switches} \left| a_{r,k} v_{r,k(rated)} \right|} \tag{2.20}$$

The asymptotic fast switching limit output impedance R_{FSL} can then be expressed as (2.21).

$$R_{FSL} = \frac{1}{D\, A_{TOT}} \left(\sum_{i \in switches} \left| a_{r,i} v_{r,i(rated)} \right| \right)^2 \tag{2.21}$$

Given a desired R_{FSL} and duty cycle, the required minimum total switch area can be found from (2.21) and subsequently used in (2.20) to find the optimal conductance of each switch. Although this optimization methodology is geared towards integrated switches, insight from the optimal conductances can lead to smarter selection of discrete switches.

Unlike in the SSL, the output impedance in the FSL asymptote is solely dependent on the resistances of the switches and other parasitic resistances modeled. Switching frequency and capacitance are no longer factors in the FSL asymptote. The R_{FSL} sets the minimum possible output impedance i.e. the maximum theoretical efficiency.

C. Approximated Total Output Impedance

The total output impedance of a SCC is bounded by the asymptotic SSL and FSL derived in subsections A and B. For either the SSL or the FSL, the output impedance is easily determined by the calculated RS_{SL} and R_{FSL} as long as the assumptions made in each limit hold true. As the switching frequency reaches the intersection of the SSL and FSL asymptotes, the converter is not operating in neither the SSL nor the FSL and the assumptions made for the impedance calculations no longer hold. In [27] an approximation of the total impedance is given as (2.22).

$$R_o \approx \sqrt{R_{FSL}^2 + R_{SSL}^2} \tag{2.22}$$

This approximation is compared to the calculated output impedance for a simple SCC and found to be reasonably close and suitable as an estimate for design purposes [27]. Another method to calculate the equivalent output impedance of a SCC is presented in [29] using discrete state-space averaging. This produces a model that describes the dynamics of the SCC and will be given in Section 2.1.2. A comparison of SSL and FSL modeling along with the discrete state-space averaging method will be given in Section 2.1.2, and will show that they are in good agreement.

2.1.2 Dynamic Modeling

As switched capacitor converters (SCC) moved into the power conversion realm, accurately modeling their dynamics became much more important for controlling and understanding their behavior. A common approach is to use state-space averaging (SSA) as in [30]. While this method is able to capture the SCC dynamics, SSA is unable to accurately capture the switching frequency dependency of the output impedance. In state-space analysis, the state variables are the capacitor's voltages and the governing state-space equations are obtained from each state of the SCC. These state-space equations are then written as in (2.23).

$$\dot{X}(t) = A_j X(t) + B_j U(t) \tag{2.23}$$

where *X(t)* are the state variables (e.g. the capacitor voltages) and *U(t)* are the system inputs (e.g. input voltages, load current). The matrices A_j and B_j are defined for each *j*th state of the SCC. The SSA method averages the matrices as shown in (2.24).

$$A_{avg} = \frac{\left(\sum_{j \in states} A_j t_j \right)}{T_s} \qquad B_{avg} = \frac{\left(\sum_{j \in states} B_j t_j \right)}{T_s} \tag{2.24}$$

In (2.24) t_j is the time spent in the state *j* and T_s is the switching period. The averaging method simply multiplies each state by its duty cycle. The duty cycle is switching frequency independent and any attempts to model the steady state output impedance will only result in one value regardless of switching frequency. As stated in section 2.1.1 this result is undesirable and a better method for analyzing the SCC is needed.

In [31] a modeling method is proposed that captures the steady state output impedance as well as the large and small signal dynamics. This approach is able to provide a circuit model that can be used for SPICE simulations. This method works for hard-switched, multi-phase, and multi-capacitor SCC. A necessary requirement is that the each of the sub-circuits (each phase of the SCC) must be able to be modeled or approximated as a first-order RC circuit network which as shown in [32] is possible for most SCC.

Another method for dynamic modeling of SCC is presented in [29,33] and is able to accurately model the dynamics of SCC and the switching frequency dependency of the output impedance. The proposed method from [29,33] uses discrete state-space averaging (DSSA) to model the SCC and can be directly and most easily applied to quasi-steady-state SCC irregardless of their complexity. The method

presented in [29] can be extended to regulated converters but will not be covered in this paper. The work done in [34] shows how the DSSA approach to dynamic modeling from [33] can be used for duty cycle regulation. The disadvantage of this approach is that it only generates discrete numerical results and not analytical solutions.

A brief overview of the dynamic model presented in [33] using DSSA will be covered in subsection A. If a more in-depth look is desired it can be found in both [29,33]. The DSSA dynamic model approach will be applied to the two-phase 3:1 ladder SCC used as an example in section 2.1.1. A comparison of the static output impedance found through DSSA will be compared to the output impedance model found using that approach (the SSL and FSL output impedances) will be shown in subsection B. Finally, subsection C will demonstrate, as presented in [29], that a reduced order model can be used to represent the dynamics of a complex multi-capacitor SCC.

A. Dynamic Modeling Using DSSA

Consider a general SCC modeled as a black box with an output stage and a load modeled as a Thévenin equivalent circuit as shown in Fig. 2.4. The black box SCC has *n* capacitors, whose voltages are elements in vector **v** and the capacitors' currents are elements of vector **i**. The two vectors **v** and **i** can be related by (2.25).The matrix **C** is a diagonal matrix where the element C_{jj} is the capacitance of capacitor *j*.

$$\mathbf{i} = \mathbf{C}\dot{\mathbf{v}} \tag{2.25}$$

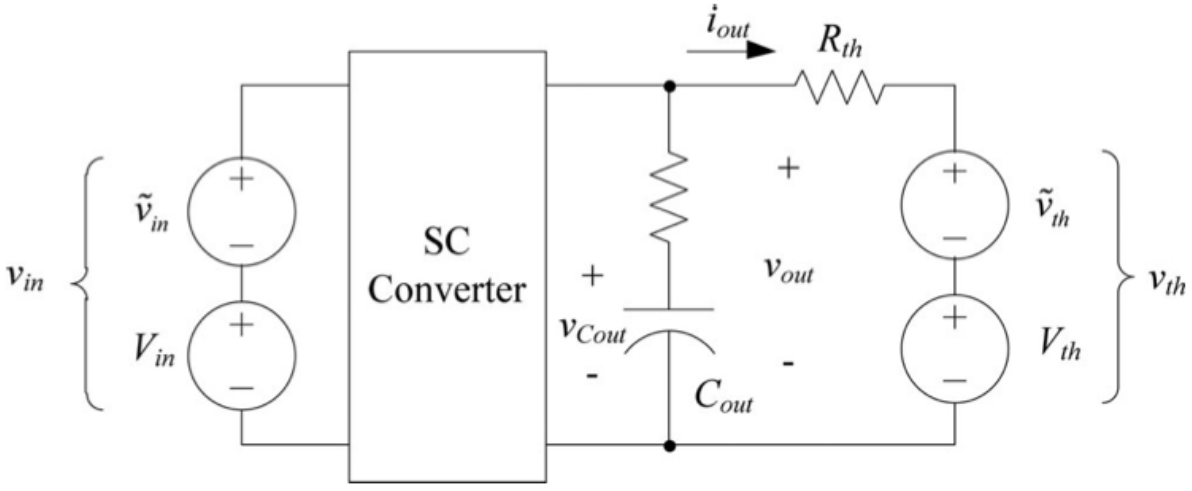


Fig. 2.4 Switched-capacitor converter with Thévenin equivalent load and output stage as in [29]

The vectors **i** and **v** and the matrix **C** represent the current and voltages and the capacitances of the capacitors in the SCC. These vectors can be modified to incorporate the output capacitor of the output

stage. The modified vectors are defined in (2.26).

$$\hat{\mathbf{i}}=\begin{bmatrix}\mathbf{i}\\ i_{Cout}\end{bmatrix}\quad \hat{\mathbf{v}}=\begin{bmatrix}\mathbf{v}\\ v_{Cout}\end{bmatrix}\quad \hat{\mathbf{C}}=\begin{bmatrix}\mathbf{C} & 0\\ 0 & C_{out}\end{bmatrix} \tag{2.26}$$

The system input vector is given as $\mathbf{u}=\begin{bmatrix}v_{in} & v_{th}\end{bmatrix}^T$. For each switching state, $j\in\{1,\ldots,m\}$, Kirchhoff's current and voltage laws (KCL and KVL) may be applied resulting in n+1 equations (number of capacitors in the SCC and the output capacitor). The equations can then be expressed as m matrix equations of the form

$$\hat{\mathbf{E}}_j\hat{\mathbf{i}}+\hat{\mathbf{F}}_j\hat{\mathbf{v}}+\hat{\mathbf{G}}_j\hat{\mathbf{u}}=0 \tag{2.27}$$

The matrices $\mathbf{E}_j$, $\mathbf{F}_j$, and $\mathbf{G}_j$ are the result of analysis of the jth switching state through KCL and KVL. The individual rows are a result of either KVL or KCL, but not both. For rows due to KVL, entries in **E** are resistances and entries in **F** and **G** are +1, -1, or 0 as voltage drops are summed around the loop. Rows due to KCL yield entries in **E** that are either +1, -1, or 0 and entries in **F** and **G** are all zero as currents are summed at a node.

From (2.27) the matrices $\mathbf{E}_j$, $\mathbf{F}_j$, and $\mathbf{G}_j$ are used to find the matrices $\mathbf{A}_j$ and $\mathbf{B}_j$ using (2.28) and (2.29) to write m continuous-time state-space equations (2.30).

$$\hat{\mathbf{A}}_j=-\hat{\mathbf{C}}^{-1}\hat{\mathbf{E}}_j^{-1}\hat{\mathbf{F}}_j \tag{2.28}$$

$$\hat{\mathbf{B}}_j=-\hat{\mathbf{C}}^{-1}\hat{\mathbf{E}}_j^{-1}\hat{\mathbf{G}}_j \tag{2.29}$$

$$\dot{\hat{\mathbf{v}}}=\hat{\mathbf{A}}_j\hat{\mathbf{v}}+\hat{\mathbf{B}}_j\hat{\mathbf{u}} \tag{2.30}$$

Once defined as a continuous-time dynamic model the model is converted to a discrete-time dynamic model as detailed in [35] as implemented in MATLAB by the `c2d` function. The sample time of the jth dynamic model is the time spent within the switching period in that subcircuit. This sample time t_j is typically represented by the duty cycle, D_j, multiplied by the switching period T_S. The discrete-time state-space equations are of the form defined by (2.31).

$$\hat{\mathbf{v}}[k+1]=\hat{\mathbf{\Phi}}_j\hat{\mathbf{v}}[k]+\hat{\mathbf{\Gamma}}_j\hat{\mathbf{u}}[k] \tag{2.31}$$

These m dynamic models can be combined into a single dynamic model with a sample period of T_S. The discrete-time dynamics of the SCC at every switching period is as given in (2.32).

$$\hat{\mathbf{v}}[k+1]=\hat{\mathbf{\Phi}}\hat{\mathbf{v}}[k]+\hat{\mathbf{\Gamma}}\hat{\mathbf{u}}[k] \tag{2.32}$$

where

$$\hat{\mathbf{\Phi}} = \hat{\mathbf{\Phi}}_m \hat{\mathbf{\Phi}}_{m-1} \ldots \hat{\mathbf{\Phi}}_1 \tag{2.33}$$

$$\hat{\mathbf{\Gamma}} = \hat{\mathbf{\Gamma}}_m + \hat{\mathbf{\Phi}}_m \left(\hat{\mathbf{\Gamma}}_{m-1} + \hat{\mathbf{\Phi}}_{m-1} \left(\hat{\mathbf{\Gamma}}_{m-2} + \hat{\mathbf{\Phi}}_{m-2} \left(\hat{\mathbf{\Gamma}}_{m-3} + \ldots \right) \right) \right) \tag{2.34}$$

The system output, y, is then expressed as (2.35). In most cases this is simply the output voltage and can be approximated by the output capacitor. If the dynamics of the capacitor ESR is desired the output voltage can be calculated as a function of $\hat{\mathbf{v}}$ and $\mathbf{u}$.

$$y = \mathbf{P}\,\hat{\mathbf{v}} + \mathbf{Q}\,\mathbf{u} \tag{2.35}$$

The DC gains of the system from inputs to outputs can be found by (2.36).

$$\boldsymbol{\alpha} = \mathbf{Q} + \mathbf{P}\left(\mathbf{I} - \mathbf{\Phi}\right)^{-1} \mathbf{\Gamma} \tag{2.36}$$

As an example, the 3:1 Ladder SCC, shown in Fig. 2.3, analyzed in Section 2.1.1 will be again considered here. The first step is to analyze the two phases using KCL and KVL to write a system of equations. From phase 1 the matrices $\mathbf{E}_1$, $\mathbf{F}_1$, and $\mathbf{G}_1$ are given in (2.36), (2.37), and (2.38) respectively.

$$\mathbf{E_1} = \begin{bmatrix} 0 & 1 & 1 & 0 \\ -R_{th} & R_{th} & R_{th} & -\left(r_{co} + R_{th}\right) \\ -\left(r_e + 2\,r_s\right) & 0 & r_s & r_{co} \\ r_s & 0 & -\left(2\,r_s + 2\,r_e\right) & 0 \end{bmatrix} \tag{2.37}$$

$$\mathbf{F_1} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 \\ -1 & 0 & 0 & 1 \\ 0 & 1 & -1 & 0 \end{bmatrix} \tag{2.38}$$

$$\mathbf{G_1} = \begin{bmatrix} 0 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{2.39}$$

From phase 1 the matrices $\mathbf{E}_2$, $\mathbf{F}_2$, and $\mathbf{G}_2$ are given in (2.40), (2.41), and (2.42) respectively. The switching capacitor ESR, output capacitor, switch on resistance, and Thévenin resistance will be represented by r_e, r_{co}, r_s, and R_{th} respectively.

$$\mathbf{E_2}=\begin{bmatrix} -1 & -1 & 1 & 0 \\ (r_s+r_e) & -(r_s+r_e) & 0 & 0 \\ 0 & (r_s+r_e) & (r_s+r_e) & r_{co} \\ R_{th} & R_{th} & 0 & -(r_{co}+R_{th}) \end{bmatrix} \tag{2.40}$$

$$\mathbf{F_2}=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \tag{2.41}$$

$$\mathbf{G_2}=\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -1 & 0 \\ 0 & 1 \end{bmatrix} \tag{2.42}$$

The **A** and **B** matrices can be calculated using (2.28) and (2.29) and converted to discrete-time utilizing MATLAB's c2d command. Finally the models are combined using (2.33) and (2.34). In this example the outputs **y** are just the capacitor voltages so **P** is defined as a 4x4 identity matrix.

As before, the switching capacitors $C_1=C_2=C_3=40\,\mu F$, the output capacitor $C_o=100\,\mu F$,the switching frequency is 250kHz, the resistances are r_e= 3mΩ, r_s= 10mΩ, r_{co}= 30mΩ, and R_{th}= 1Ω. A 1V input step is applied to a circuit model in LTSpice and to the model developed in MATLAB. The capacitor voltages are compared in Fig. 2.5(a-d) and show reasonable agreement between the SPICE simulation and the dynamic model.

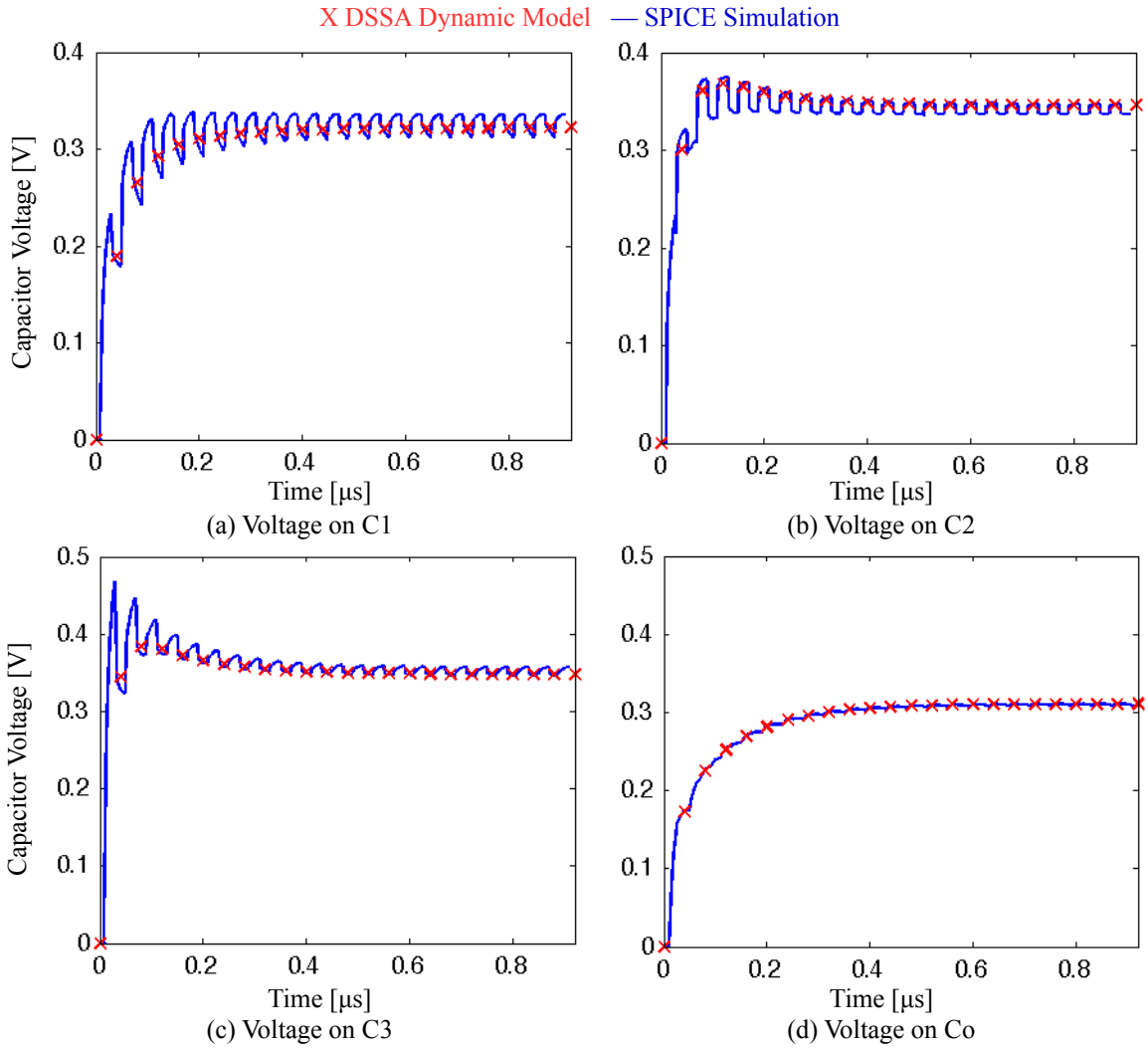


Fig. 2.5 Comparison of SPICE Simulated 3:1 Ladder SCC and the DSSA Dynamic Model.

B. Output Impedance Modeling

An important outcome of the DSSA approach used in [29] is that it captures the switching frequency dependency of the steady state equivalent output impedance. The common approach of state-space averaging in continuous time does not capture this dependency. In section 2.1.1, a simple method was described to approximate the output impedance in relation to the asymptotic slow switching limit (SSL) impedance and the fast switching limit (FSL) impedance, R_{SSL} and R_{FSL} respectively. From [33] DSSA dynamic model can approximate the output impedance as (2.43).

$$R_{eq} \approx Z_{out}|_{s=0} = \frac{\alpha_2 R_{th}}{1-\alpha_2} \tag{2.43}$$

where α_2 is the DC gain found by (2.36) from the input v_{th} to the output voltage.

By generating a dynamic model at various switching frequencies, a comparison of the modeled output impedances can be made between the DSSA dynamic model and the previously covered switching limit approach. The R_{FSL} used in this comparison is the modified impedance given in (2.18) that includes capacitor ESR. The results shown in Fig. 2.6, show the model generated by DSSA is in close agreement but does show an error in the both the SSL and the FSL. This discrepancy is due to the effect of the output stage (output capacitor and ESR) on the SCC dynamic model. While modeling the SCC output impedance with the SSL and FSL method the output voltage is assumed to be ideal (fixed and no resistance). If the DSSA dynamic model is generated with a much larger output capacitance and small ESR, C_o = 600µF and r_{co} = 1mΩ, the difference becomes negligible and the models are in good agreement as seen in Fig. 2.7.

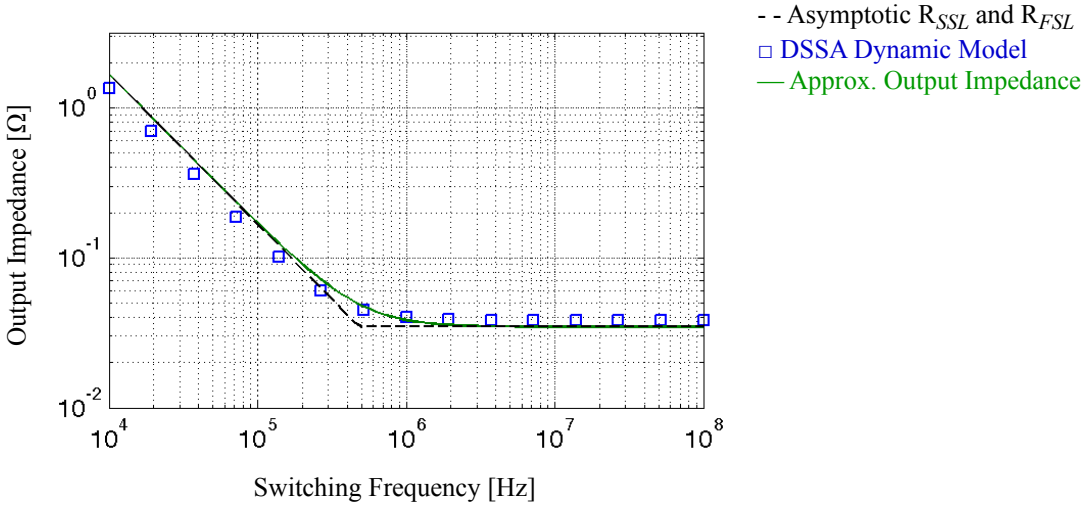


Fig. 2.6 Steady-state output impedance of the DSSA dynamic model and of the SSL/FSL model

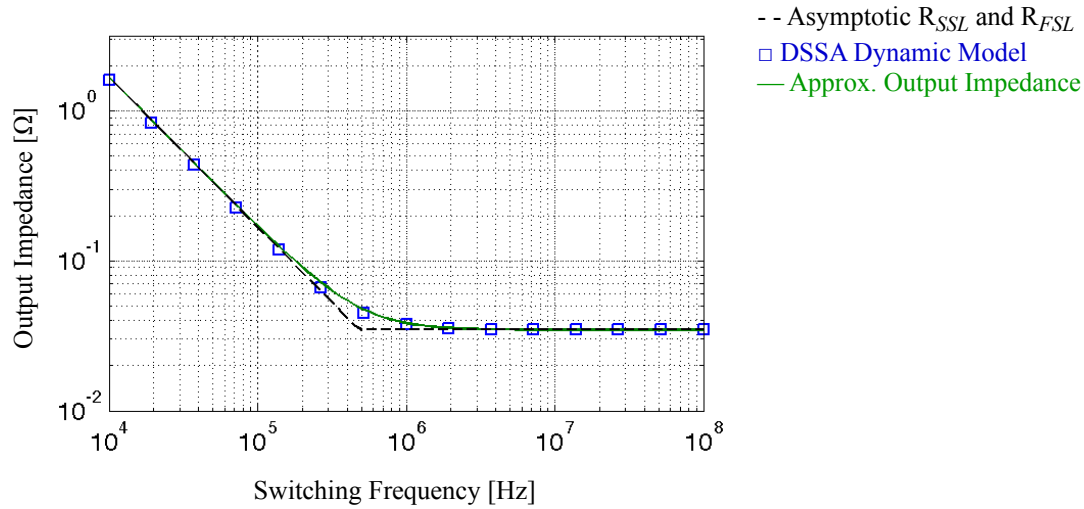


Fig. 2.7 Steady-state output impedance of the DSSA dynamic model and of the SSL/FSL method without an output capacitance ESR

C. Model Reduction

The model generated by (2.32), as shown in Fig. 2.5, captures all the internal dynamics of the SCC. In addition, the model will be a *n*-ordered model where *n* is the number of capacitors in the system including the output capacitor. In most cases the only dynamics of interest are those of the input and output stages. The SCC model only contains capacitors and resistors resulting in real eigenvalues of Φ. In general (2.32) yields a single dominant pole, λ, that dominates the dynamics. For most applications, a first order model can be generated from this higher order model given by (2.44).

$$y[k+1]=\lambda\, y[k]+(1-\lambda)\boldsymbol{\alpha}\,\mathbf{u}[k] \tag{2.44}$$

Again, $\boldsymbol{\alpha}$ represents the DC gains of the output from the inputs as found in (2.36). This simple model can easily be converted to continuous time via (2.45).

$$Y(s)=\left(\frac{a}{s+a}\right)\boldsymbol{\alpha}\boldsymbol{U}(s) \quad , \quad a=-\frac{\ln(\lambda)}{T} \tag{2.45}$$

The transfer function defined in (2.45) can be transformed to give the audio susceptibility and output impedance. Audio susceptibility is the small-signal input to output voltage transfer function and can be written as (2.46) for a model with output $y = v_o$ and the inputs $\mathbf{u} = [v_{in}\ v_{th}]^T$. The output impedance, for the same example system, is written as (2.47).

$$\frac{\tilde{v}_o}{\tilde{v}_{in}}=\frac{\alpha_1 a}{s+a} \tag{2.46}$$

$$Z_{out}=\frac{\alpha_2 a R_{th}}{s+(1-\alpha_2)a} \tag{2.47}$$

2.1.3 Switching Losses

Switching losses in the SCC are made up of gate charge losses, MOSFET output capacitance losses, and turn on losses. In most SCC current goes to zero right after a switch turns off unless there is significant parasitic inductance. With proper design of the printed circuit board (PCB), the parasitic inductance is on the order of a few nano-Henries and provide negligible loss [36].

The gate charge loss is due to charging and discharging of the MOSFET input capacitance by the gate driver. For a drive voltage of V_{DD}, total gate charge Q_g, and switching frequency f_{sw} the gate charge loss is calculated by (2.48).

$$P_g=V_{DD}Q_g f_{sw} \tag{2.48}$$

There is also an output capacitance with stored energy associated with each MOSFET that is abruptly discharged when the MOSFET turns on. For each switching period, the switch output capacitance C_{oss} is charged and discharged to the blocking voltage of the MOSFET $V_{DS\text{-}off}$ resulting in lost power calculated as (2.49).

$$P_g = \frac{1}{2} V_{DS-off} C_{oss} f_{sw} \tag{2.49}$$

The last switching loss considered is the turn on loss caused by the overlap of the falling switch voltage V_{DS} and the rising switch current. The switch voltage falls from $V_{DS\text{-}off}$ to approximately zero while the current rises from zero to a peak value $I_{DS\text{-}pk}$ during the turn on transition occurring in time t_{on}. For a SCC the switch load is resistive so the turn on loss can be approximated by (2.50) assuming linear voltage and current waveforms during the turn on period.

$$P_{on} = \frac{t_{on}}{6} V_{DS-off} I_{DS-pk} f_{sw} \tag{2.50}$$

2.2 Switched-Capacitor Converter Regulation Strategies

The poor or almost absent line and load regulation of SCC has been a major reason preventing the acceptance of SCC for various power converter applications. There are various approaches to provide regulation for the SCC [21-24][37-39]. One method is to control the switching frequency to vary the output impedance allowing for a small range of load regulation, though this approach does not solve line regulation issues. A second method is to dynamically alter the topology using different switching patterns to achieve multiple discrete conversion ratios. By monitoring the input and output voltages the closest achievable conversion ratio is chosen and switching pattern implemented. Other methods use duty cycle variation and adaptive on-times have also been researched as options for regulation.

Other approaches added magnetics to provide regulation. One approach is to utilize a second inductor based converter in a cascaded configuration to provide regulation. Another approach is to put an inductor at the end of suitable SCC and with the proper control strategy, regulation can be achieved. These approaches utilize the high conversion ratios offered by SCC but reintroduce magnetics to provide regulation. The magnetics used in a cascaded regulating converter will have to be rated for the power rating of the SCC making them undesirable for regulation of higher power SCC.

2.2.1 Regulation Through Switching Frequency

As covered in section 2.1, the SCC in steady state can be though of as a DC transformer with an output impedance. This output impedance is switching frequency dependent and has a minimum as the SCC nears the fast switching limit (FSL). In the slow switching limit (SSL) the output impedance varies inversely proportional to the switching frequency as shown in Fig. 2.8. By manipulating the output impedance through the switching frequency, voltage regulation can be achieved below the nominal output voltage. The impedance is varied to create the necessary voltage drop for the desired voltage. Regulation is provided by increasing or decreasing the losses of the SCC as appropriate.

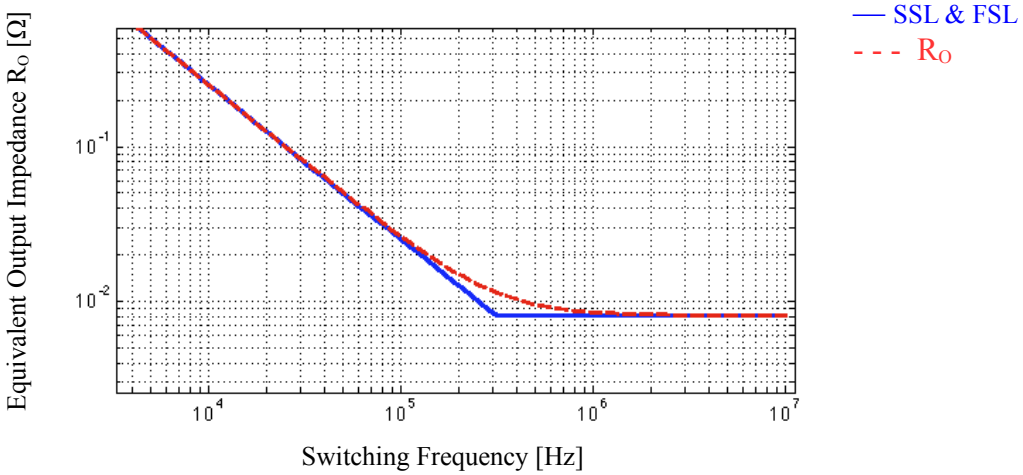


Fig. 2.8 Equivalent output impedance showing the SSL and FSL asymptotic limits

This can be thought as a SCC followed by an LDO in series. It is practical and relatively efficient for low voltage drops. Regulation can be provided for a large range of load current through variation of the switching frequency. The maximum theoretical efficiency is dependent on the SCC conversion ratio *n*, the input voltage, and the output voltage given by (2.51). For a desired regulated voltage of 1V and SCC with a conversion ratio of 2:1 (n=2) the input voltage must be larger than 2V. For a input voltage of 2.2V the SCC can be regulated for large load transients at roughly 91% efficiency. This approach quickly becomes inefficient and ineffective in the face of large input voltage variation or output voltage variation due to increased loads. While this regulation strategy may be an effective choice for low power, for applications at higher powers, like an LDO, it is a poor choice as losses become excessive. Further the heat generated by the losses in the converter become problematic.

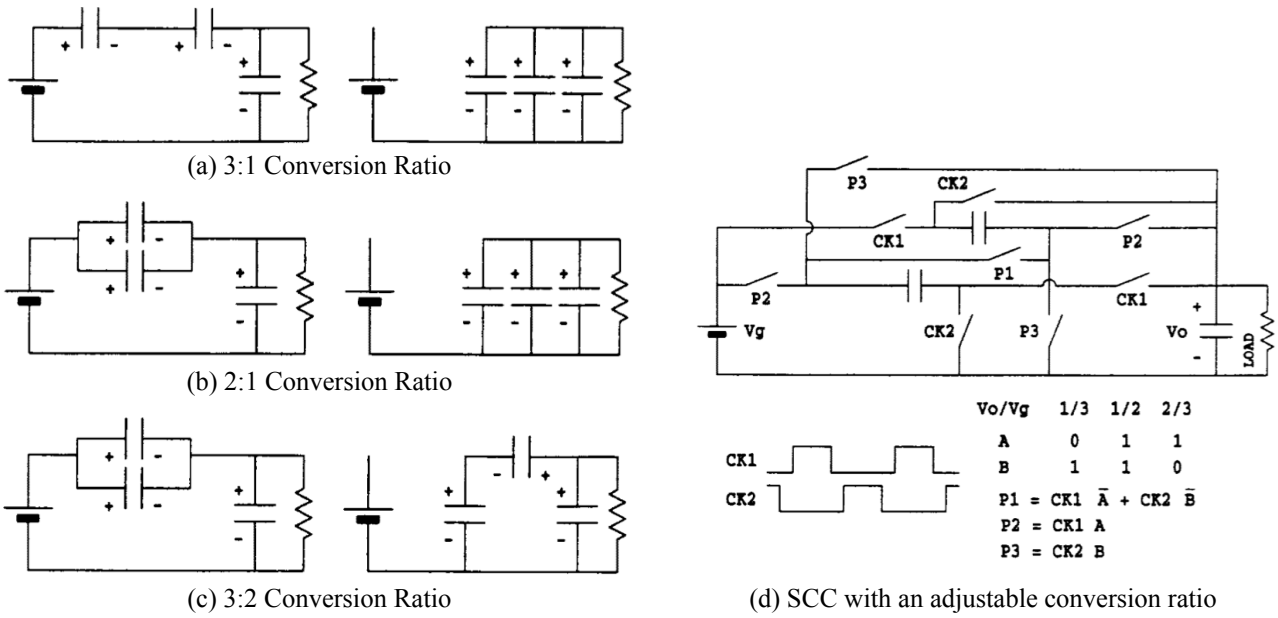
$$\eta_{SCC}=\frac{nV_o}{V_{in}} \tag{2.51}$$

This method of regulation can be implemented with a linear feedback from the output voltage. Output current feedforward can also be added for better transient response. Using linear feedback may not be the most desirable since the system is non-linear due to the frequency dependence of the transient response. If a larger ripple voltage is acceptable a hysteresis feedback (bang-bang control) can be implemented. Hysteresis feedback is effective, stable, and a simple means of control for switching frequency based regulation [28].

2.2.2 Adjustable Conversion Ratios

In the face of large input voltage variation, switching frequency regulation becomes inefficient and impractical as seen in (2.51). One solution is to modify the SCC topology to enable it to achieve multiple conversion ratios. Then as the input voltage increases the conversion ratio that results in highest efficiency can be selected and the desired switching pattern implemented. This can be done with a complex set of switching patterns [21] or by implementing different input or output taps to the topology [28]. This method can be combined with switching frequency regulation to provide tighter output voltage control and excellent load regulation. Further as the conversion ratio is being altered, through a new switching pattern or different tap, the output voltage will see a large transient due to the change. Utilizing frequency modulation can help provide a fluid conversion ratio transition as in [22].

An example of utilizing different switching patterns is taken from [21]. In [21] a method to solve for the set of realizable conversion ratios for a given number of capacitors is covered. If there are 2 capacitors then 2:1, 1, and 1:2 are possible conversion ratios. For 4 capacitors there are 19 realizable ratios: 5:1, 4:1, 3:1, 5:2, 2:1, 5:3, 3:2, 4:3, 5:4, 1:1, 4:5, 3:4, 2:3, 3:5, 1:2, 2:5, 1:3, 1:4, and 1:5. By identifying the different topologies needed for a set of desired ratios, the circuits can be combined to create a single SCC. This single SCC, with the right switching patterns, achieve the desired ratios. In [21] an example is given for a 3 capacitor SCC that desires the ratios 3:1, 2:1, and 3:2. The switched circuits are given in Fig. 2.9. They are then combined to create a SCC with an adjustable conversion ratio.



(a) 3:1 Conversion Ratio

(b) 2:1 Conversion Ratio

(c) 3:2 Conversion Ratio

(d) SCC with an adjustable conversion ratio

Fig. 2.9. Switched-capacitor converter sub circuits for conversion ratios of (a) 3:1, (b) 2:1, and (c) 3:2 can be combined and realized by the (d) switched-capacitor converter with an adjustable conversion ratio. Diagrams from [21].

Achieving multiple conversion ratios in such a manner generally requires more switches, complex topologies, and complex switching patterns and control. The other approach slightly modifies the SCC by adding numerous input or output access points, or taps, to the topology. An example from [28] is a 4:1 Ladder SCC also has a 3:1 and a 2:1 Ladder SCC within it. By adding input taps as in Fig. 2.10 the 4:1 Ladder SCC can also achieve 3:1 and 2:1 operation with little added complexity or switches.

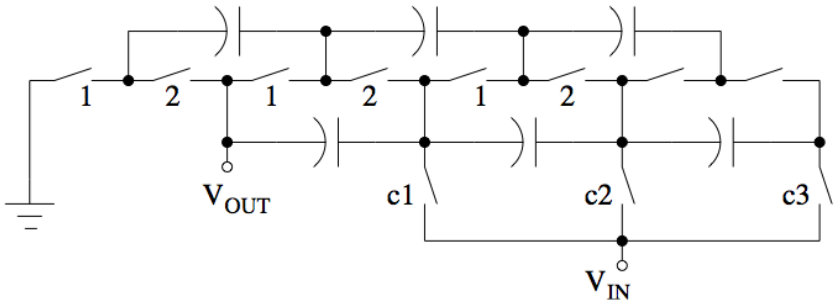


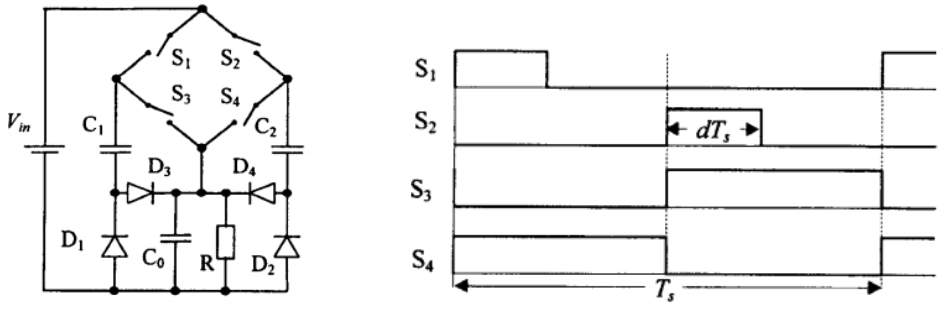
Fig. 2.10. Step down ladder with different taps for the input voltage allowing multiple integer conversion ratios to be achieved. Figure taken from [28].

By providing multiple conversion ratios in a single SCC regulation can be implemented for variations in input voltage to some degree. This works well for applications that do not require strict output voltage regulation. Adjustable conversion ratios can be combined with switching frequency modulation to provide tighter output regulation.

2.2.3 Regulation Through Duty Cycle

Another approach for regulation is to control the duty cycle or the on time of a SCC phase. Such regulation techniques have been employed in [38,39] but they lead to increased losses as it moves the output voltage away from the ideal conversion ratio (i.e. ideal output voltage). In some cases, such as low power, the power density of SCC may outweigh the efficiency lost due to regulating the SCC. These strategies are not suitable for high power applications or where efficiency is top priority such as battery powered consumer devices like smartphones.

Results in [38] demonstrated that line and load regulation can be provided (in SCC) using the duty cycle as a control variable. The control strategy is implemented on a simple two phase SCC with four active switches shown in Fig. 2.11(a). The timing waveforms for the switches depicted in Fig. 2.11(b) and show there will be four different states, two in each phase.



(a) (b)Switch Gate Waveforms

Fig. 2.11. The (a) 2:1 step down SCC and the (b) corresponding gate signals for switch operation. Images taken from [38].

State-space averaging (SSA) techniques are employed to find the steady-state output voltage function (2.52) where r_c is the capacitor ESR, r_1 is the on-resistance of switches S_1 and S_2, r_2 is the on-resistance of switches S_3 and S_4, and V_d is the forward voltage drop of the diodes. Inspection of (2.52) shows that the output voltage can be regulated through the duty cycle variable *d* by varying the effective resistances seen in the equation. In addition, there is a limit to the regulation ability of the control variable *d* as illustrated in .

$$V_o = \frac{V_{in} - 2V_d}{2 + \frac{1}{R}\left(\frac{r_c + r_2}{2} + \frac{r_c + r_1}{4d}\right)} \tag{2.52}$$

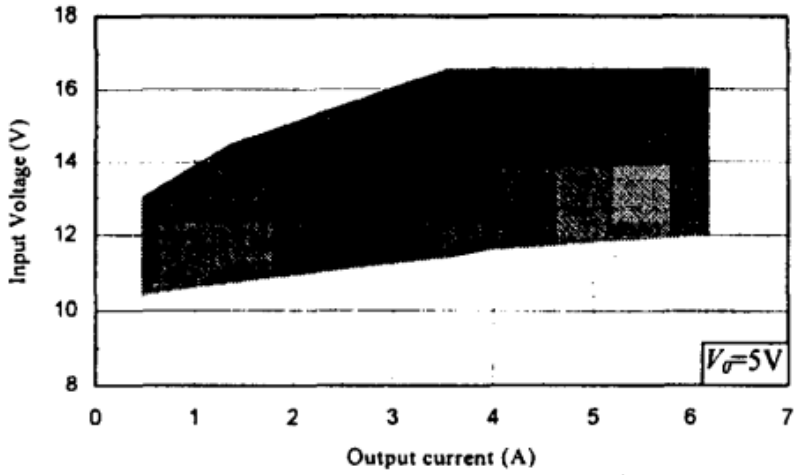


Fig. 2.12. Regulation limits of the SCC from [38]

The SCC in [38] is designed for a 12V input and 5V output with a maximum load of 7A. The experimental results confirmed regulation within the limited capabilities of the regulation strategy. The efficiency of the converter is limited to the theoretical maximum efficiency given by (2.53).

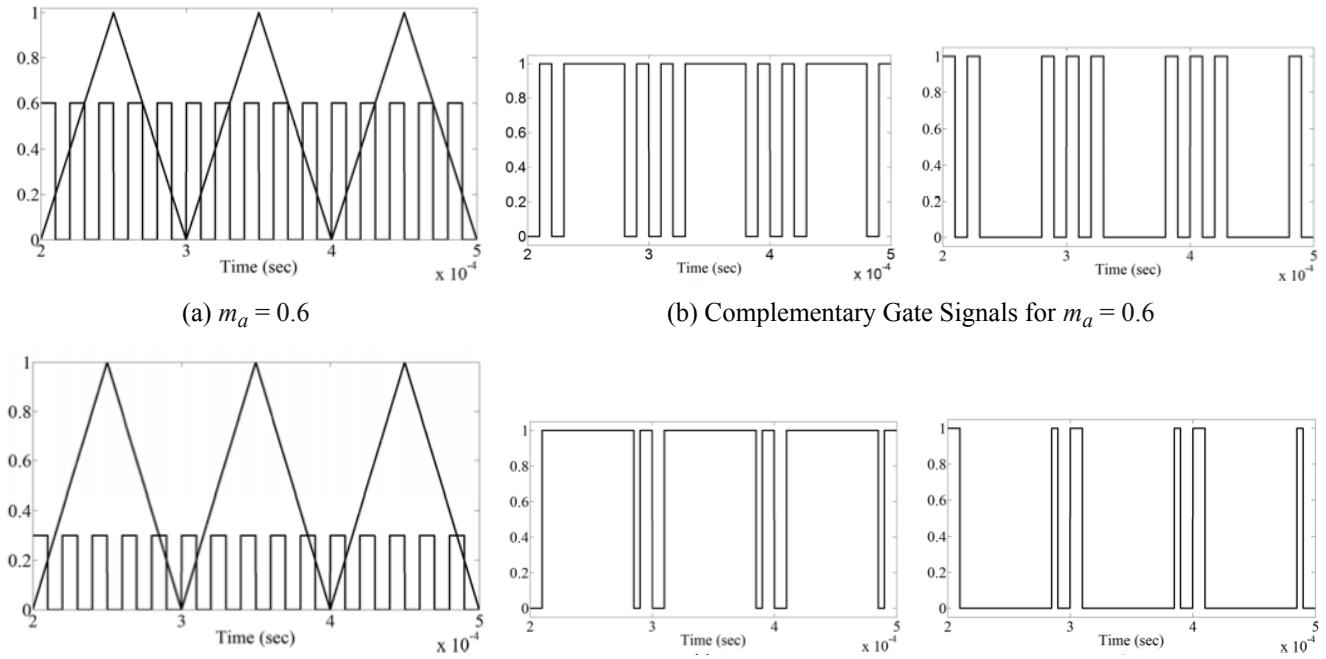
$$\eta_{SCC}=\frac{nV_o}{V_{in}}=\frac{2(5)}{12}=83.3\% \tag{2.53}$$

2.2.4 Pulse Dropping Technique

Another method to regulate a SCC is the pulse dropping technique (PDT) utilized in [22]. This technique's effect on the SCC is similar to switching frequency regulation in that it changes the effective output resistance of the SCC. The gate signals for PDT are generated by comparing a square wave signal to a triangular wave and generating a pair of opposing gate signals. One gate signal is generated when the triangular wave is larger than the square wave signal and while the other when the square wave signal is larger. Control for PDT is implemented with two modulation indexes: amplitude modulation (m_a) and frequency modulation (m_f) defined in (2.54) and (2.55) respectively. Using the amplitude modulation index m_a different gate signals can be generated as shown in Fig. 2.13.

$$m_a=\frac{\hat{v}_{sqr}}{\hat{v}_{tri}} \tag{2.54}$$

$$m_f=\frac{f_{sqr}}{f_{tri}} \tag{2.55}$$



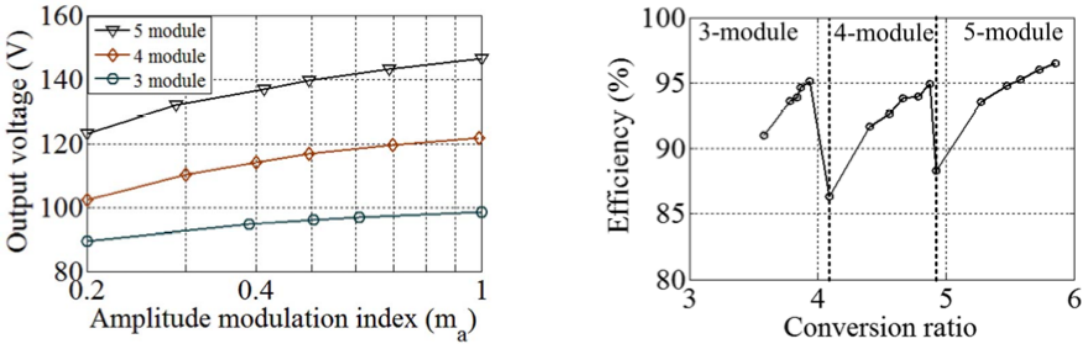
(a) $m_a = 0.6$ (b) Complementary Gate Signals for $m_a = 0.6$

(c) $m_a = 0.3$ (d) Complementary Gate Signals for $m_a = 0.3$

Fig. 2.13. PDT can vary m_a to generate different gate signals and vary the equivalent output impedance of the SCC. Diagrams taken from [22].

Like switching frequency regulation, PDT varies the output impedance but does so by varying the modulation indexes m_a and m_f. Again regulating the converter in this fashion simply varies the power dissipation within the SCC to provide a constant output voltage. A lower amplitude modulation index not only increases losses but causes larger output voltage ripples.

An advantage shown in [22] is that the SCC can also change its conversion ratio allowing for a larger range of regulation for either the input voltage or the output voltage. In [22] the results shown in Fig. 2.14(a) that different output voltages can be achieved with a constant input voltage and load meeting the goal of a continuous conversion ratio. The experimental results shown in Fig. 2.14(b) shows the efficiency fluctuates across the conversion ratio but remains above 85%. This demonstrates the benefits of having a SCC that can change its conversion ratio in order to remain close to the ideal conversion ratios set by the topology.



(a) (b)

Fig. 2.14. Through PDT (a) a continuous conversion ratio is achieved. Due to the ability to change the topology dynamically and thus the ideal conversion ratio (b) efficiencies are kept above 85% [22].

2.2.5 Cascaded Or Merged Topologies for Regulation

With the previous methods regulation required operating the SCC at a non-ideal conversion ratio leading to decreased efficiencies. For low power applications this can be acceptable considering the benefits of high power density and larger conversion ratios achievable by SCC. Others approaches have utilized SCC "cells" to be merged with common topologies such as buck, boost, buck-boost, Ćuk, and SEPIC converters to achieve higher conversion ratios [40],[41]. These hybrid converters focus more on augmenting the original converter and increasing the conversion ratio and minimizing switch stresses. In work such as [24] and [42] the SCC is used for its high efficiency, power density, and conversion ratio and then regulated with a second converter in a cascade configuration. The work in [24] also pursued SCC as it lends itself well for integrated power chips.

By cascading a second converter, such as a buck or boost converter, the SCC can be operated unregulated, at its ideal conversion ratio and highest efficiency, while the cascaded converter provides regulation. This approach also decreases the voltages and input voltage range seen by the second converter which can minimize that converter's component stresses and losses. The drawback to this approach is both converters must be rated for the full power requirements and the combined efficiency of the two converter efficiencies is (2.56).

$$e_{cascaded} = e_{SCC}\, e_{PWM} \tag{2.56}$$

An unregulated SCC can provide a high conversion ratio, high efficiency, and high power density while providing a lower unregulated voltage for the second regulatory magnetic converter. The second converter can then utilize fast, low voltage devices allowing for higher switching frequencies. Operating at high frequencies allows for smaller passive components which is vital with the

introduction of a magnetic device.

This cascaded regulation approach can be used with a SCC that can dynamically change its conversion ratio. Utilizing a SCC that achieves multiple conversion ratios allows for the second regulation stage to see a low and narrow range of voltages even with a large input voltage to the system.

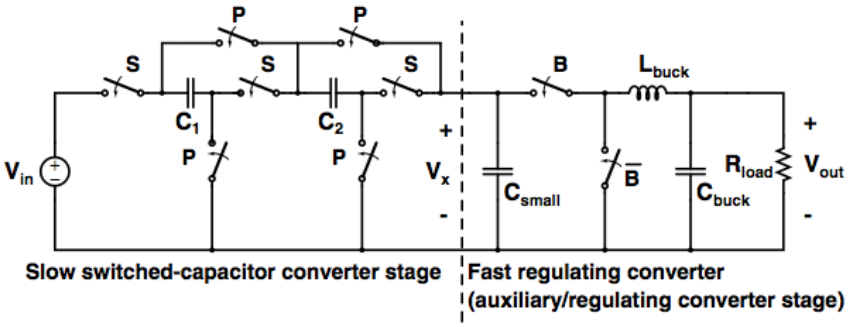


Fig. 2.15. The SCC transformation stage coupled with a fast regulating buck converter from [24]

The work in [24] built a prototype of the cascaded converters shown in Fig. 2.15 and utilizes the second converter to provide soft charging of the SCC. Typically as SCC capacitors are charged they experience a large current that exponentially decreases on top of a steady state current. This is referred to as hard charging and generally leads to larger capacitive losses than resistive losses. Alternatively, when there is a voltage source, such as a secondary converter, that produces the difference between the charging voltage and the capacitor voltage the charging current can be reduced. This is referred to as soft charging in [24]. This soft charging approach can produce efficiency gains for the SCC or for reduction in the switching capacitances and the capacitor labeled C_{small}. The purpose of [24] was not to create a high efficiency converter but to prove the benefits of soft charging. The output voltage of the SCC with soft charging is shown in Fig. 2.16 along with the regulated output voltage from the second converter.

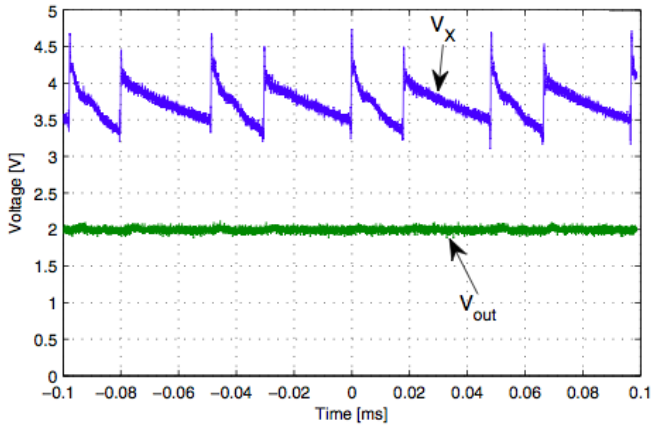


Fig. 2.16. The soft charging SCC provides an output voltage V_x that the second converter regulates to V_{out}. Image taken from [24].

With this approach the cascaded converter attains peak efficiencies of about 85% as seen in Fig. 2.17. The SCC is estimated in [24] to be 90% efficient. The work in [24] noted that they did not design the converter for efficiency but to demonstrate the soft charging concept and use it to reduce the needed switching capacitance. The work in [42] did aim for efficiency and achieved a SCC that maintained efficiencies above 97% with an overall peak efficiency of 89% for the cascaded converters. Thus even with highly efficient converters the overall efficiency of the cascaded approach is limited. The regulating converter benefits from smaller voltage requirements and higher switching frequencies allowing for size reduction, but it must still have the same full power rating as the SCC.

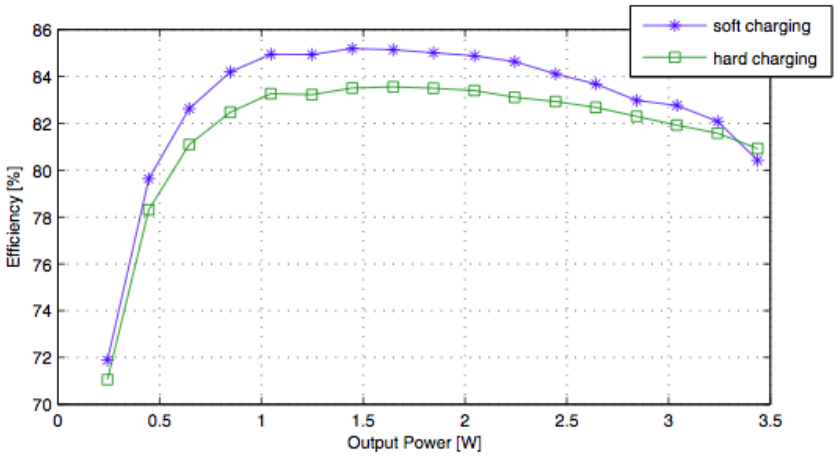


Fig. 2.17. Efficiency of the cascaded SCC and regulating buck converter from[24].

Chapter 3 Proposed Quasi-Parallel Regulated Switched-Capacitor Converter

The proposed Quasi-Parallel Regulated Switched-Capacitor Converter (QPRSCC) utilizes an unregulated switched capacitor converter and a partial power inductor based pulse width modulated (PWM) converter in an input series and output parallel configuration as shown in Fig. 3.1.

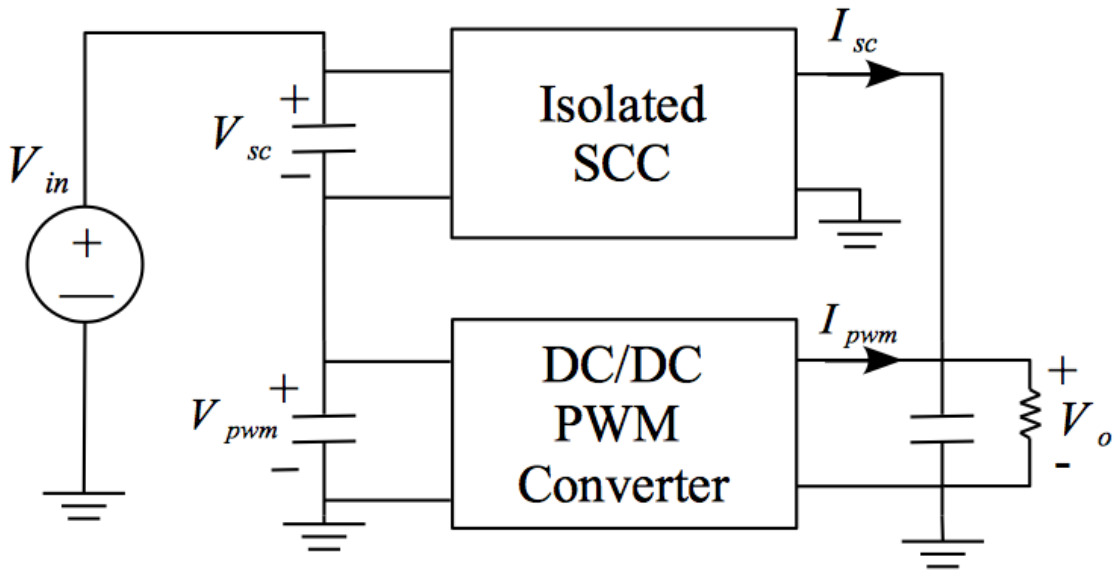


Fig. 3.1. Proposed quasi-parallel regulated switched-capacitor converter showing an unregulated SCC with a partial-power PWM converter providing regulation.

The QPRSCC utilizes a PWM DC-DC converter in an input-series output-parallel (ISOP) configuration allowing for line and load regulation of the SCC. This regulating PWM converter is a partial power converter, only converting a portion of the QPRSCC total power. This enables decreased converter size and cost, but most importantly it decreases the necessary size of the magnetics introduced. Due to the ISOP configuration the overall efficiency of the topology is additive of the two individual converter efficiencies, offering better efficiency than cascaded topologies whose efficiency is the multiple of the individual converters' efficiencies. The QPRSCC also boasts higher overall efficiencies than the partial power series regulated converters [43].

Depending on the input voltage range and the required output voltage, the PWM converter can be implemented with common buck, boost, or buck-boost topologies. The PWM Converter provides load and line regulation for the QPRSCC while only converting a portion of the total converted power. The

SCC is operated unregulated handling the majority of the converted power. This allows for all the benefits of an unregulated SCC such as high conversion ratio and high efficiencies. Unlike cascaded designs [24] and merged switched-capacitor buck/boost topologies [45-47] the PWM converter is partial power allowing for significant size reduction of the magnetics and the overall converter size.

This configuration satisfies the requirements to be considered quasi-parallel in [48], due to the SCC operating unregulated with a regulating PWM converter. The quasi-parallel configuration, also called the Sigma architecture [49], provides an inherent feedback path through the power stage and offers excellent transient properties. It is also inherently stable, unlike ISOP configurations that utilize multiple regulating converters. Multiple regulated converters in ISOP configurations must have their input voltages actively balanced due to the input impedance of a regulated converter appearing negative. With the unregulated SCC acting like a transformer a natural stability is attained. For instance if the regulating PWM converter pulls more current to increase the output voltage, the input voltage on the PWM will drop as it's input capacitor is discharged. As the PWM converter input voltage drops the SCC input voltage increases which will lead to a higher output voltage since the SCC is unregulated. With this increase of the output voltage the regulating PWM will require less input current and it's input voltage will either decrease at a slower rate or stabilize.

In section 3.1 the QPRSCC will be analyzed in an ideal steady state condition to show the partial power property and develop the efficiency equation given the efficiency of the SCC and the regulating PWM converter. The improved transient response of the quasi-parallel configuration will also be outline in the overview of the QPRSCC. Using a telecom application, the topologies for the SCC and the PWM converter will be selected for the QPRSCC. The selected topologies, the isolated multilevel modular switched-capacitor converter (MMSCC) and the DC-DC H-bridge converter, will be described and formally designed in sections 3.2 and 3.3 respectively.

3.1 Quasi-parallel Regulated Switched-Capacitor Converter Overview

3.1.1 Partial Power Property and Efficiency of the QPRSCC

The QPRSCC provides regulation of a SCC utilizing a inductor based PWM controlled converter in an ISOP configuration. With this configuration the PWM converter handles some portion of the total converted power. Regulation strategies, utilizing a merged or cascaded inductor-based PWM converter, required this PWM controlled converter to be sized for the total SCC power rating increasing total size,

total cost, and magnetic size. The partial power property of the QPRSCC allows for a smaller sized and lower cost inductor based PWM converter to provide regulation.

Partial power processing is one of the major benefits of this configuration. A second major benefit is the increased overall efficiency of the QPRSCC when compared to cascaded or series regulated converters. Both of these properties can be illustrated by a top level steady-state analysis of the QPRSCC.

The efficiency and partial power property of the QPRSCC can be defined in terms of the input voltage V_{in}, the output current I_o, the SCC efficiency e_{sc}, the PWM efficiency e_{pwm}, the SCC input voltage V_{SC}, the PWM input voltage V_{PWM}, the SCC output current I_{SC}, and the PWM output current I_{PWM}. The output power is related to the input power by its efficiency as in (3.1). The output power can be written as the sum of the two converters output power (3.2), which are defined as (3.3) and (3.4) for the SCC and PWM converter respectively.

$$P_{out} = e_{QPRSC} P_{in} = e_{QPRSC} V_{in} I_{in} \tag{3.1}$$

$$P_{out} = V_o \left(I_{SC} + I_{PWM} \right) = P_{SC} + P_{PWM} \tag{3.2}$$

$$P_{SC} = e_{SC} V_{SC} I_{in} \tag{3.3}$$

$$P_{PWM} = e_{PWM} V_{PWM} I_{in} \tag{3.4}$$

The power processed by each converter is dependent on the input voltage of the converter shown in (3.3) and (3.4) . If it assumed that each converter is ideal (100% efficiency) then the percentage of the total power processed in each converter can be written as (3.5) and (3.6). From these equations it is immediately evident that the power processed is entirely dependent on the ratio of the converter's input voltage to the total input voltage of the QPRSCC. The PWM converter power rating is then dependent on the input voltage range of the application of the QPRSCC, as given by:

$$\frac{P_{SC}}{P_{QRPSC}} = \frac{V_{SC} I_{in}}{V_{in} I_{in}} = \frac{V_{SC}}{V_{in}} \tag{3.5}$$

$$\frac{P_{PWM}}{P_{QRPSC}} = \frac{V_{PWM} I_{in}}{V_{in} I_{in}} = \frac{V_{PWM}}{V_{in}} \tag{3.6}$$

To find the efficiency of the QPRSCC in terms of each converter's efficiency the output power of each converter, given in (3.3) and (3.4), is substituted into (3.2). This gives (3.7) which can be solved for the QPRSCC efficiency e_{QPRSC} (3.9).

$$P_{out} = \left(e_{PWM} V_{PWM} + e_{SC} V_{SC} \right) I_{in} \tag{3.7}$$

$$e_{QPRSC} V_{in} I_{in} = \left(e_{PWM} V_{PWM} + e_{SC} V_{SC}\right) I_{in} \tag{3.8}$$

$$e_{QPRSC} = e_{PWM} \frac{V_{PWM}}{V_{in}} + e_{SC} \frac{V_{SC}}{V_{in}} \tag{3.9}$$

The QPRSCC efficiency is a weighted average of the individual converter efficiencies, dependent on the ratio of the converter's input voltages to the total input voltage of the QPRSCC. This offers higher possible efficiencies than cascaded converters where the power is processed twice, once by the SCC and once by the regulating PWM converter, and the efficiency is given by (3.10). There may be applications that the cascaded regulated SCC can achieve a higher efficiency, the proper choice is highly dependent on the efficiency of the SCC. Further discussion into this matter is beyond the scope of the thesis.

$$e_{cascaded} = e_{SCC} e_{PWM} \tag{3.10}$$

The QPRSCC efficiency, in some cases, can be better than in series regulated converters which utilizes the partial power concept as well. If a series regulated SCC configuration (SRSCC) is employed the SCC would have a power rating for the full power and handle all power processing. The series regulating partial power PWM converter would then process a portion of that power to provide regulation. If the regulated output voltage V_o is always higher than the output voltage of the unregulated SCC which can be expressed as V_{in}/n where n is the SCC conversion ratio (n:1), then the efficiency of the SRSCC is given by (3.11). This is certainly better than a cascaded approach for regulation but the max efficiency is still limited by the efficiency of the SCC. In comparison with the efficiency of the QPRSCC, (3.9) can be expressed similarly as (3.12). From inspection it can be seen that the QPRSCC will obtain a higher efficiency compared to the series regulated switched-capacitor converter.

$$e_{SRSC} = e_{sc}\left(\frac{nV_o}{V_{in}} + e_{pwm}\left(\frac{V_{in} - nV_o}{V_{in}}\right)\right) = e_{sc}\frac{nV_o}{V_{in}} + e_{sc} e_{pwm}\left(\frac{V_{in} - nV_o}{V_{in}}\right) \tag{3.11}$$

$$e_{QPRSC} = e_{sc}\frac{nV_o}{V_{in}} + e_{pwm}\left(\frac{V_{in} - nV_o}{V_{in}}\right) \tag{3.12}$$

Hence the QPRSCC utilizes partial-power processing to provide an overall higher efficiency when compared to the other two converter regulation strategies. The partial power property allows the regulating PWM converter to be smaller in size and lower cost proportionally to its power rating. For a given application, it becomes necessary to know what power rating the PWM converter will need.

Depending on the application, the input voltage to the QPRSCC can vary greatly. The voltage seen on the PWM converter will vary linearly with the input voltage. The unregulated SCC will act like a DC-DC transformer in steady state; the input voltage will aways be equal to the output voltage times *n* as in (3.13).

$$V_{SC} = nV_o \tag{3.13}$$

Thus the ratio of the power processed by the PWM to the total power can be written in terms of the input voltage, output voltage, and SCC conversion ratio *n* giving (3.14).

$$p_{PWM} = \frac{V_{in} - nV_o}{V_{in}} = \left(1 - \frac{nV_o}{V_{in}}\right) \tag{3.14}$$

3.1.2 Benefits of Quasi-parallel Configuration

The quasi-parallel configuration allows for high overall efficiency. In most cases unregulated converters achieve higher efficiencies, and in particular, unregulated SCC can achieve high efficiencies [5,11,22]. With the unregulated SCC converting a majority of the power, the overall efficiency of the QPRSCC will be dependent on the SCC efficiency. The QPRSCC will enable regulation while providing high efficiencies [48,49].

The quasi-parallel configuration has two feedback paths. The first is the usual feedback due to closed-loop control. The regulated PWM DC/DC converter will alter it's duty cycle to maintain tight regulation of the output voltage. The second feedback path is inherent to the quasi-parallel structure, where the configuration is repeated here in Fig. 3.2 for reference to the following thought experiment.

Consider a increase in load causing a droop in the output voltage. The decrease in output voltage will decrease the voltage seen at the SCC input, V_{sc}. This will lead to an increase in the voltage at the PWM converter allowing for more power to flow through the regulating PWM converter to raise the output voltage [48,49].

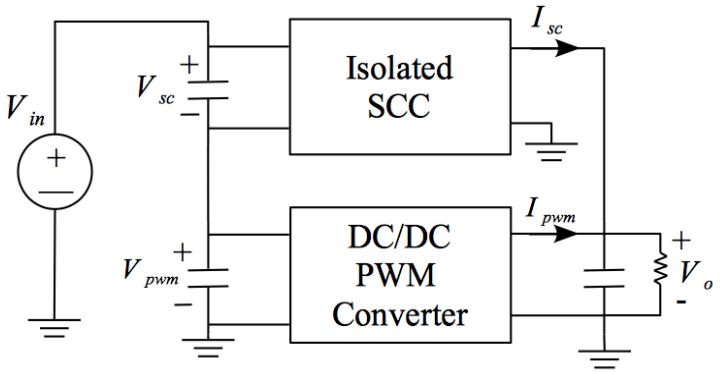
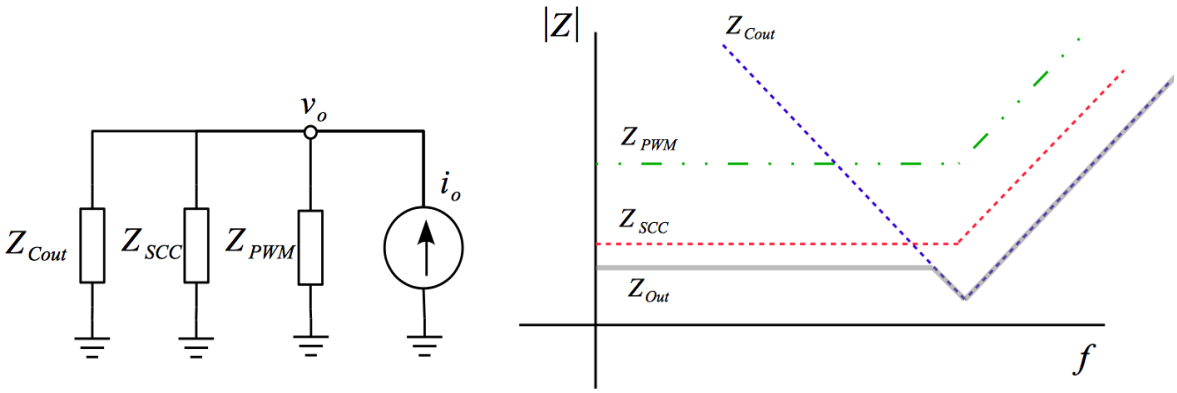


Fig. 3.2. Proposed quasi-parallel regulated switched-capacitor converter showing an unregulated SCC with a partial-power PWM converter providing regulation.

The quasi-parallel configuration also provides excellent load transient response. Unregulated converters provide low output impedance which provides the quasi-parallel configuration with a fast current slew rate [48]. An unregulated SCC operating near or in the FSL will provide very low output impedances that will be proportional to the total resistance due to switches, parasitics, and capacitor ESR. The output impedance of the QPRSCC can be represented as Fig. 3.3(a) and the approximate frequency response in Fig. 3.3(b). The low output impedance of the SCC will give the QPRSCC a low output impedance improving the current slew rate and load transient response. Further the lower output impedance of the SCC indicates it will provide the majority of the current during an increase in load to the QPRSCC.



(a) Equivalent Output Impedance Circuit (b) Approximate QRPSC Output Impedance Frequency Response

Fig. 3.3. Approximated QPRSCC output impedance indicating excellent load transient response

3.1.3 Topology Selection for Telecom Application

The proposed Quasi-Parallel Regulated Switch Capacitor Converter is a general solution and can be applied to any switched capacitor converter. The application requirements will dictate which SCC are

suitable and from the appropriate subset of SCC, a specific topology can be selected based on the restricting requirements such as efficiency, number of components, gate drive simplicity, or overall component volume. Other variables such as the input voltage range and the maximum power capacity of the regulating PWM converter will also limit the choice of SCC for the QPRSCC design.

Due to the high efficiency and large conversion ratios attainable by a SCC, a telecommunication's power supply is an excellent application of the QRPSC. In most datacenters 48V (36V to 72V range) is applied to server racks, each rack will then have DC/DC converters to step down the 48V to 12V. Common sizes, in inches, for these DC/DC converters are full brick 4.6″x2.4″x0.5″, half brick 2.3″x2.4″x0.35″, and quarter brick 2.3″x1.45″x0.35″. Power ratings range from 50-720W for these sizes [12], with 720W attained in half bricks [13], 180W in an eighth brick [14]. Future telecom power supplies will need have high power density (180W/in^3), high reliability, and fast transient responses [15-17].

The QPRSCC can provide high efficiency, the SCC can provide high power densities and if designed with ceramic capacitors improve reliability over electrolytic designs. The QPRSCC can also provide excellent transient response. The QPRSCC prototype design requirements and goals are as follows:

- Input Voltage: 48V Nominal (36V to 72V)
- Output Voltage: 12V ± 10%
- Power Rating > 120W (10A @ 12V)
- At Most Half Brick Size

With a wide input voltage range, the regulating PWM power rating will vary significantly for a SCC with a single conversion ratio. In the following (subsection A), the PWM power rating will be determined in terms of the conversion ratio n of the SCC. The result will be the needed to select a SCC that achieves a few discrete conversion ratios while remaining unregulated leading to the selection of a SCC topology in subsection B. Lastly, analysis of the input voltage seen by the regulating PWM converter will dictate what topologies will be selected for the PWM converter in subsection C.

A. PWM Power Rating Limit and SCC Conversion Ratio Selection

The power processed by the PWM converter is given by (3.15) where n is the SCC conversion ratio, V_o is the QPRSCC output voltage, and V_{in} is the QPRSCC input voltage. The choice of the conversion

ratio of the SCC is then determined by the input voltage range and/or the maximum power rating desired of the PWM converter.

$$p_{PWM} = \frac{V_{in} - n V_o}{V_{in}} = \left(1 - \frac{n V_o}{V_{in}}\right) \tag{3.15}$$

If it is assumed that the SCC conversion ratio n is static, then as input voltage increases, the power converted by the PWM regulating converter will increase as well. If the input voltage range is large enough, the power rating of the PWM converter may become undesirably high. For a Telecom power supply application, the output voltage is 12V and the input voltage range is from 36V to 72V. With a single conversion ratio, the SCC conversion ratio is selected at the minimum input voltage required to keep a reasonable voltage (at least 4V) on the PWM converter over the input voltage range. Thus the largest integer conversion ratio the SCC can have is n=2. As the input voltage increases so will the power processed in the PWM as shown by Fig. 3.4. At the maximum input voltage, the PWM converter input voltage will be 72V – 2*12V = 48V and processing 66.66% of the total power. At this point the SCC is no longer processing the majority of the power and the benefit of a small regulating PWM converter is lost. For applications, such as telecom power supply, with large input voltages it will be necessary to limit the PWM power by achieving multiple conversion ratios on the SCC.

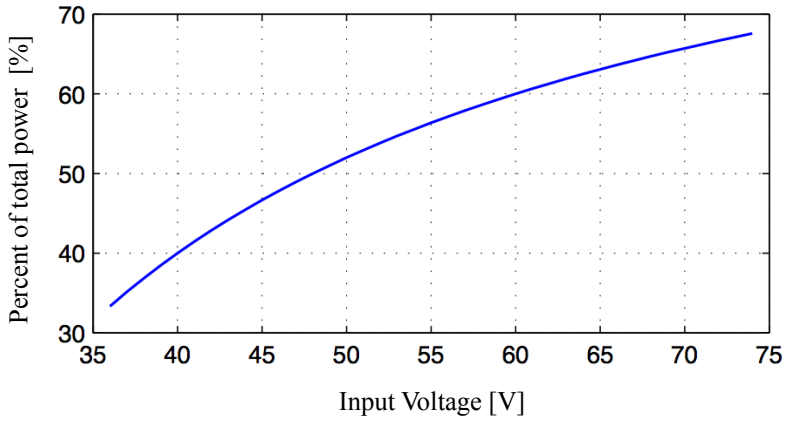


Fig. 3.4. The percentage of total power processed by the PWM with 2:1 SCC operating over the QRPSC input voltage range (36V to 72V).

If the SCC, while still unregulated, is able to achieve multiple conversion ratios n with minimal added complexity then a maximum PWM power rating can be chosen as the design requirement in terms of SCC topology selection. There are SCC that can achieve numerous non-integer conversion ratios [21] but require numerous different switching patterns. Utilizing these conflicts with the main objective of using a simple unregulated SCC. If the conversion ratios are limited to a few discrete values then

multiple conversion ratios can be obtained with little complexity [8,28].

The required conversion ratios can be found by setting a power limit for the PWM converter. With a power limit set, then for the given input voltage range the conversion ratios can be identified to prevent the PWM from converting more than the set power limit. A plot for the telecom application's required conversion ratios for a given power limit is shown in Fig. 3.5. The lower the percentage of power the PWM is designed to convert, the more conversion ratios must be provided in the SCC. It becomes evident that the SCC will need multiple conversion ratios to minimize the power, size, and cost of the regulating PWM converter in the telecom application of the QPRSCC.

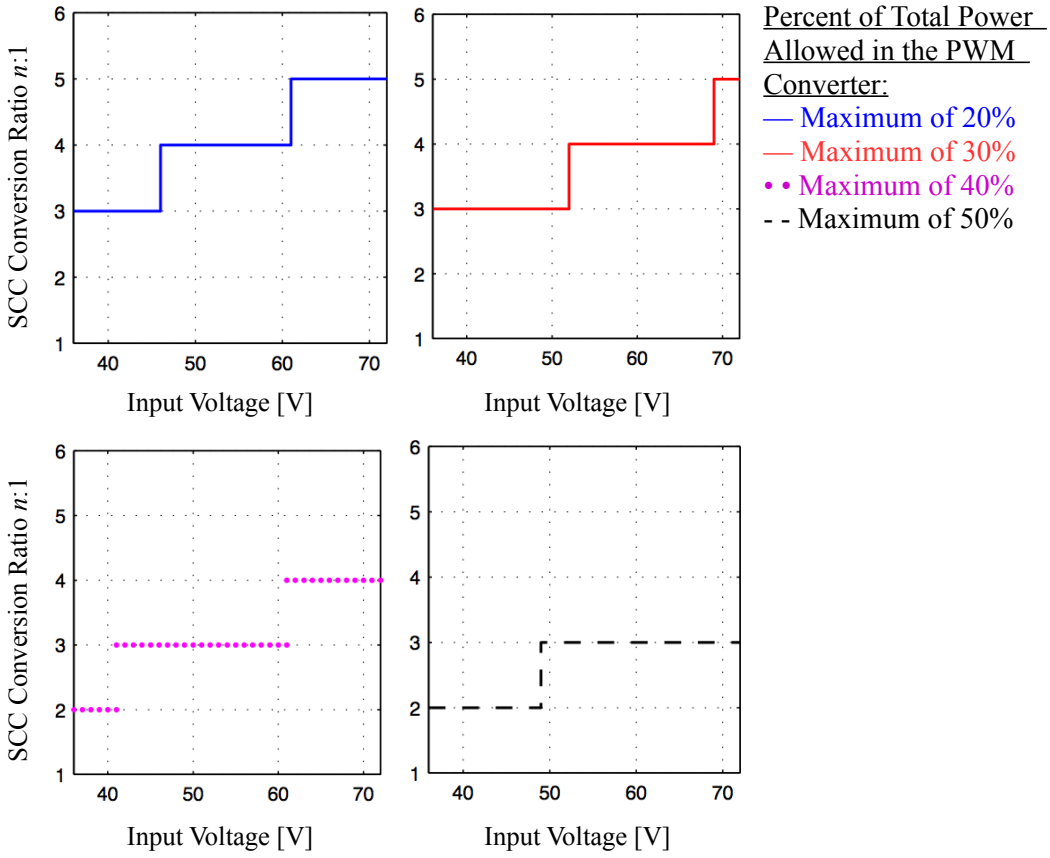


Fig. 3.5. The SCC conversion ratios n:1 over the QRPSC input voltage range for selected maximum PWM power in terms of percentage of the total power.

B. SCC Topology Selection

The requirement for multiple conversion ratios and a simple method to switch between them greatly reduces the number of switched-capacitor converters to consider. There are some SCC which can produce numerous conversion ratios by switch phasing [21], but their implementation adds more complexity than desired for the QPRSCC prototype. Other SCC, such as the Ladder and Dickson

Charge pump, can be augmented to have different taps where the input voltage is applied. Essentially the SCC is designed for the highest conversion ratio and either the access point for the input or the output is changed via different switches. An example of a ladder topology with this approach is taken from [28] and shown here in Fig. 3.6.

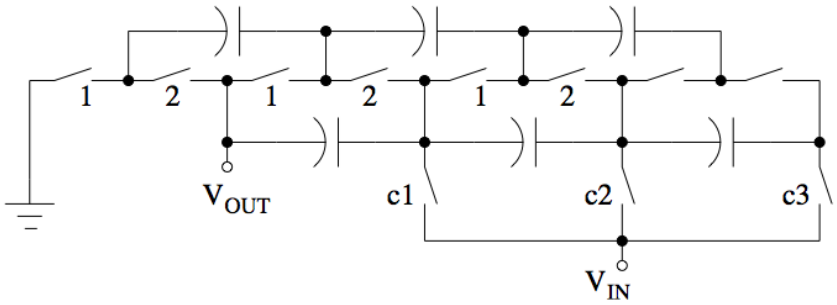


Fig. 3.6. Step down ladder with different 'taps' for the input voltage allowing multiple integer conversion ratios [28]

Another SCC converter that achieves multiple conversion ratios is the multilevel modular switched-capacitor converter (MMSCC) [8]. The MMSCC is a two phase SCC that is bi-directional, can achieve high conversion ratios without increasing switch voltage stresses, and possess excellent capacitor utilization (low and equal current stress). The MMSCC is designed with modules which can be bypassed or activated to achieve any number of integer conversion ratios [50-55]. The conversion ratio achievable is *k+1* where *k* is the number of modules. Bypassing a module is done by turning off the bottom two switches in the module and setting the floating MOSFET to be always on. The designed isolated MMSCC for the QPRSCC is shown in Fig. 3.7 with the modules labeled.

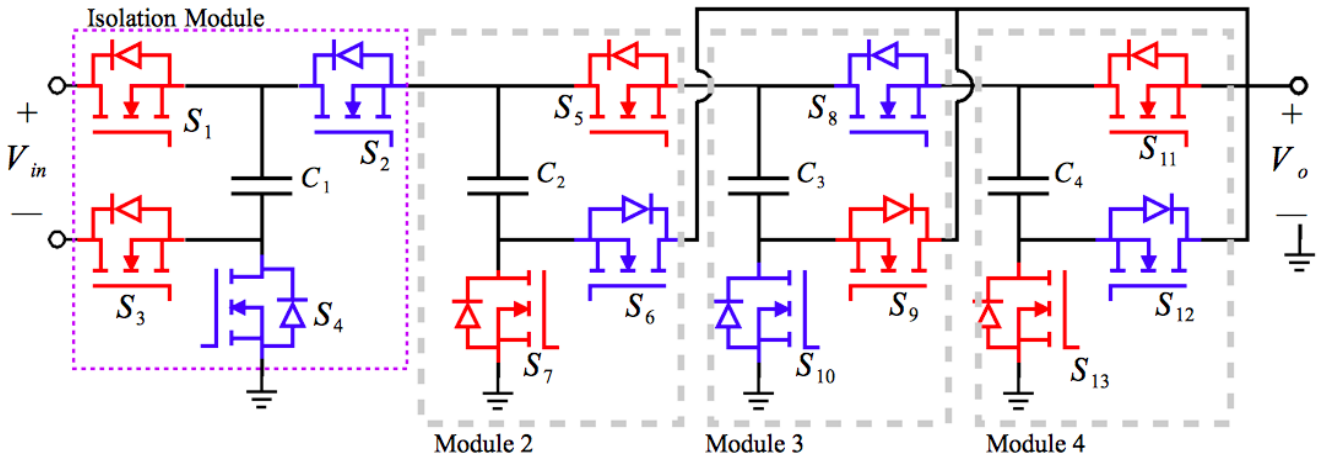


Fig. 3.7. The two phase isolated multilevel modular switched-capacitor converter (red MOSFETs indicate phase 1 and blue MOSFETs phase 2)

The MMSCC is chosen as the SCC for its proven ability to operate at power levels from a hundred watts to a few kilowatts, achieve high efficiencies, and adjust its conversion ratio [5-11,21]. In addition, the MMSCC allows for a simplified gate drive as each module has two MOSFETS that can be driven by commercially available synchronous HS/LS gate drivers. The only complicated gate drive is the floating MOSFET seen in each module. In comparison, the Ladder SCC shown in Fig. 3.6 has a total of 8 switches 7 of which are floating. In order to be used with the quasi-parallel topology the MMSCC is combined with the ground isolation strategy from [20] to create the isolated MMSCC shown in Fig. 3.7.

Since the MMSCC can achieve any integer conversion ratio up to $k+1$, where k is the number of modules not counting the isolation module (Fig. 3.7), it is necessary to find the max conversion ratio for the QPRSCC. As discussed previously, the higher the conversion ratios achieved, the lower the required power rating of the regulating PWM converter. Higher conversion ratios require more modules increasing cost and the physical area of the SCC. The percentage of power converted by the PWM converter as a function of the QPRSCC input voltage with increasing achievable conversion ratio for the MMSCC is plotted in Fig. 3.8. The conversion ratio of the MMSCC is changed to the next conversion ratio (e.g. 2:1 to 3:1) once the input voltage of PWM will be 4V with the new conversion ratio. To clarify, at 40V the MMSCC can operate as 3:since as the MMSCC will have an input voltage of 36V leaving 4V for the input voltage of the PWM. At 39V the PWM would only see 3V and thus the MMSCC will operate as 2:1. This minimum input voltage of 4V chosen by a rule of thumb for boost converters. It is best to keep the conversion ratio less than 1:3 (input to output) and with 12V output voltage then the minimum input voltage should be 4V. When the QPRSCC is actually implemented the LT8705 will be utilized for control and it has under voltage lock out implemented at around 4V as well.

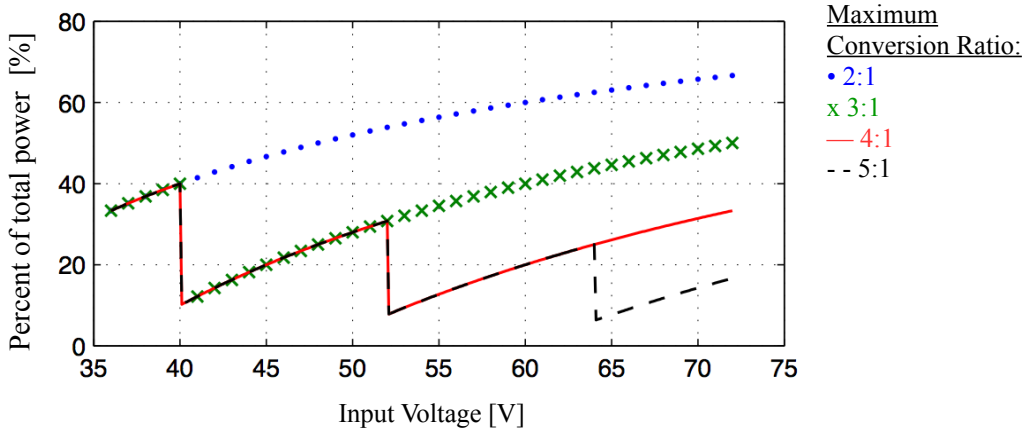


Fig. 3.8. Maximum allowed power for the PWM (in terms of percentage of total power) given selected maximum SCC conversion ratios *n*:1 over the QPRSCC input voltage range

It becomes evident from Fig. 3.8 that because the SCC cannot operate as 3:1 below an input voltage of 40V (to keep at least 4V on the PWM and maintain regulation) the PWM will have to be rated at a minimum of 40% of the QPRSCC power rating. In order to keep the PWM power rating at 40% of the total power then a max conversion ratio of 4:1 is needed. The 4:1 MMSCC has been selected as the SCC for the QPRSCC, as the input voltage increases to the QPRSCC the MMSCC will activate modules to increase it's conversion ratio from 2:1, 3:1, and to 4:1. This will limit the input voltage, i.e. the power, of the PWM converter. The MMSCC will change conversion ratios at approximately 40V for 2:1 and 3:1 operation and at 52V for 3:1 and 4:1 operation.

C. PWM Topology Choice

With the SCC topology selected as a 4:1 MMSCC a suitable topology for the regulating PWM converter needs to be selected. The PWM converter should have simple control, high efficiency, and low component count. The regulating PWM converter will also need to be a non-inverting buck-boost topology due the selected voltage range of 4V to 24V (seen at the PWM input) and a 12V output. This can be seen in Fig. 3.9 as the QPRSCC input voltage increases so does the PWM input voltage until the transition voltages are reached at which time the MMSCC will change it's conversion ratio. For the telecom application described here, the PWM input voltage swings from below to above the output voltage thus requiring a buck-boost topology.

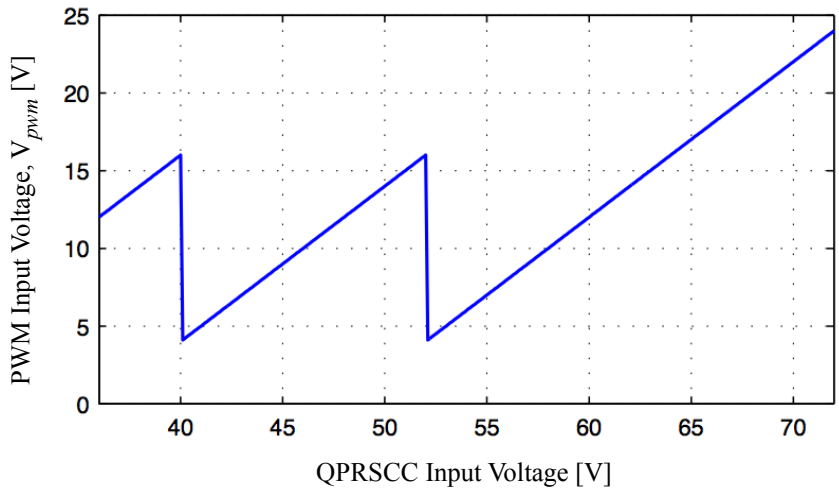


Fig. 3.9. The input voltages for the regulating PWM converter indicate it must be a non-inverting buck-boost converter for a QPRSCC with a 4:1 MMSCC

The SEPIC, Zeta, and DC/DC H-bridge converters will be considered since they are well documented and there are commercially available power management ICs for control and regulation [56-63]. The SEPIC and Zeta converters are both fourth order systems with two inductors, a series capacitor, and a filter output capacitor. Both exhibit two resonant peaks in their duty cycle to output voltage transfer function since the transfer function has two pairs of complex conjugate poles. There are also a pair of complex zeros that, depending on component values, will be in the right half plane (RHP) or left half plane (LHP). RHP zeros are extremely undesirable as each will add 180 degree phase lag. The SEPIC also has one real RHP zero that is common to all boost derived topologies [60-63], while the Zeta converter does not as it is a buck derived topology. The RHP zero found in boost derived topologies can be removed by implementing current mode control [56]. Since SEPIC and Zeta converters are fourth order, design and control are complex and generally limited in terms of bandwidth.

The other converter considered is the DC/DC H-bridge converter. The H-bridge combines a buck and boost converter utilizing four active switches (realized with synchronous MOSFETS or MOSFETs and diodes), one inductor, and an output filter capacitor as shown in Fig. 3.10. Analog and DSP based controls strategies are outlined in [64-66] and have achieved efficiencies over 95% [64]. The H-bridge does have a RHP zero, having a boost derived topology that can be eliminated with current model control. One disadvantage of the H-bridge is having to control and drive four different MOSFETs. Using commercially available power management ICs, such as the LT8705 provided by Linear Technology, provides current mode control and the necessary gate drive in a single package.

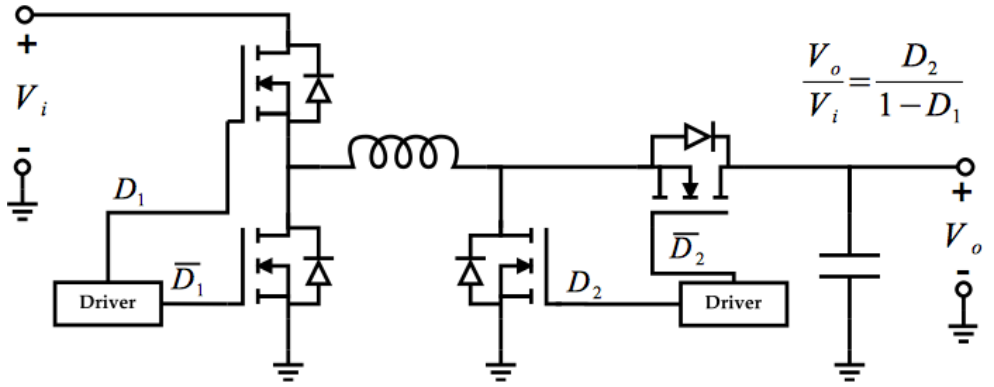


Fig. 3.10. The H-bridge DC/DC Converter utilizes one inductor and an output capacitor

The DC/DC H-bridge converter was selected for the QPRSCC because it only requires one inductor and a small output capacitor, which for the QRPSC will be provided by the SCC output capacitor. The SEPIC and Zeta both require two inductors and a flying series capacitor, (generally a large component). The H-bridge provides a simplified and generally faster control since it is a second order system compared to the fourth order systems of the SEPIC and Zeta. The one disadvantage of the H-bridge, namely the four active switches, is mitigated by utilizing the LT8705 which will provide current mode control and gate drive for the switches.

3.2 Isolated Multilevel Modular Switched-Capacitor Converter

The multilevel modular switched-capacitor converter (MMSCC) is chosen as the switched-capacitor converter for its proven ability to operate at power from a hundred watts to kilowatts [5-11], obtain high efficiencies [5-8,10], and adjust its conversion ratio while in operation [8]. In order to be used with a quasi-parallel topology, the MMSCC is combined with the ground isolation strategy from [20] to create the isolated MMSCC shown in Fig. 3.34. The isolated MMSCC is four-level MMSCC with the usual three modules and an added isolation module. The isolated MMSCC is a two-phase SCC; the two phases are color coded in Fig. 3.34. The quasi-parallel regulated switched-capacitor converter prototype is designed to be roughly 120W, i.e. 10A at 12V output. The isolated MMSCC will need to be designed to handle the majority of the power. For the prototype the MMSCC is designed for a maximum output of 9A (108W).

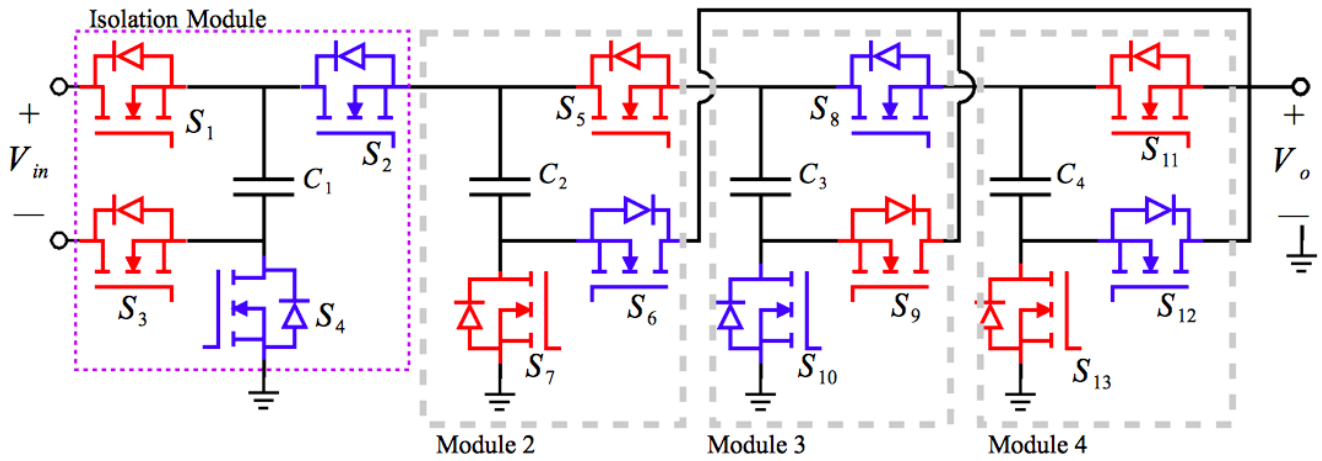


Fig. 3.11. The two phase isolated multilevel modular switched-capacitor converter (red MOSFETs indicate phase 1 and blue MOSFETs phase 2)

3.2.1 Modeling and Design of the Isolated MMSCC

The chosen design of the MMSCC allows for the choice of switching frequency and capacitance to achieve to the desired efficiency and size. Ideally, large capacitance and low MOSFET resistances will achieve the highest efficiency but to be competitive in terms of power density, some compromise between area and efficiency must be made. One objective of this research is to implement a SCC using ceramic capacitors and switching frequency in the hundreds of kilohertz, reducing the required capacitance and size so that the SCC can use ceramic capacitors.

In steady state, a SCC can be modeled as a DC transformer with an output impedance (Fig. 3.12). The output impedance is bounded by two asymptotic limits, the slow switching limit and fast switching limit [25]. This modeling approach will be outlined in subsection A, obtaining the required switching frequency and capacitance in subsection B. Steady state analysis also provides the blocking voltages seen by the switches and the rated voltages needed for the switching capacitors. Once the MMSCC component values have been chosen, a dynamic analysis using DSSA will be presented in subsection C, focusing on the choice of the sampling time within the switching period to provide an averaged small-signal model.

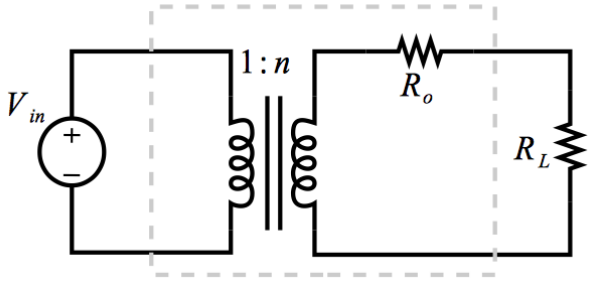


Fig. 3.12. Steady-state model of an unregulated SCC with an equivalent output impedance R_o

A. Steady State Modeling

The MMSCC will now be analyzed to identify the steady-state output impedance, capacitor voltages, and the switch blocking voltages. This analysis will provide the groundwork for the component and switching frequency selection following the design methodology given in [33]. The output impedance has two asymptotic limits, R_{SSL} and R_{FSL}, which can be found from the capacitor charge multiplier vector and the resistance charge multiplier vector.

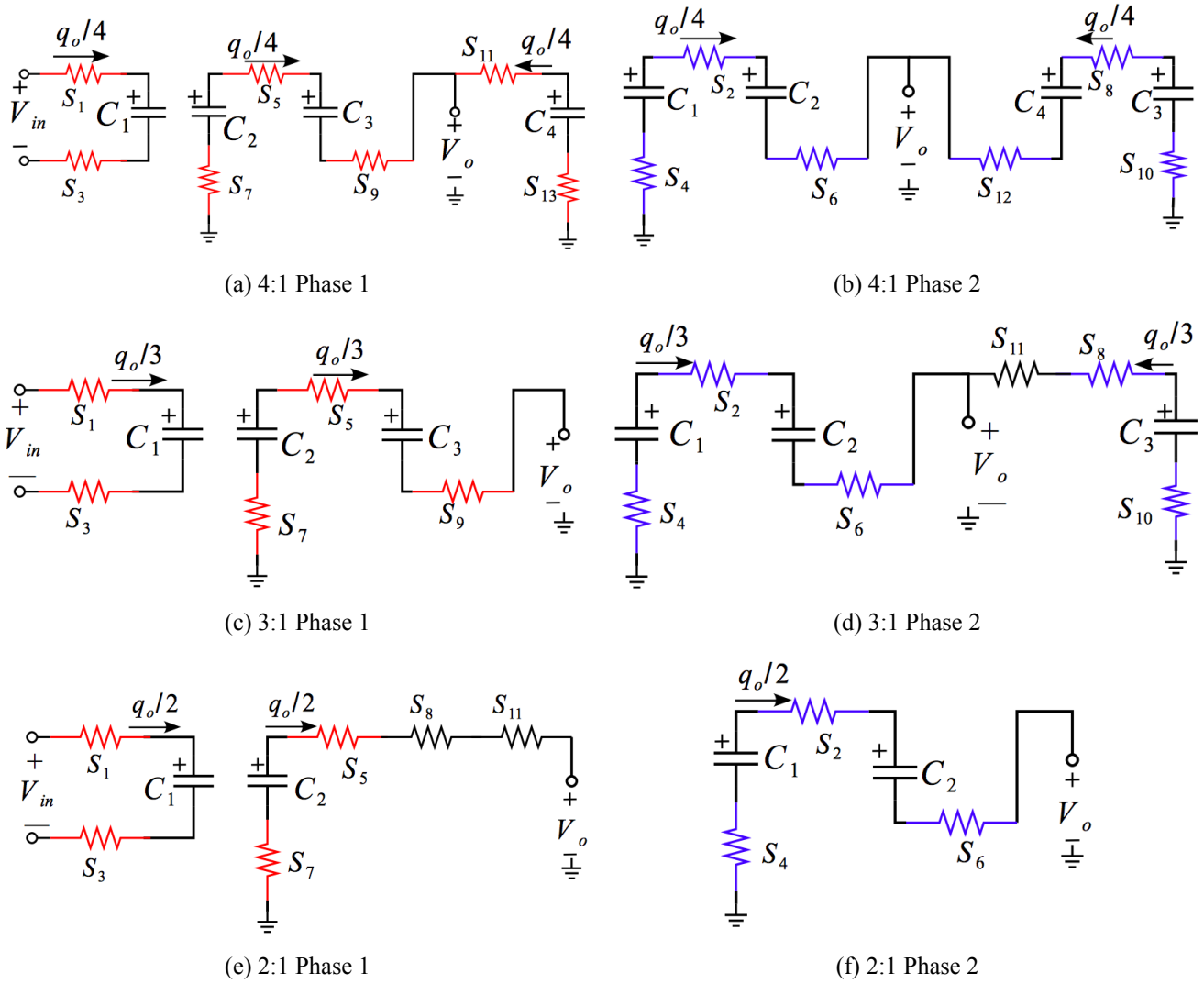


Fig. 3.13. The MMSCC sub-circuits with charge flows when operating as 4:1 (a)phase 1 (b)phase 2, as a 3:1 (c)phase 1 (d)phase 2, and as a 2:1 (e)phase 1(f) phase 2

The MMSCC is shown in phase 1 and in phase 2 in Fig. 3.13(a) and Fig. 3.13(b) when operating with a 4:1 conversion ratio. The charge flow of the capacitors are found by inspection, as outlined in section 2.1.1, and displayed in Fig. 3.13. The capacitor and resistive charge multiplier vectors are (3.16) and (3.17) respectively. The position of element j in the charge multiplier vectors corresponds to the capacitor C_j or switch S_j.

$$\boldsymbol{a}_c^{4:1} = \left[\frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\right] \tag{3.16}$$

$$\boldsymbol{a}_r^{4:1} = \left[\frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\right] \tag{3.17}$$

The MMSCC while operating as a 3:1 converter has the sub-circuits with the charge flows shown in Fig. 3.13(c) and Fig. 3.13(d). The capacitor and resistive charge multiplier vectors are (3.18) and (3.19) respectively.

$$\boldsymbol{a}_c^{3:1} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 \end{bmatrix} \tag{3.18}$$

$$\boldsymbol{a}_r^{3:1} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 \end{bmatrix} \tag{3.19}$$

Lastly the MMSCC while operating as a 2:1 converter has the sub-circuits with the charge flows shown in Fig. 3.13(e) and Fig. 3.13(f). The capacitor and resistive charge multiplier vectors are (3.20) and (3.21) respectively.

$$\boldsymbol{a}_c^{2:1} = \begin{bmatrix} \frac{1}{2} & \frac{1}{2} & 0 & 0 \end{bmatrix} \tag{3.20}$$

$$\boldsymbol{a}_r^{2:1} = \begin{bmatrix} \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & 0 & 0 & \frac{1}{2} & 0 & 0 \end{bmatrix} \tag{3.21}$$

From the charge multiplier vectors, the slow switching limit impedance and the fast switching limit impedance, R_{SSL} and R_{FSL}, can be calculated for 4:1, 3:1, and 2:1 operation. If it is assumed that each capacitor has the same capacitance and each switch has the same on resistance then a single equation can be written for each switching limit impedance. Examining the capacitor charge multiplier vectors, (3.16), (3.18), and (3.20), one sees that the number of operating capacitors and charge flow are n and $1/n$ where n is the conversion ratio. For the resistive multiplier vectors, (3.17), (3.19), and (3.21), each element is also $1/n$ while the number of operating switches is $5 + 2n$. Using these assumptions, R_{SSL} and R_{FSL} can be written as (3.22) and (3.23), respectively where n is the conversion ratio, C is the capacitance of the switching capacitors, f_{SW} is the MMSCC switching frequency, there obtains

$$R_{SSL} = \frac{1}{C f_{SW}} \sum_{i=1}^{n} \left(\frac{1}{n}\right)^2 = \frac{1}{C f_{SW}} n \left(\frac{1}{n^2}\right) = \frac{1}{n C f_{SW}} \tag{3.22}$$

$$R_{FSL} = 2 R_{ds-on} \sum_{i=1}^{13-2n} \left(\frac{1}{n}\right)^2 = 2 R_{ds-on} \left(\frac{5+2n}{n^2}\right) \tag{3.23}$$

The fast switching limit impedance, R_{FSL}, can be modified to include capacitor ESR giving (3.24).

$$R_{FSL} = 2\,R_{ds-on}\left(\frac{5+2n}{n^2}\right) + 4\,R_{ESR}\frac{1}{n} \tag{3.24}$$

Finally the total output impedance can be approximated by (3.31).

$$R_o = \sqrt{R_{FSL}^2 + R_{SSL}^2} \tag{3.25}$$

The voltages seen on the capacitors can be found by inspection of Fig. 3.13(a)-(f) for each mode of operation of the MMSCC (4:1, 3:1, and 2:1). In steady state, each capacitor will have a constant voltage (the rated voltage of the capacitor will have to be larger than this value). Similarly, once the voltage of the capacitors are known, the blocking voltages seen by each switch can also be found by inspection of Fig. 3.34. The capacitor's voltages for each mode of operation are shown in Table 3.1. The blocking voltages of the switches are shown in Table 3.2. The average current seen in each switch is the output current divided by *n,* the conversion ratio of the MMSCC. Assuming the MMSCC is operating in the FSL, the current waveforms can be approximated by square waves. Thus the current in the switch will be the average current divided by the duty ratio (here 50%). The current in the switch is ($2I_o$ /*n*). If operating on the boundary of the SSL and FSL a SCC will have partial charging, i.e. the current behaves roughly linearly [67]. Thus the current's waveform can be approximated to have a 50% ripple. The approximate peak currents in the switches are given in Table 3.3.

TABLE 3.1: SUMMARY OF MMSCC CAPACITOR VOLTAGES

Conversion Ratio	C_1	C_2	C_3	C_4
4:1	$4V_o$	$3V_o$	$2V_o$	V_o
3:1	$3V_o$	$2V_o$	V_o	0
2:1	$2V_o$	V_o	0	0

TABLE 3.2: SWITCH BLOCKING VOLTAGES FOR THE MMSCC

Conversion Ratio	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}
4:1	V_{in}- $4V_o$	V_{in}- $3V_o$	V_{in}- $4V_o$	V_{in}- $4V_o$	$2V_o$	V_o	V_o	$2V_o$	V_o	V_o	V_o	V_o	V_o
3:1	V_{in}- $3V_o$	V_{in}- $2V_o$	V_{in}- $3V_o$	V_{in}- $3V_o$	$2V_o$	V_o	V_o	V_o	V_o	V_o	0	0	V_o
2:1	V_{in}- $2V_o$	V_{in}- V_o	V_{in}- $2V_o$	V_{in}- $2V_o$	V_o	V_o	V_o	0	0	V_o	0	0	V_o

TABLE 3.3: APPROXIMATED PEAK CURRENTS IN THE SWITCHES FOR THE MMSCC

Conversion Ratio	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}
4:1	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$	$3I_o/4$
3:1	I_o	I_o	I_o	I_o	I_o	I_o	I_o	I_o	I_o	I_o	I_o	0	0
2:1	$3I_o/2$	$3I_o/2$	$3I_o/2$	$3I_o/2$	$3I_o/2$	$3I_o/2$	$3I_o/2$	$3I_o/2$	0	0	$3I_o/2$	0	0

Having set the asymptotic limits of the output impedance and the voltages seen by the capacitors and switches one may now design the MMSCC. The output impedances R_{SSL} and R_{FSL} will determine an appropriate switching frequency as well as the capacitance of the switching capacitors.

B. Determining Component Values and Switching Frequency

In common power converters (e.g. a Buck converter), the switching losses are proportional to the switching frequency. As the switching frequency is increased so are the switching losses. For SCC this is not necessarily the case. Low switching frequencies cause high peak currents leading to high conduction and switching losses [11]. Increasing the switching frequency, approaching the fast switching limit, will decrease the peak charging and discharging current leading to smaller RMS currents [11] as well as decreased the output impedance. Once the switching frequency reaches the corner frequency, i.e. the intersection of R_{SSL} and R_{FSL}, the current is almost a square wave and the output impedance is approaching it's minimum (R_{FSL}). Increasing switching frequency beyond this point will provide no additional benefits and simply increase the switching losses of the MOSFETs. Thus the ideal switching frequency is near the intersection of the asymptotic switching limits impedances R_{SSL} and R_{FSL} [33]. In general the most efficient SCC will have large capacitance and low switch on resistances.

In this section the MMSCC will be analyzed in the different operating modes (4:1, 3:1, and 2:1) to identify the proper operating point. Then MOSFETs will be chosen to construct the switches, giving an estimate of R_{FSL} and switching losses. Using the calculated conduction and switchings losses a suitable range of switching frequencies will be chosen to obtain high efficiency. Lastly, from the range of switching frequencies the necessary capacitance of the switching capacitors will be calculated. The final value of capacitance and switching frequency will be chosen to minimize the size of the capacitors while maintaining an acceptable efficiency.

Unlike the SCC in [33] the designed isolated MMSCC achieves multiple conversion ratios (4:1, 3:1,

and 2:1) by turning off modules which alter the R_{SSL} and R_{FSL}. The change in R_{SSL} and R_{FSL} will lead to three different "optimal" operating frequencies as shown in Fig. 3.14. One approach is to change the switching frequency to the "optimal" frequency as the conversion ratio changes. This approach adds negligible complexity to the control of the MMSCC. A second approach is to keep the switching frequency fixed and design the MMSCC at the intersection of 4:1 operation. This will ensure the MMSCC will be in or on the cusp of the FSL operation regardless of the operation mode as shown in Fig. 3.14.

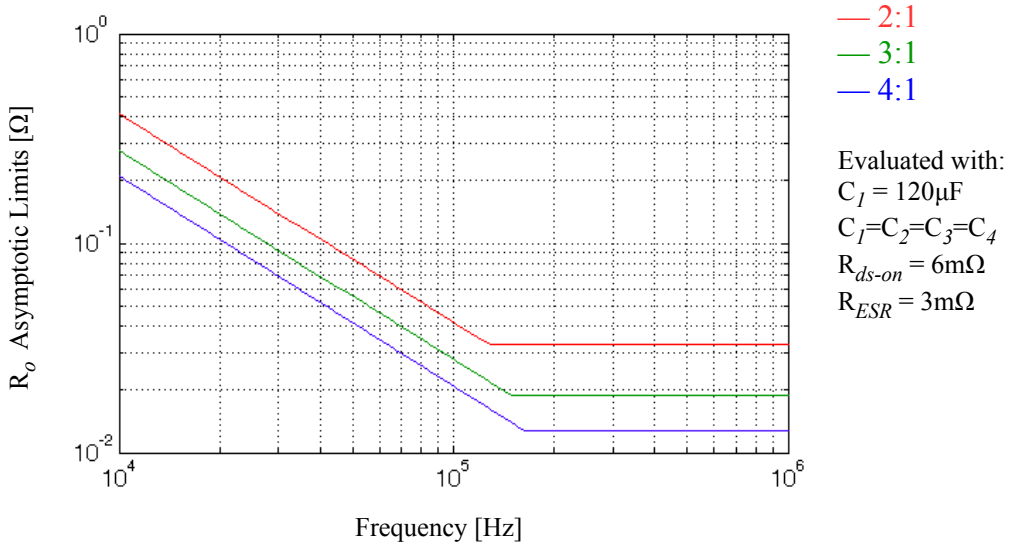


Fig. 3.14. The MMSCC equivalent output impedance asymptotic limits

A third method is to choose the capacitances of C_1, C_2, C_3, and C_4 such that R_{SSL} will intersect with R_{FSL} at the same or approximately the same switching frequency. If it is assumed that $C_1 = C_2 = C$ then the intersection of R_{SSL} and R_{FSL} will happen at f_c which can be solved for using (3.26). Using the other two modes of operation, a system of equations relating R_{FSL} and R_{SSL} obtains as in (3.27), where α_j is the ratio of the jth capacitor capacitance, C_j , to C and where $a_{c,i}^{n:1}$ is the ith element of the capacitor charge multiplier vector for operation of the MMSCC as n:1. Equation (3.27) can then solved for the ratios α_j (3.28).

$$f_c = \frac{1}{2C\,R_{FSL,2:1}} \tag{3.26}$$

$$\begin{bmatrix} R_{FSL,2:1} \\ R_{FSL,3:1} \\ R_{FSL,4:1} \end{bmatrix} = \frac{1}{C f_c} \begin{bmatrix} a_{c,1}^{2:1} + a_{c,2}^{2:1} & 0 & 0 \\ a_{c,1}^{3:1} + a_{c,2}^{3:1} & a_{c,3}^{3:1} & 0 \\ a_{c,1}^{4:1} + a_{c,2}^{4:1} & a_{c,3}^{4:1} & a_{c,4}^{4:1} \end{bmatrix} \begin{bmatrix} \frac{1}{\alpha_2} \\ \frac{1}{\alpha_3} \\ \frac{1}{\alpha_4} \end{bmatrix} \tag{3.27}$$

$$\begin{bmatrix} \frac{1}{\alpha_2} \\ \frac{1}{\alpha_3} \\ \frac{1}{\alpha_4} \end{bmatrix} = \begin{bmatrix} 1 \\ \frac{4\left(R_{ESR} + R_{ds-on}\right)}{4R_{ESR} + 9R_{ds-on}} \\ \frac{4\left(R_{ESR} + R_{ds-on}\right)}{4R_{ESR} + 9R_{ds-on}} \end{bmatrix} \tag{3.28}$$

Evaluating (3.28) assuming an $R_{ds\text{-}on}$ of 6mΩ and R_{ESR} of 3mΩ gives $C_1 = C_2 = 1.83\,C_3 = 1.83\,C_4$. In Fig. 3.14, the intersecting frequency, f_c, occurs roughly at 170kHz for the 4:1 MMSCC. To obtain f_c = 170kHz $C_1 = C_2 \approx 90\mu\text{F}$ thus $C_3 = C_4 \approx 165\,\mu\text{F}$, plotting the output impedance asymptotic limits in Fig. 3.15 shows that intersecting frequency occurs at 170kHz when operating as 4:1, 3:1 and 2:1. Using this constant f_c ratio in this example only required 10μF additional capacitance compared to the MMSCC depicted in Fig. 3.14 which had C_1=C_2=C_3=C_4=120μF. In addition to aligning the intersecting switching frequencies, utilizing a constant f_c ratio minimizes the total energy of the MMSCC thus decreasing the total area required by the capacitors. The total energy of a SCC is given by (3.29), evaluating the MMSCC in each operating mode assuming each capacitor is 120μF and assuming $C_1 = C_2 \approx 90\,\mu\text{F}$ $C_3 = C_3 \approx 165\,\mu\text{F}$ yields total energy in (3.30) and (3.25).

$$E_C = \frac{1}{2} \sum_{i \in caps} C_i V_i^2 \tag{3.29}$$

$$E_{C1,C2,C3,C4=120\mu\text{F}} = 15\,C_1 V_o^2 = 0.0018\,V_o^2 \ [\text{J}] \tag{3.30}$$

$$E_{\substack{C1,C2=90\mu\text{F} \\ C3,C4=165\mu\text{F}}} = 17.0825\,C_1 V_o^2 = 0.0015\,V_o^2 [\text{J}] \tag{3.31}$$

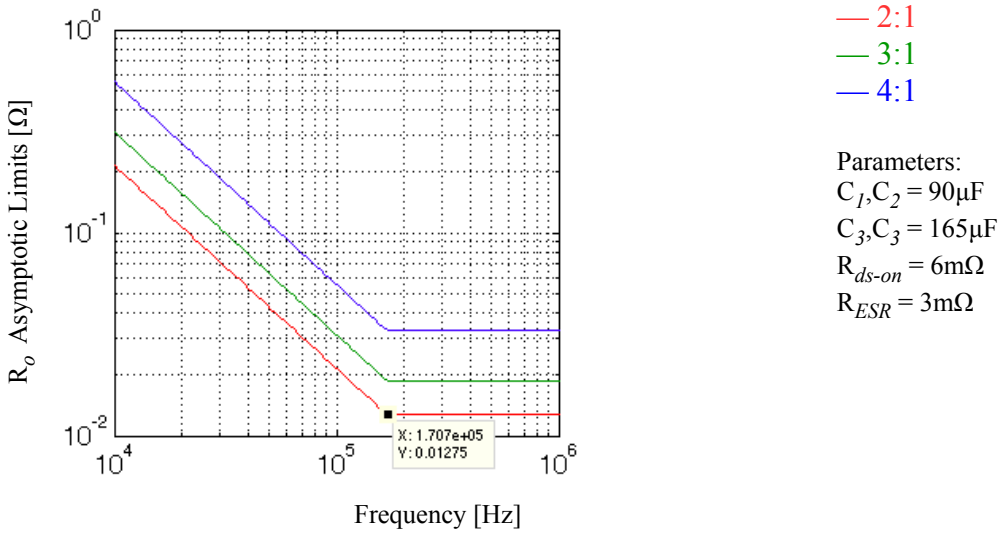


Fig. 3.15. MMSCC's output impedance asymptotic limits employing "constant f_c ratio"

Despite the benefits of the last method (the constant f_c ratio), this method was not utilized in the design of the MMSCC due to inexperience in SCC design. Instead the MMSCC will be designed to be near the cusp of the FSL while operating with a 4:1 conversion ratio. The MMSCC will be controlled by a microcontroller allowing for the switching frequency to be changed with no added complexity as the MMSCC changes operating modes (4:1, 3:1, and 2:1). This will keep the MMSCC operating at the desired intersection of R_{FSL} and R_{SSL}.

Following this design methodology [33] MOSFETs were chosen that have low switch resistances and meet the current and voltage stress requirements. The output voltage of the MMSCC will be the same as the output voltage of the QPRSCC (12V). From Table 3.2 the minimum blocking voltage required for each switch in each operating mode is given in Table 3.4. The switches are then designed for the maximum voltage which occurs in the 4:1 configuration. To find the current ratings of the MOSFETs, the MMSCC is assumed to be operating in FSL or near FSL operation. The peak currents approximated in Table 3.3 are calculated with an output current of 9A. The average and peak currents for switches are then given in Table 3.5, with the highest currents occurring in 2:1 configuration.

TABLE 3.4: MAXIMUM BLOCKING VOLTAGE OF SWITCHES IN THE MMSCC

Conversion Ratio	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}
4:1	24V	36V	24V	24V	24V	12V	12V	24V	12V	12V	12V	12V	12V
3:1	20V	32V	20V	20V	24V	12V	12V	12V	12V	12V	0	0	12V
2:1	18V	30V	18V	18V	12V	12V	12V	0	0	12V	0	0	12V

TABLE 3.5: SUMMARY OF APPROXIMATE CURRENTS IN THE SWITCHES OF THE MMSCC

Conversion Ratio	Average Current	Approx. Peak Current
4:1	2.25 A	6.75A
3:1	3 A	9
2:1	4.5 A	13.5A

As a prototype the switches S1 through S5 have been oversized in case the full maximum input voltage of 72V were to be applied. The MOSFETs are chosen to be oversized in terms of power rating so they can be operated without heat sinks. Using the voltage and current requirements outline in Table 3.4 and Table 3.5 and trying to achieve low on resistance, $R_{DS(ON)}$, the MOSFETS AON6280 and PSMN3R9 are selected for the MMSCC. A summary of the MOSFET properties are given in Table 3.6. Since the output capacitance is nonlinear and is dependent on V_{DS} it is listed at the most common V_{DS} seen by each MOSFET in the MMSCC.

TABLE 3.6: SUMMARY OF MOSFET PROPERTIES

MOSFET	V_{DS}	I_D (V_{GS}=10V)	maximum $R_{DS(ON)}$ (V_{GS}=10V) @25ºC	Q_G (V_{GS}=10V)	C_{OSS}
AON6280	80V	85A	4.1mΩ	54nC	1200pF (V_{DS}=24V)
PSMN3R9-25MLC	25V	70A	4.15mΩ	24nC	400pF (V_{DS}=12V)

The FSL output impedance must now be approximated. At the fast switching limit, R_{FSL} is dictated by the switches' on resistance and the capacitors ESR. A quick examination of available ceramic capacitors found that: (1) the switching capacitors will be made from several ceramic capacitors in parallel and (2) a ceramic capacitor ESR is typically less than 15mΩ. A search of TDK's ceramic capacitors by characteristics found no capacitors with an ESR over 10mΩ when restricted to a capacitance of 10uF with a voltage rating over 35V [68]. Paralleling capacitors will increase the equivalent capacitance but decreases the equivalent ESR. With this in mind, the switching capacitors ESR will be approximated to be 3mΩ. The PCB trace resistance was not considered here as the PCB layout has not yet been designed. However experimental results indicated that PCB trace resistance would significantly affect the R_{FSL} in this design. The MOSFET $R_{DS(ON)}$ will be assumed to experience an operating junction temperature rise of 80º C, with 0.4%/C variability, a temperature factor ρ_T=1.32 will be used. The approximate R_{FSL} can then be calculated as (3.32).

$$R_{FSL,4:1} = \frac{2(13)}{16} R_{DS(ON)@25C} \rho_T + R_{ESR} = 11.8\text{m}\Omega \qquad (3.32)$$

At a maximum output current of 9A the maximum conduction losses will be roughly 1W. To achieve 97% efficiency, one can allow 2.24W in switching losses. Plotting the switching losses at the QPRSCC's maximum input voltage of 72V and the MMSCC maximum load current of 9A and the maximum desired power loss of 2.24W in Fig. 3.16, shows that maximum switching frequency should be approximately 130kHz.

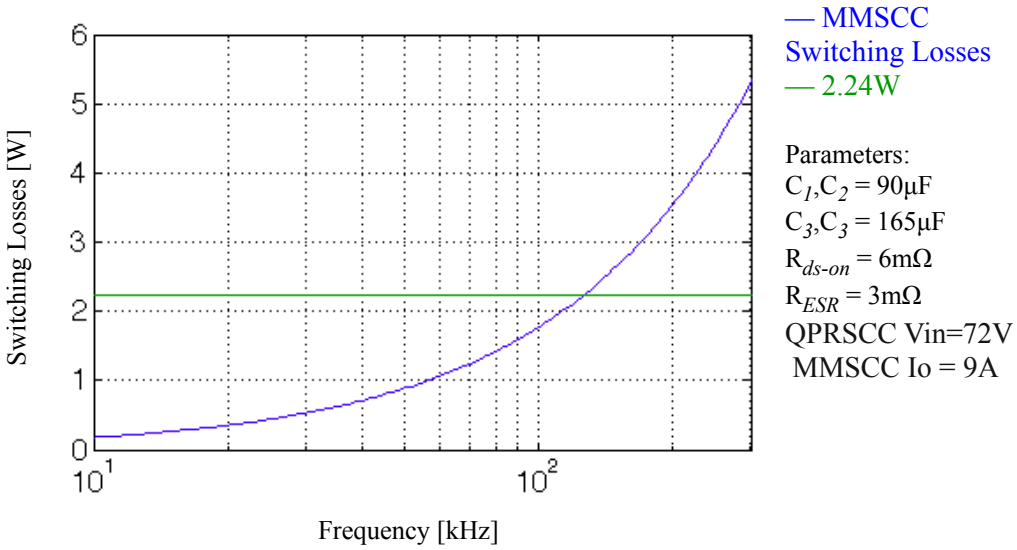


Fig. 3.16. Plot of the MMSCC's worst case switching losses

The required capacitance that yields an intersection frequency of R_{FSL} and R_{SSL} can be found by using (3.33). The resulting plot (Fig. 3.17) shows that to operate on the boundary of the FSL, each switching capacitor will need to be over 150µF. Balancing design size and efficiency, the capacitance is selected to be 120µF. This requires a switching frequency of roughly 180kHz which from Fig. 3.16 will result in roughly 3.2W of switching losses and an efficiency of 96%.

$$C = \frac{1}{4 f_{SW} R_{FSL,4:1}} \tag{3.33}$$

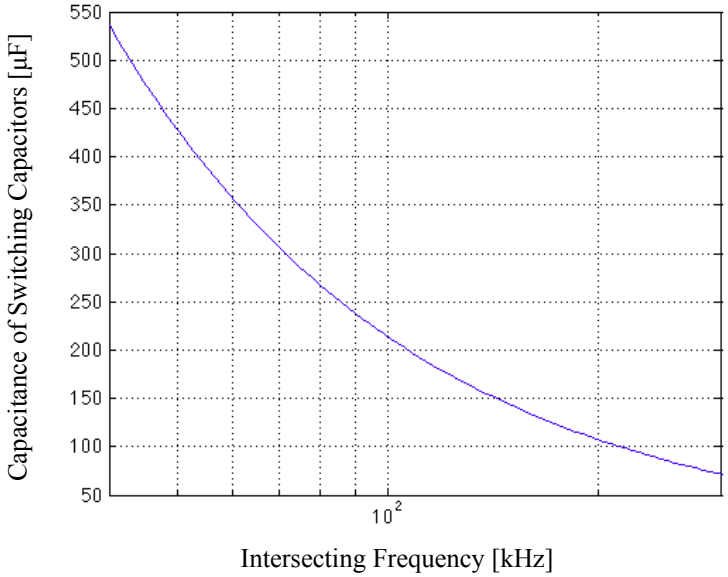


Fig. 3.17. Capacitance needed for a intersection of the R_{SSL} and R_{FSL} at a selected frequency

Having selected a switching frequency and capacitance values, there remains the choice of capacitors. The switching capacitance will have to be realized using multiple ceramic capacitors in parallel. The ceramic capacitors capacitance will also have to be derated due to the DC voltage bias as shown in Fig. 3.18 [68]. The loss of capacitance with increasing DC voltage in a ceramic capacitor is due to the physics of the device's material thus Fig. 3.18 is fairly representative of any ceramic capacitor made with X5R/S, X6R/S, and X7R/S. Loss of capacitance due to DC voltage can be mitigated by choosing capacitors that have a higher voltage rating and a larger package size. The realization of the capacitors C_1, C_2, C_3, and C_4 of the MMSCC is given in Table 3.7.

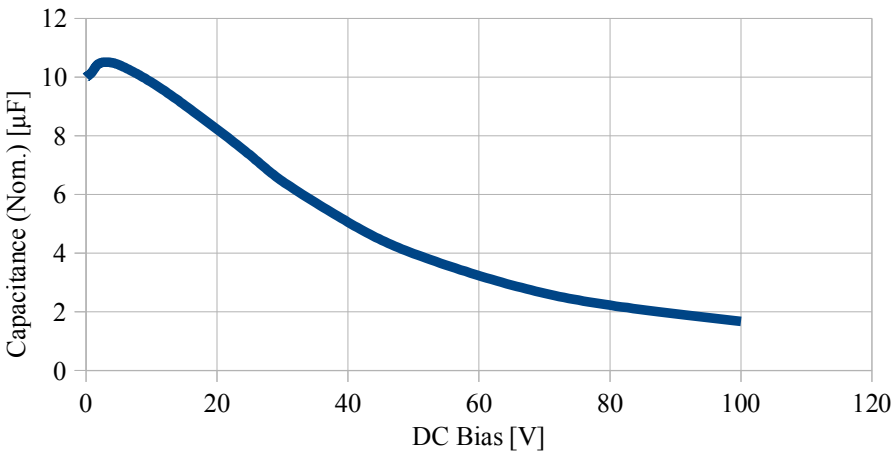


Fig. 3.18. Loss of capacitance on 10µF 100V X7S due to DC voltage [68]

TABLE 3.7: REALIZATION OF MMSCC SWITCHING CAPACITORS

Switching Capacitor	Capacitor Part No.	Capacitance	No. Used to Realize Cx	Nominal Capacitance	Estimated Capacitance at Operation for 4:1
C_1	C5750X7S2A106K230KB	15µF	16	240µF	100µF
C_2	C5750X7S2A106K230KB	15µF	16	240µF	128µF
C_3	UMK325BJ106MM-T	10µF	20	200µF	120µF
C_4	C4532X5R1E226M250KA	22µF	8	176µF	120µF

Since this is a prototype, it is prudent to have a design which more than adequate capacitance. The capacitors can easily be removed during experimentation to find the lowest needed capacitance. In the following analysis, it will be assumed the switching capacitors will be 120µF. A higher capacitance reduces the MMSCC output impedance pushing it further into the FSL.

C. Output Capacitor Value

For SCC a large output voltage ripple, ΔV_o, causes large peak currents in the switches and capacitors. Properly sizing the output capacitor ensure small output voltages and well behaved charging and discharging current waveforms. In each phase the MMSCC can be represented by a single equivalent capacitance (including the output capacitor) and the equivalent load resistance. The equivalent capacitance is function of the switching-capacitors and the output capacitance. The output voltage ripple ΔV_o is then estimated as (3.34) where $C_{eq}^{n:1}$ is the equivalent capacitance in a phase for n:1 mode of the MMSCC, I_o is the output current of the MMSCC, and f_{SW} is the switching frequency.

$$\Delta V_o = \frac{I_o T/2}{C_{eq}^{n:1}} = \frac{I_o}{2 C_{eq}^{n:1} f_{SW}} \tag{3.34}$$

The worst case output voltage ripple for the MMSCC will occur at full load(9A), operating in 3:1 mode, and during phase 1 when the equivalent capacitance is C_o + C_{sc} (where C_o is the output capacitor and C_{sc} is the switching-capacitor). Even though 2:1 mode would have a lower equivalent capacitance the maximum load seen is only 6A for the MMSCC. The required output capacitance can then be approximated by (3.35).

$$C_o = \frac{I_o}{2 f_{SW} \Delta V_o} - C_{sc} \tag{3.35}$$

A output voltage ripple of 70mV is chosen to keep the peak currents low and the discharging current waveform approximately linear (decreasing the RMS current value). This gives an output capacitance

of 330µF. The 3:1 MMSCC with the 330µF output capacitor and 9A load is simulated in LTSpice (Fig. 3.19) confirming the selection of output capacitance. The SPICE circuit used is shown in Fig. 3.22(b).

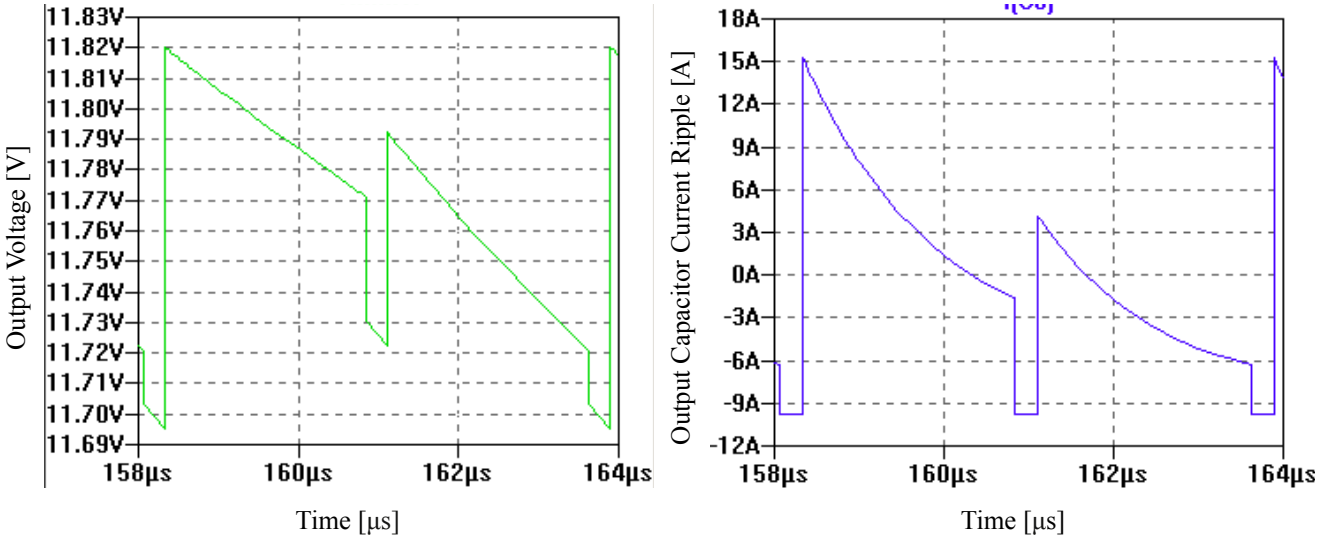


Fig. 3.19. LTSpice simulation of 3:1 MMSCC with 9A load verifying choice C_o= 330µF

D. Dynamic Modeling

The MMSCC dynamics are modeled using DSSA, the approach proposed by [29] and [33] covered in section 2.1.2. The output stage of the MMSCC is modeled by a Thévenin equivalent load as well as a current source representing the current from the H-Bridge as shown in Fig. 3.20.

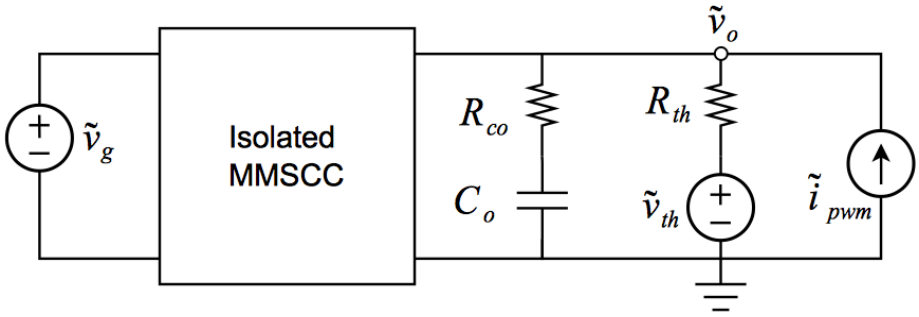


Fig. 3.20. Dynamic model of the isolated MMSCC with an output capacitor, Thévenin equivalent load, and a current source representing the regulating PWM converter

The model input **u** is given by (3.36). Each switching capacitor and the output capacitor will be a state variable giving **x** to be (3.37) and the capacitance matrix **C** to be (3.38).

$$\mathbf{u}=\begin{bmatrix} v_g & v_{th} & i_{pwm} \end{bmatrix}^T \tag{3.36}$$

$$\mathbf{x}=\begin{cases} \begin{bmatrix} v_{C1} & v_{C2} & v_{C3} & v_{C4} & v_{CO} \end{bmatrix}^T & when\ 4:1 \\ \begin{bmatrix} v_{C1} & v_{C2} & v_{C3} & v_{CO} \end{bmatrix}^T & when\ 3:1 \\ \begin{bmatrix} v_{C1} & v_{C2} & v_{CO} \end{bmatrix}^T & when\ 2:1 \end{cases} \tag{3.37}$$

$$\mathbf{C}_{4:1}=\begin{bmatrix} C_c & 0 & 0 & 0 & 0 \\ 0 & C_c & 0 & 0 & 0 \\ 0 & 0 & C_c & 0 & 0 \\ 0 & 0 & 0 & C_c & 0 \\ 0 & 0 & 0 & 0 & C_o \end{bmatrix} \quad \mathbf{C}_{3:1}=\begin{bmatrix} C_c & 0 & 0 & 0 \\ 0 & C_c & 0 & 0 \\ 0 & 0 & C_c & 0 \\ 0 & 0 & 0 & C_o \end{bmatrix} \quad \mathbf{C}_{4:1}=\begin{bmatrix} C_c & 0 & 0 \\ 0 & C_c & 0 \\ 0 & 0 & C_o \end{bmatrix} \tag{3.38}$$

In modeling the dynamics of the MMSCC the output voltage and the input current output variables. We wish to obtain a small-signal model of the MMSCC into the QPRSCC for analysis. It is necessary to represent the input and output dynamics of the MMSCC for the given model inputs (i.e. input voltage and output load). The input current will be approximated by the difference between the input voltage and the voltage on C_1 over the resistance seen by the input voltage. The output **y** for the system is then defined as (3.39).

$$\mathbf{y}=\begin{bmatrix} i_{in} & v_o \end{bmatrix}^T \tag{3.39}$$

The MMSCC is modeled with four different states, one of each phase and then one for each deadtime between phases. Analyzing the sub-circuits in Fig. 3.13 with KVL and KCL gives the matrices $\mathbf{E}_i$, $\mathbf{F}_i$, and $\mathbf{G}_i$ for phase 1 and 2. The sub-circuit for deadtime is the output stage: the output capacitor, the

Thevenin equivalent load, and the current source representing the H-Bridge as shown in Fig. 3.20. Analyzing the output stage during deadtime with KCL and KVL gives $\mathbf{E}_{dt}$, $\mathbf{F}_{dt}$, and $\mathbf{G}_{dt}$. The matrices $\mathbf{E}_i$, $\mathbf{F}_i$, and $\mathbf{G}_i$ are shown for the 3:1 MMSCC in Table 3.8 for phase 1, phase 2, and the deadtime. The matrices $\mathbf{E}_i$, $\mathbf{F}_i$, and $\mathbf{G}_i$ for 2:1 and 4:1 operation can be seen in Appendix A. The matrices $\mathbf{E}_i$, $\mathbf{F}_i$, and $\mathbf{G}_i$ are then solved for the familiar state space matrices $\mathbf{A}_i$ and $\mathbf{B}_i$.

TABLE 3.8: MATRICES FOR ACTIVE AND DEADTIME MODES OF 3:1 ISOLATED MMSCC

Phase 1	$\mathbf{E}_1^{3:1}=\begin{bmatrix} -(2r_s+r_e) & 0 & 0 & 0 \\ 0 & 0 & (3r_s+2r_e) & R_{co} \\ 0 & 1 & 1 & 0 \\ 0 & 0 & R_{th} & -(R_{th}+R_{co}) \end{bmatrix}$	$\mathbf{F}_1^{3:1}=\begin{bmatrix} -1 & 0 & 0 & 0 \\ 0 & -1 & 1 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix}$	$\mathbf{G}_1^{3:1}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & R_{th} \end{bmatrix}$
Phase 2	$\mathbf{E}_2^{3:1}=\begin{bmatrix} 0 & (3r_s+2r_e) & 0 & R_{co} \\ 1 & 1 & 0 & 0 \\ 0 & 0 & -(3r_s+r_e) & R_{co} \\ 0 & R_{th} & -R_{th} & -(R_{th}+R_{co}) \end{bmatrix}$	$\mathbf{F}_2^{3:1}=\begin{bmatrix} -1 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix}$	$\mathbf{G}_2^{3:1}=\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & R_{th} \end{bmatrix}$
Deadtime	$\mathbf{E}_{dt}^{3:1}=(R_{th}+R_{co})$	$\mathbf{F}_{dt}^{3:1}=1$	$\mathbf{G}_{dt}^{3:1}=\begin{bmatrix} 0 & -1 & \dfrac{R_{co}}{R_{th}+R_{co}} \end{bmatrix}$

The MMSCC is designed to operate in or near the FSL, where the voltages are assumed to behave linearly. With the assumption of linear voltages the average voltage should occur in the middle of phase 1 or in phase 2. Under this assumption the chosen sampling time is in the middle of phase 1. Phase 1 is chosen over phase 2 since this is when the input voltage is connected to the MMSCC, thus allowing for a model of the average input current.

Sampling at the end of phase 1 or phase 2 yields accurate dynamics, but the choice to sample in the middle of phase 1 (or phase 2) provides a closer approximation of the average values during steady state. This can be seen by a comparison of step response of the output voltages of the dynamic models in Fig. 3.21 where the sampling time is chosen to be at the end of phase 1, end of phase 2, and in the middle of phase 1.

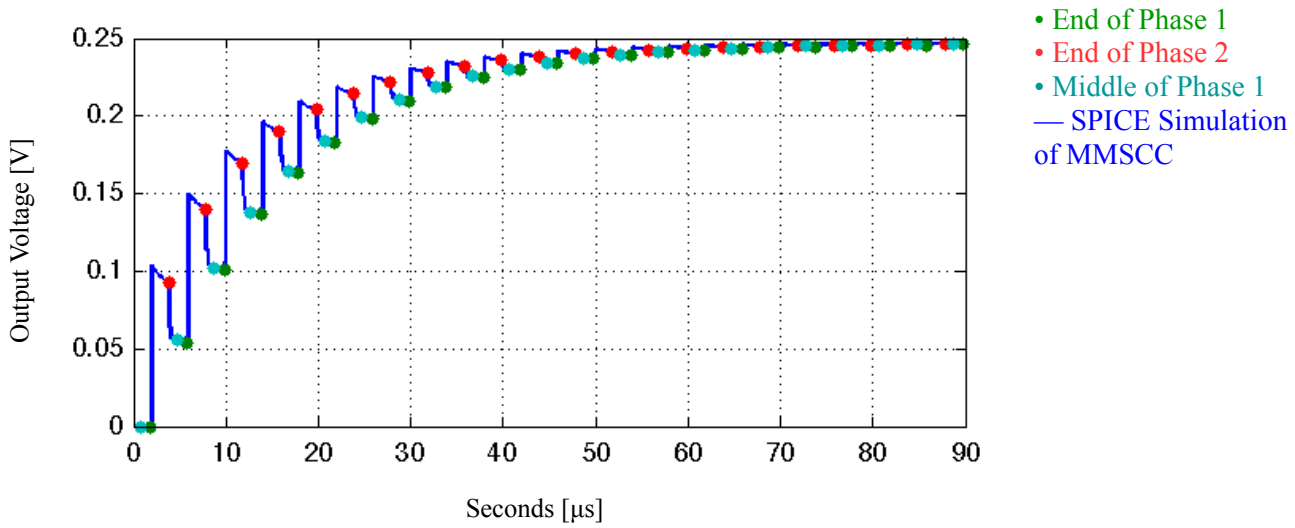


Fig. 3.21. Effect of sampling time (within a switching period) on the MMSCC Dynamic Model

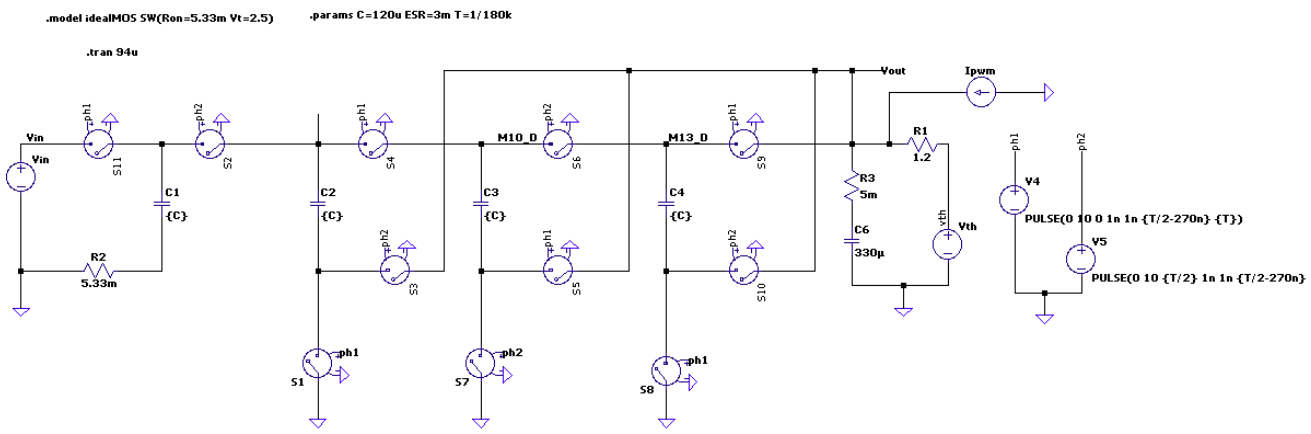
With the selection of Phase 1 for sampling the output **y** can be defined from the output matrices **P** and **Q** as shown in (3.40). The output matrices **P** and **Q** for each conversion ratio are shown in Appendix A.

$$\mathbf{y} = \mathbf{P}\,\mathbf{x} + \mathbf{Q}\,\mathbf{u} \tag{3.40}$$

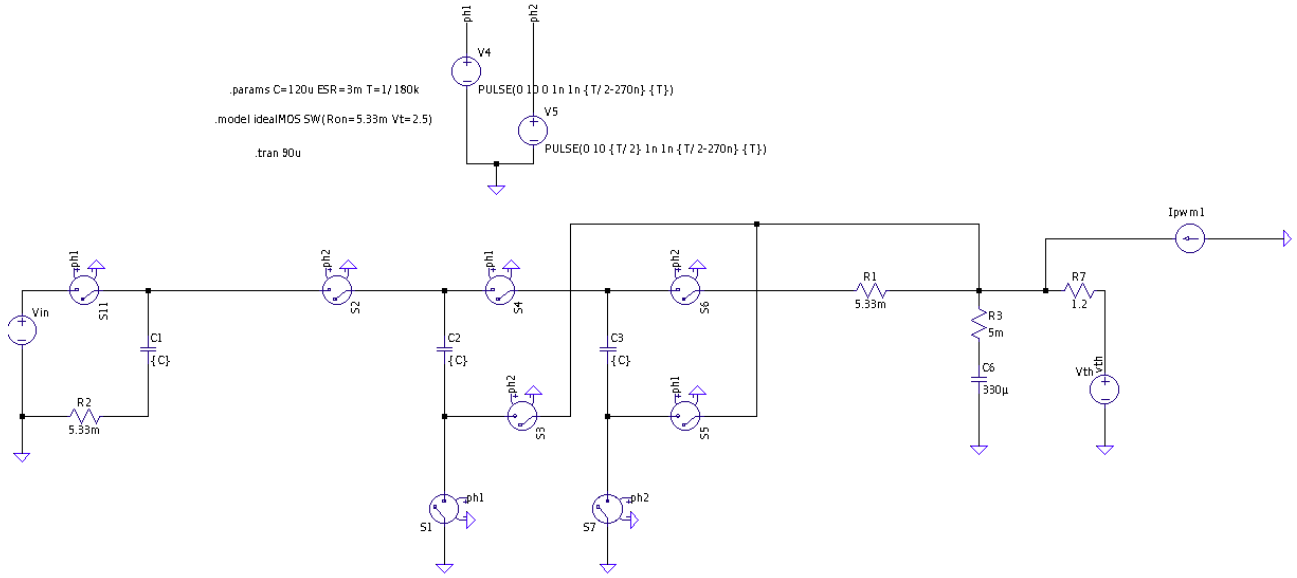
To verify the accuracy of this dynamic model, the model outputs (v_{out} and i_{in}) are compared to a switching SPICE model of the designed MMSCC performed in LTSpice. A step is applied to each system input: the input voltage v_{in}, the Thévenin equivalent load v_{th}, and the pwm current i_{pwm} in the middle of phase 1 to match the step response of the dynamic model. The parameters used for the SPICE simulation and the dynamic model are listed in Table 3.9. The switching models used in LTSpice for each operating mode 4:1, 3:1, and 2:1 are shown in Fig. 3.22(a)-(c). It is assumed that the MOSFETs share the same resistance assuming a temperature rise of 80º C. It is also assumed that each switching capacitor is 120µF. The duty ratios of phase 1, phase 2, and the dead time are notated as D_1, D_2, and D_{dt}.

TABLE 3.9: MMSCC PARAMETERS USED FOR SIMULATION AND DYNAMIC MODELING

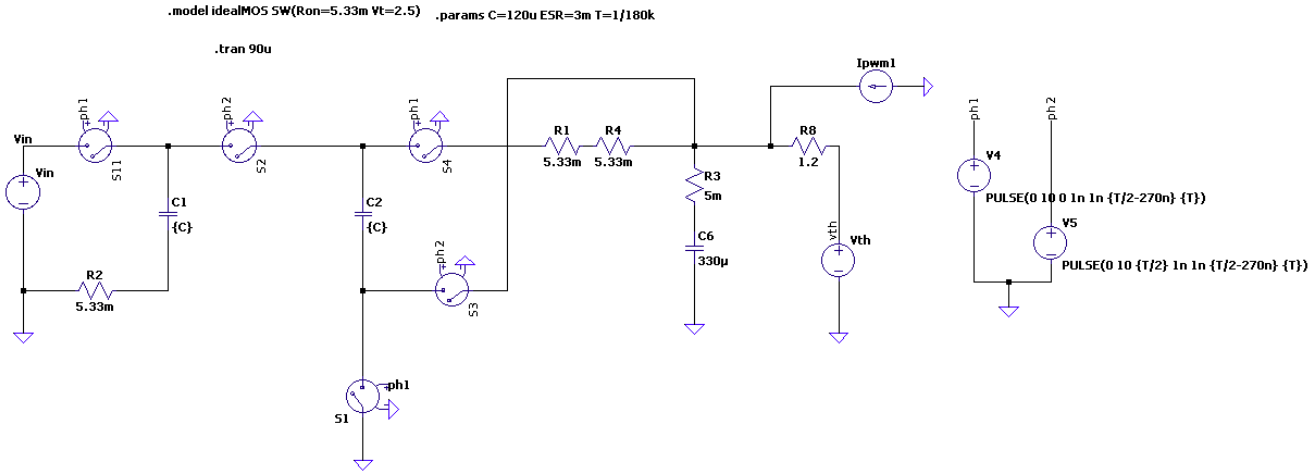
Parameter	Value	Parameter	Value	Parameter	Value
C_1	120µF	D_1	0.45	R_{ESR}	3mΩ
C_2	120µF	D_2	0.45	$R_{ESR\text{-}outputCap}$	5mΩ
C_3	120µF	D_{dt}	0.05	f_{SW}	180kHz
C_4	120µF	$R_{ds(on)@105^o}$	5.33mΩ		
C_{out}	330µF	R_{th}	1.2Ω		



(a) 4:1 MMSCC



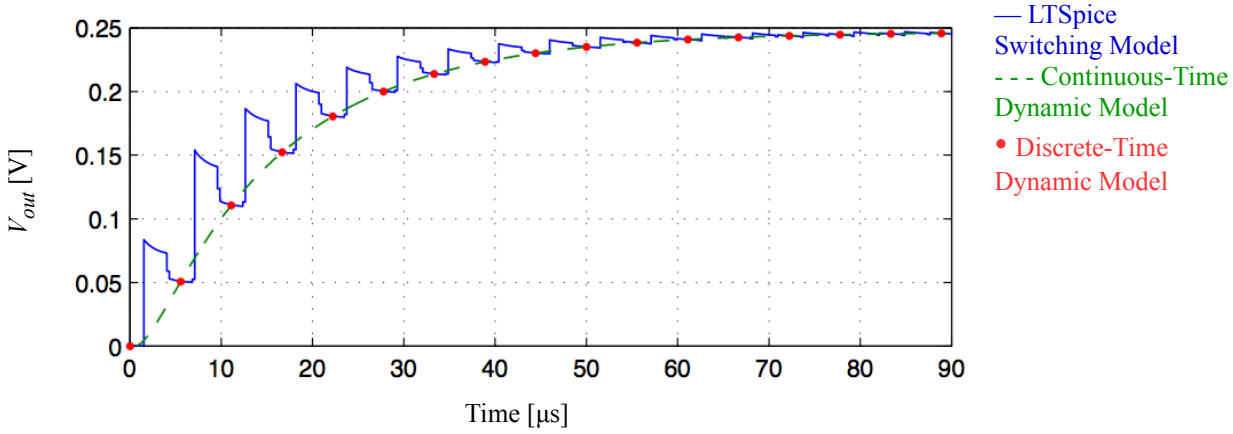
(b) 3:1 MMSCC



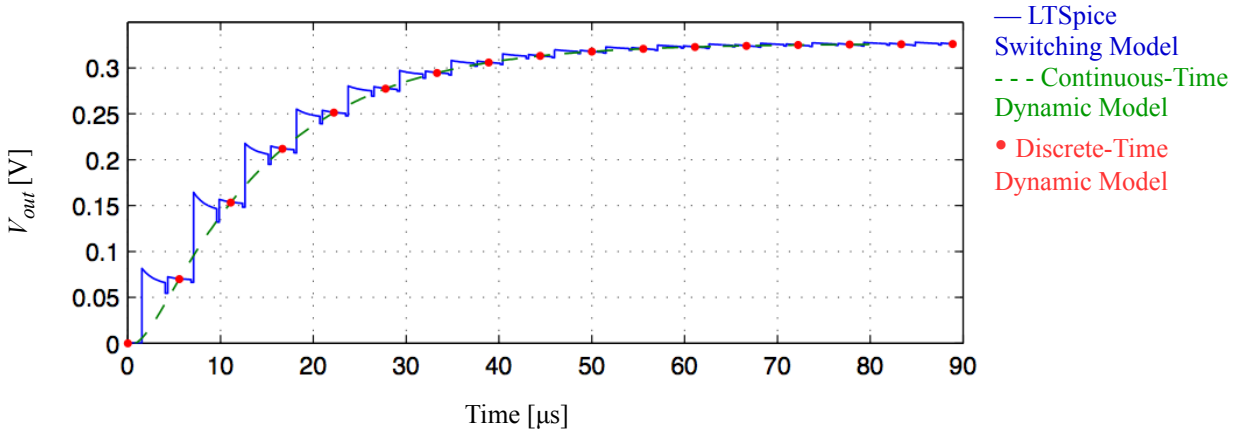
(c) 2:1 MMSCC

Fig. 3.22. The MMSCC SPICE models used in LTSpice for step responses.

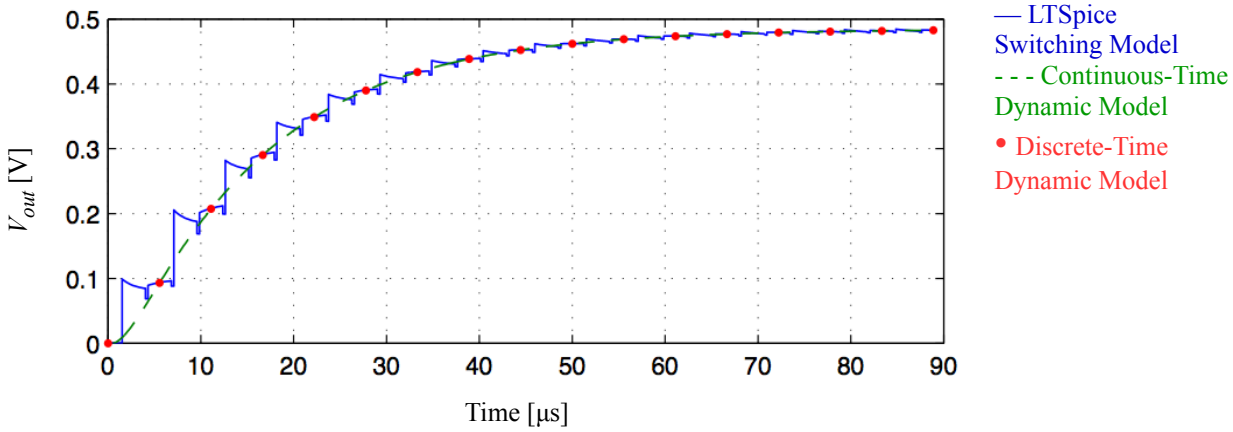
A comparison of the output voltage step response due to a step change in input voltage is shown in Fig. 3.23(a)-(c) for each operating mode. The step response of the dynamic model's output voltage due to the other model inputs, v_{th} and i_{pwm}, are shown in Fig. 3.24(a)-(c) for each operating mode. The comparisons show perfect agreement between the dynamic model generated via DSSA and the SPICE simulation from LTSpice. A continuous time model is also generated using the `d2c()` function in MATLAB and plotted along with the switching model and discrete time model in Fig. 3.23 and Fig. 3.24. The continuous time model will be used to generate an approximate small-signal circuit model of the MMSCC in section 3.2.3.



(a) 4:1

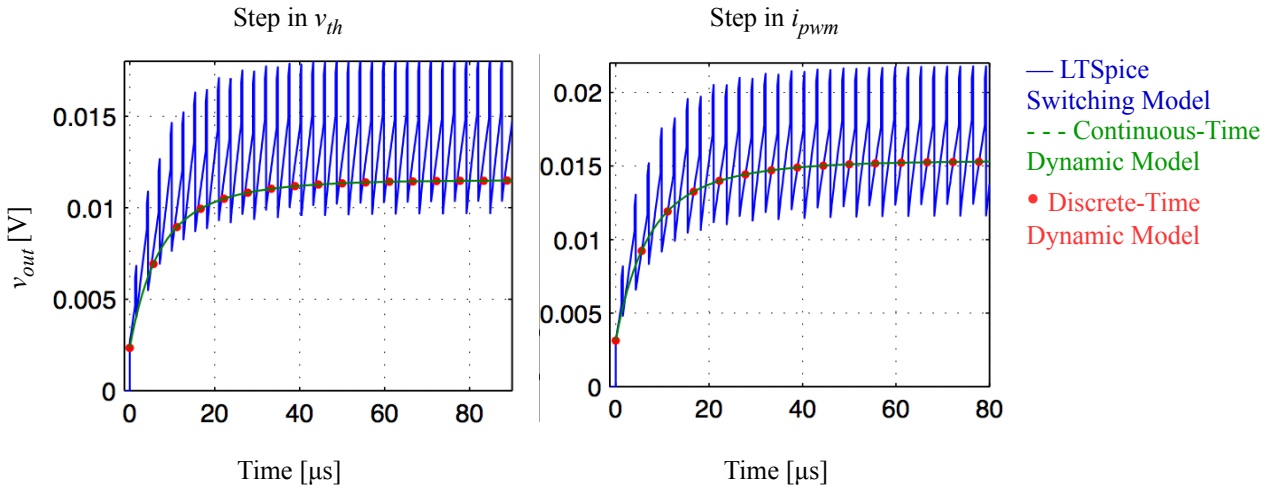


(b) 3:1

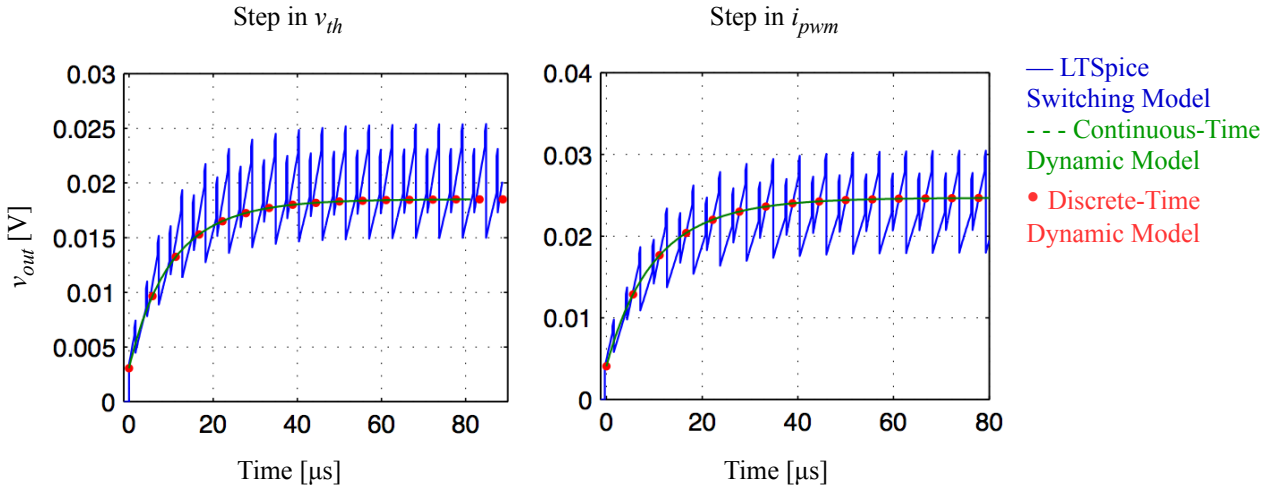


(c) 2:1

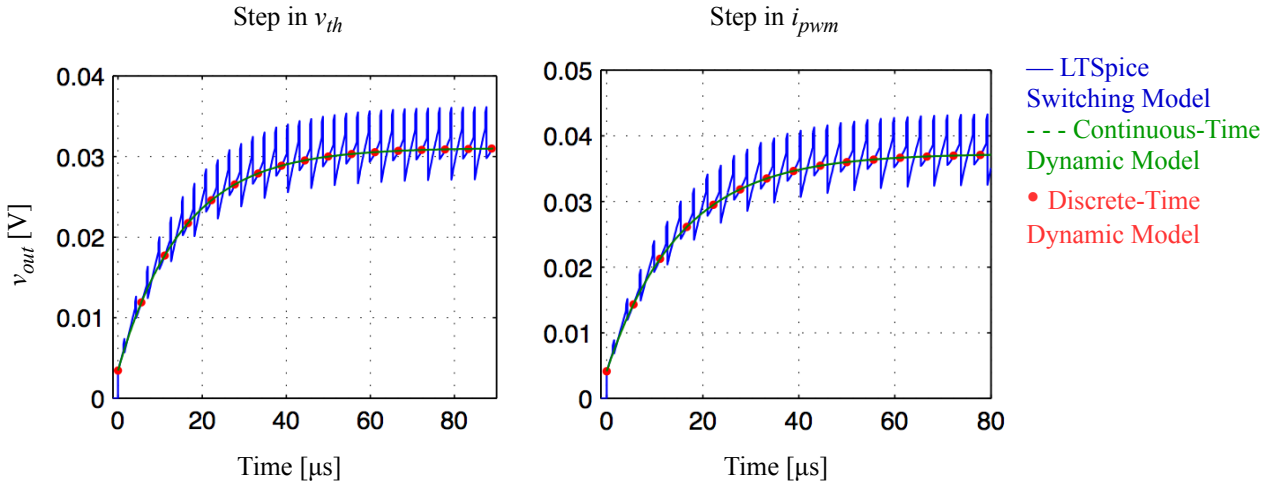
Fig. 3.23. Comparison of the output voltage step response of the DSSA Dynamic Model and the LTSpice simulation of the MMSCC in each mode to a step in the input voltage.



(a) 4:1 Operation



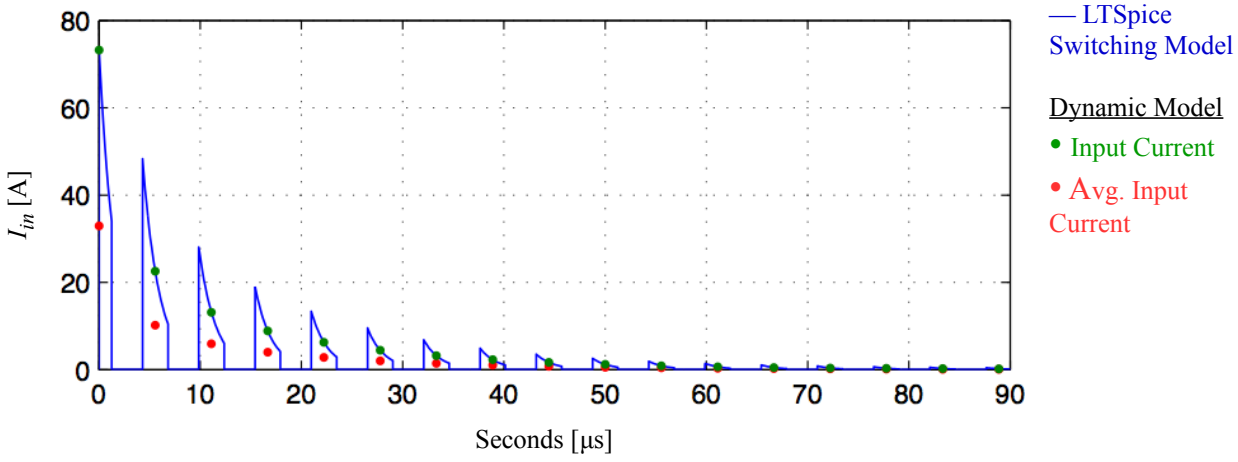
(b) 3:1 Operation



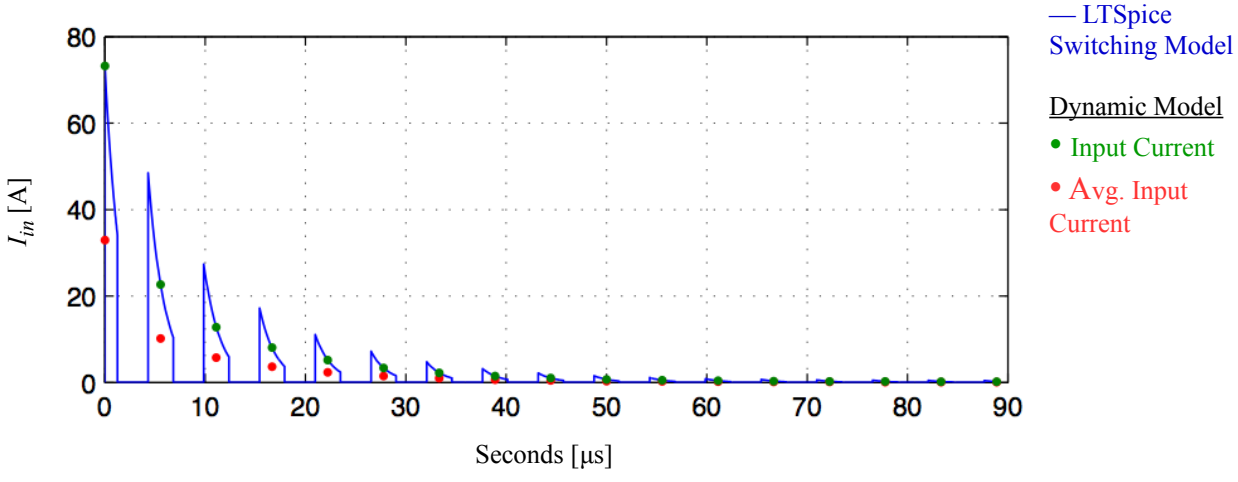
(c) 2:1 Operation

Fig. 3.24. Comparison of the output voltage response of the DSSA Dynamic Model and the LTSpice simulation of the MMSCC in each operating mode to a step in v_{th} and i_{pwm}

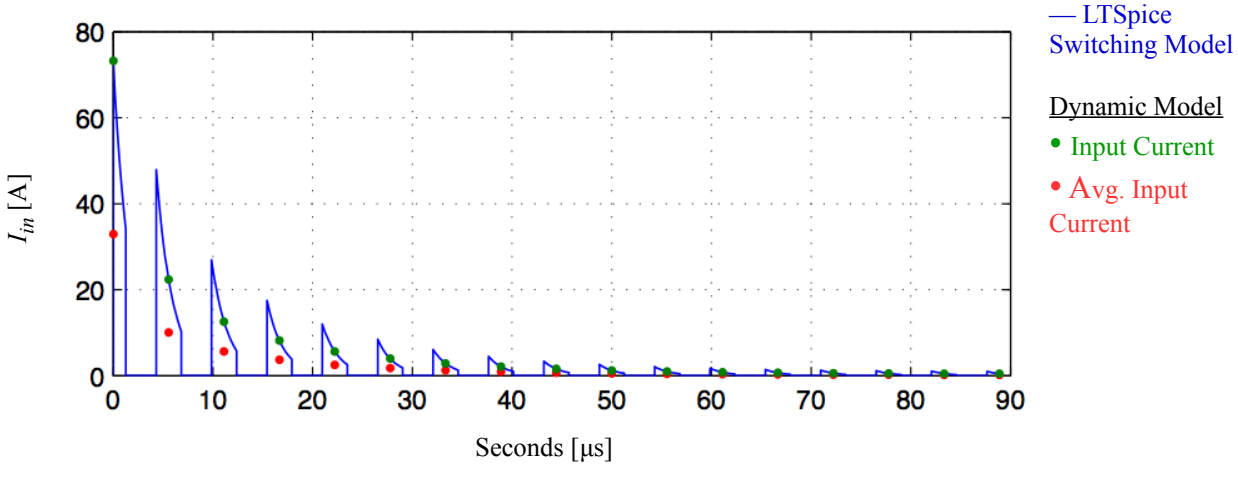
The model accuracy can also be verified by comparing the other models output, the input current, to the LTSpice simulation of the MMSCC. The dynamic model's input current and the average input current step responses due to a step in input voltage are compared to the input current waveform of the LTSpice simulation in Fig. 3.25(a)-(c) for each operating mode. The dynamic models sampled input current is shown to be in agreement with the LTSpice simulation. As long as the input current of the dynamic model approximates the average value of the input current during phase 1 (when the input current is nonzero) then the average input current is also accurate. The step response of the dynamic model's input current due to a step in the other model inputs, v_{th} and i_{pwm}, are also in good agreement with the LTSpice simulations. A plot of these step responses are shown in Appendix B.



(a) 4:1



(b) 3:1



(c) 2:1

Fig. 3.25. Comparison of the input current step response of the DSSA Dynamic Model and the LTSpice simulation of the MMSCC in each operating mode due to a step in the input voltage.

With the dynamic model verified, our analysis of the input to output voltage, input impedance, and output impedance can now proceed. The magnitude and phase of the input to output voltage transfer function are plotted in Fig. 3.26. As expected (see [29]) the input to output voltage dynamics appear similar to that of a first order system despite being a 5th order model. Approximating the input to output voltage transfer function as first order gives the poles (dominate eigenvalue) of 61.3 krad/s, 79.2 krad/s, and 64.8 krad/s for each operating mode. The DC gains of the input to output voltage are not the ideal 4:1, 3:1, and 2:1, this is due to the output load being modeled as a Thévenin equivalent load. Evaluation of the input to output voltage transfer functions has $v_{th} = 0$, thus the MMSCC is being modeled at full load. DC values of the output voltage include the conduction losses of the equivalent output impedance at full load i.e. $Z_o*(V_o/R_{th})$. The DC gains of the output voltage (Fig. 3.26) are 0.247, 0.327, and 0.485 for 4:1, 3:1, and 2:1 which are close to the expected ideal gains.

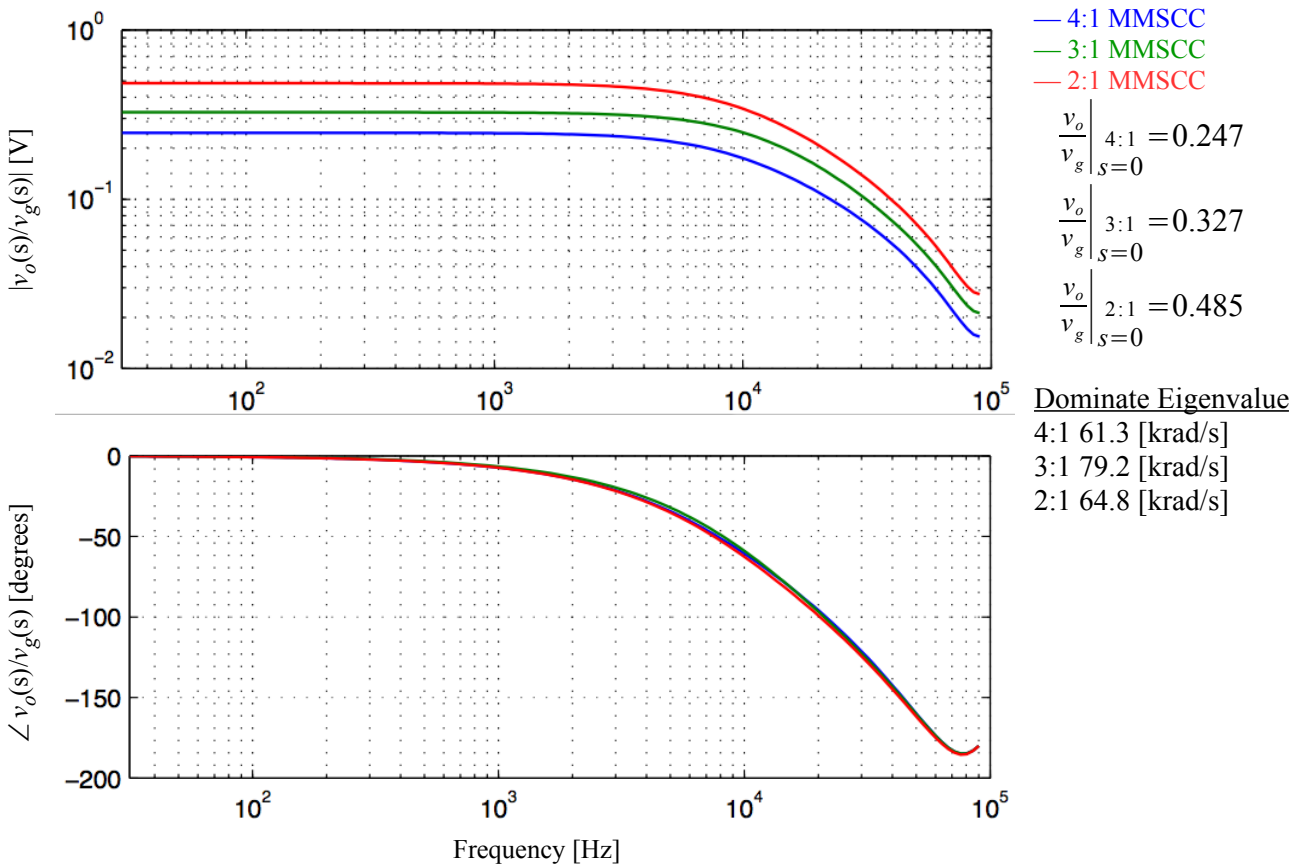


Fig. 3.26. Frequency response of the line-to-output voltage transfer function of the MMSCC for each operating mode is similar to the frequency response of a first order system.

The frequency response of the output impedance is plotted in Fig. 3.27. The expected DC output impedance calculated from (3.31) are 16.4mΩ, 23.0mΩ, and 37.9mΩ for the MMSCC operating in

4:1, 3:1, and 2:1. The output impedances in Fig. 3.27 are 15.5mΩ, 25.15mΩ, and 38.47mΩ which are in good agreement with the calculated approximate output impedances. The output impedance of the 4:1 and 3:1 are similar in terms of the shape of the curve but include a larger second order component, only offset by differing DC values. Using MATLAB function `balred()`, the approximate second order output impedance transfer functions for 4:1 operation has poles at 63.1 krad/s and 183.7 krad/s and most importantly a zero at 82.6 krad/s. The 3:1 second order approximate output impedance has poles at 80.2 krad/s and 172 krad/s with one of the zeros at 128 krad/s. This implies that the dominate eigenvalue from the input to output voltage transfer functions is still present, but is being effectively canceled out in the output impedance transfer functions by a nearby zero. Approximating the output impedance as a first order system, the poles are 104 krad/s and 92.6 krad/s for 4:1 and 3:1 operation compared to the 61.3 krad/s and 79.2 krad/s poles in the input to output voltage transfer functions. This difference in first order approximation poles for 4:1 operation is significant enough to be deemed unacceptable. This leads to poor agreement with the first order model proposed in [29] where a single dominate pole appeared in both the input to output voltage and output impedance transfer functions.

Unlike operation in 4:1 or 3:1 the output impedance in 2:1 operation is approximated very well by a first order model with a pole occurring at 64.8 krad/s. This pole is identical to the one seen in the 2:1 input to output voltage transfer function. It appears that as the operating mode moves from 4:1 to 3:1 to 2:1 the output impedance becomes more like a first order system and the pole in the first order approximated transfer function approaches the one seen in the input to output voltage transfer function.

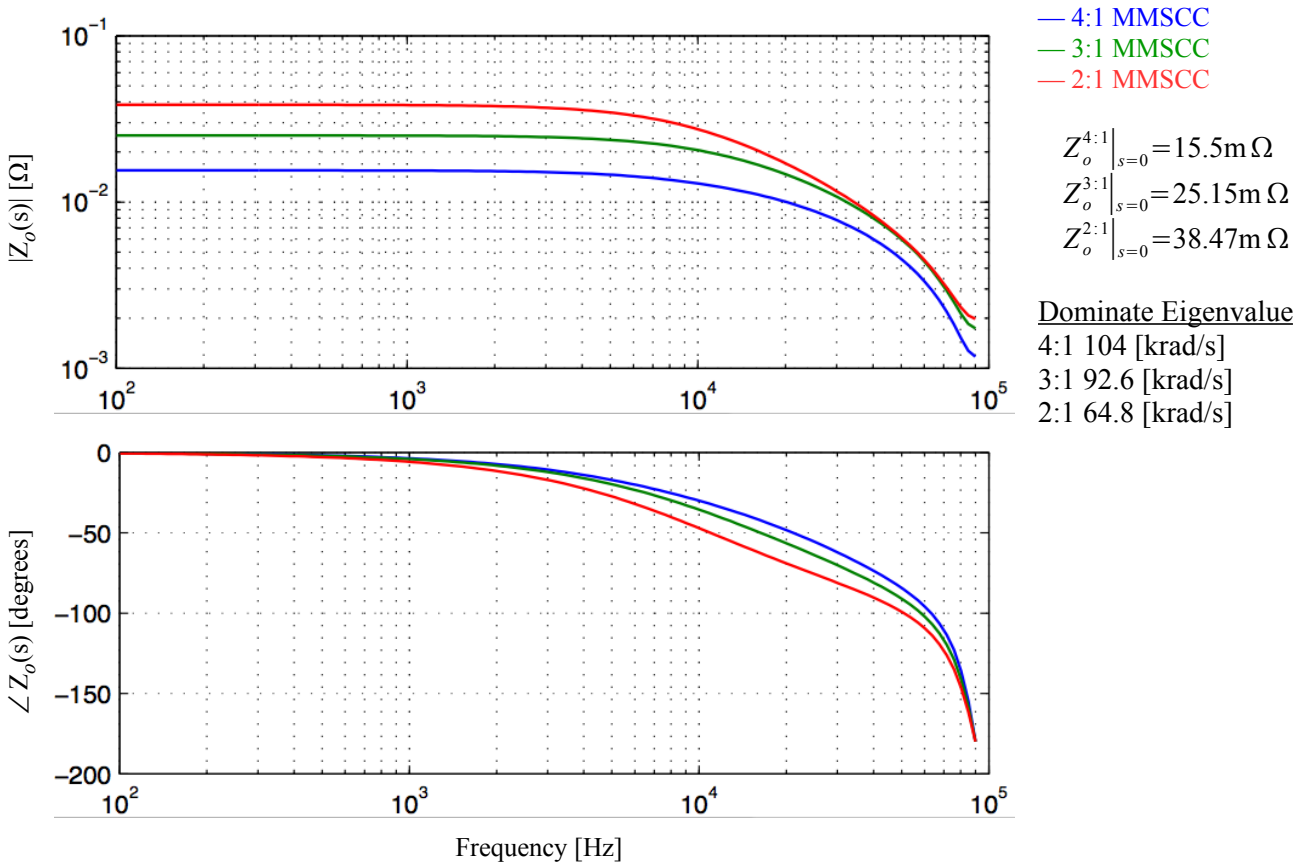


Fig. 3.27. Frequency response of the output impedance of the MMSCC for each operating mode

At steady state the MMSCC can be modeled as a DC transformer (with a turns ratio of 4:1, 3:1, and 2:1 depending on the mode of operation) and a series output impedance. The input impedance at steady state would then be the output impedance and load impedance seen from the input. The DC input impedance can then be calculated from the calculated output impedance added with the load resistance giving 19.5Ω, 11Ω, and 4.95Ω for the MMSCC operating in 4:1, 3:1, and 2:1. The calculated values are approximate but agree well with the DC input impedances 21.4Ω, 12.1Ω, and 5.5Ω seen in Fig. 3.28.

Recall that an output variable of the model is actually the input current and thus it is the input admittance that will share the systems eigenvalues (i.e. will share the same dominate eigenvalue as the input to output transfer function). The input impedance will then have the system eigenvalues as zeros.

The plot of the input impedance magnitude in Fig. 3.28 reveals it to be suitably approximated as first order. The first order pole does change significantly as the operation mode changes from 4:1 to 3:1 to 2:1. The pole can be allowed to vary but it is the input impedance zero (the system dominate eigenvalue) that must remain constant in the first order approximation if an accurate reduced-order model is to be generated. Inspection of phase plot of the input impedance in Fig. 3.28 indicates a

constant zero, using MATLAB function `balred()` the approximate zeros are 76.6 krad/s, 95.7 krad/s, and 85.6 krad/s for 4:1, 3:1, and 2:1 operation. These approximate zeros are reasonably close the dominate poles seen in the first order approximations of the input to output voltage transfer functions.

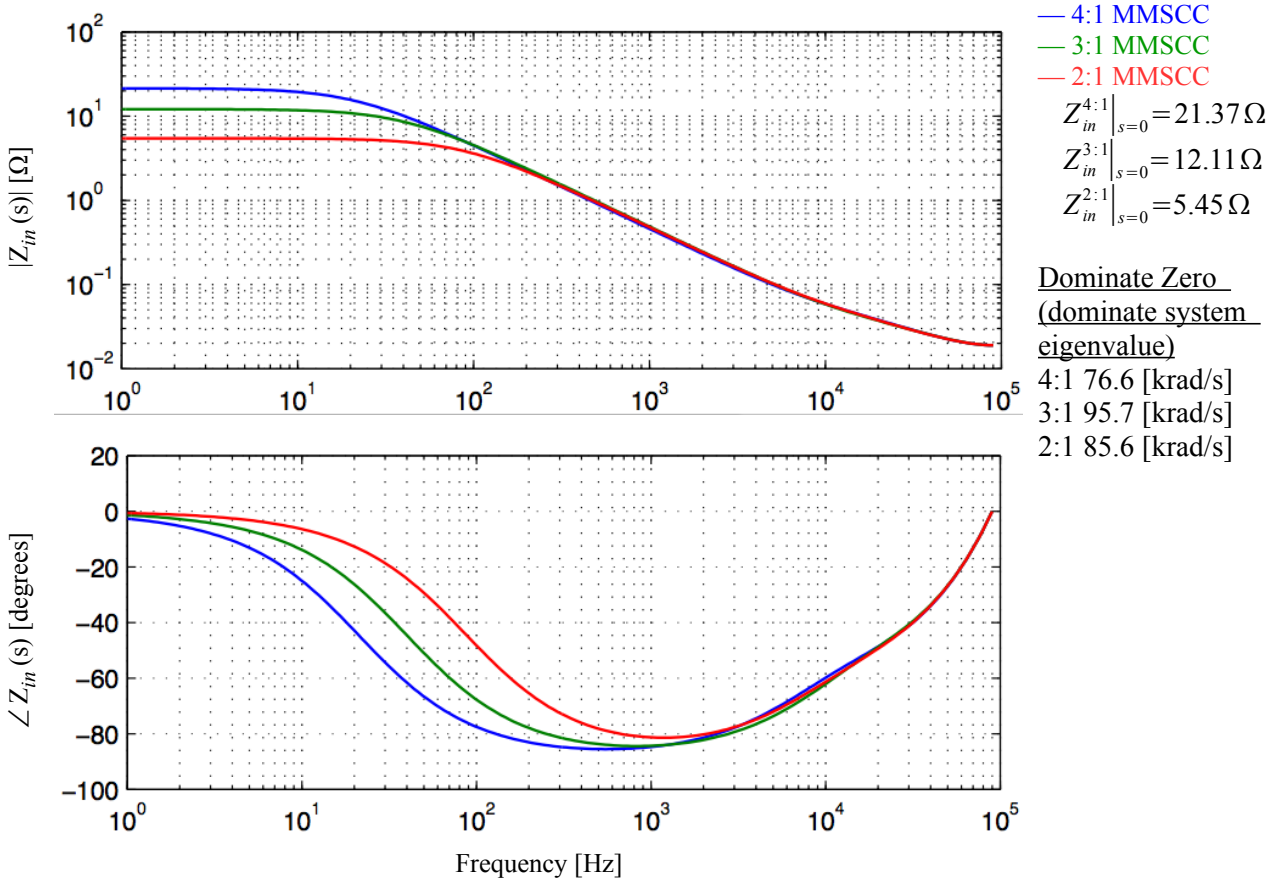


Fig. 3.28. Frequency response of the input impedance of the MMSCC for each operating mode

In summary, the isolated MMSCC has been dynamically modeled through DSSA for each operating mode. The model outputs, output voltage and input current, have been verified to be accurate by comparison to a SPICE simulation. Frequency response analysis has been done on the input to output transfer function, output impedance, and input impedance in preparation of obtaining a reduced-order model. Analysis reveals that the input impedance and the input to output voltage characteristics should be well suited for first order approximation by the systems dominate eigenvalue regardless of the operating mode (4:1, 3:1, and 2:1). The output impedance can be approximated with the system dominate eigenvalue in 2:1 operation, with less accuracy in 3:1 operation, and very poorly in 4:1 operation.

3.2.2 Reduced Order Dynamic Model of the Isolated MMSCC and Derivation of a Circuit Model

In most applications the I/O behavior of a converter is the primary interest, not the internal dynamics such as the voltages on each switching capacitor. Switched-capacitor converters, assuming low parasitic inductances, are a network of capacitors and resistors resulting in all real eigenvalues [29]. As shown in Fig. 3.26 the dynamics of the MMSCC is dominated by a single eigenvalue and appears to be first order in nature. As discussed in section 2.1.2, a continuous time (CT) reduced order model can be made for the MMSCC using the DC gains and the dominate eigenvalue [29]. The motivation for a CT reduced-order model (ROM) is not to reduce computation time or complexity, but to generate a simplified small-signal circuit model that can be used in SPICE simulations and for small-signal analysis of the QPRSCC.

The first step in generating a circuit model is to find the approximate ROM. The ROM generated in [29] ignores zeros that may be in the output impedance transfer function or input admittance. The output impedance is a bi-proper transfer function with equal order numerator and denominator (3.41), unlike the line to output voltage and current transfer functions which are proper (higher order denominator). The addition of a continuous time zero, ζ, to the reduced order output impedance transfer function adds little complexity and better represents the response of the MMSCC due to changes in load currents. The required zero, ζ, can be calculated so that the ROM has the same DC gain when using the high frequency gain, k, from the zero-pole-gain model and the dominate eigenvalue of the system.

$$Z_o(s)=\begin{cases}\dfrac{0.0031(z+1.523)(z-0.648)(z-0.187)(z-0.103)(z-0.048)}{(z-0.711)(z-0.388)(z-0.185)(z-0.082)(z-0.046)} & when\ 4:1\\ \dfrac{0.004(z+1.64)(z-0.514)(z-0.125)(z-0.064)}{(z-0.644)(z-0.415)(z-0.125)(z-0.05)} & when\ 3:1\\ \dfrac{0.004(z-0.3441)(z-0.06867)(z+1.778)}{(z-0.6978)(z-0.341)(z-0.05533)} & when\ 2:1\end{cases} \quad (3.41)$$

The high frequency gain can easily be found by inspection of the zero-pole-gain form of the bi-proper transfer functions. The zero-pole-gain form can be found with the `zpk()` command in MATLAB. The dominate eigenvalue, λ, of a discrete time system is the one closest to the unit circle. The eigenvalues of the system are the poles seen in (3.41). The dominate eigenvalue for operating mode is $\lambda_{4:1} = 0.711$,

$\lambda_{3:1}$ = 0.644, and $\lambda_{2:1}$ = 0.6978. The bi-proper transfer functions of interest are the input admittance and the output impedance. The DC gains are (3.42), where the element α_{ij} of the matrix $\boldsymbol{\alpha}^{\mathbf{n:1}}$ .is the DC gain from the *j-th* input to the *i-th* output.

$$Y_{DC}=\begin{bmatrix} I_{in} \\ V_o \end{bmatrix}=\boldsymbol{\alpha}^{\boldsymbol{n:1}}=\begin{cases} \begin{bmatrix} 0.0467 & -0.1869 & -0.2243 \\ 0.2468 & 0.0128 & 0.0153 \end{bmatrix} & when\ 4:1 \\ \begin{bmatrix} 0.0826 & -0.2477 & -0.2972 \\ 0.3265 & 0.0205 & 0.0246 \end{bmatrix} & when\ 3:1 \\ \begin{bmatrix} 0.1835 & -0.3670 & -0.4403 \\ 0.4845 & 0.0311 & 0.0373 \end{bmatrix} & when\ 2:1 \end{cases} \tag{3.42}$$

The needed CT zero for the CT reduced model of the bi-proper transfer functions from input *i* to output *j* can be calculated by (3.43), where T_s is the switching period.

$$\zeta_{ij}^{n:1}=\ln\left(\frac{\lambda_{n:1}}{T_s}\right)\frac{\alpha_{ij}^{n:1}}{k_{ij}} \tag{3.43}$$

The ROM can then be generated for the input current and the output voltage, (3.44) and (3.45) respectively, where $a=-\ln\left(\frac{\lambda_{n:1}}{T_s}\right)$.

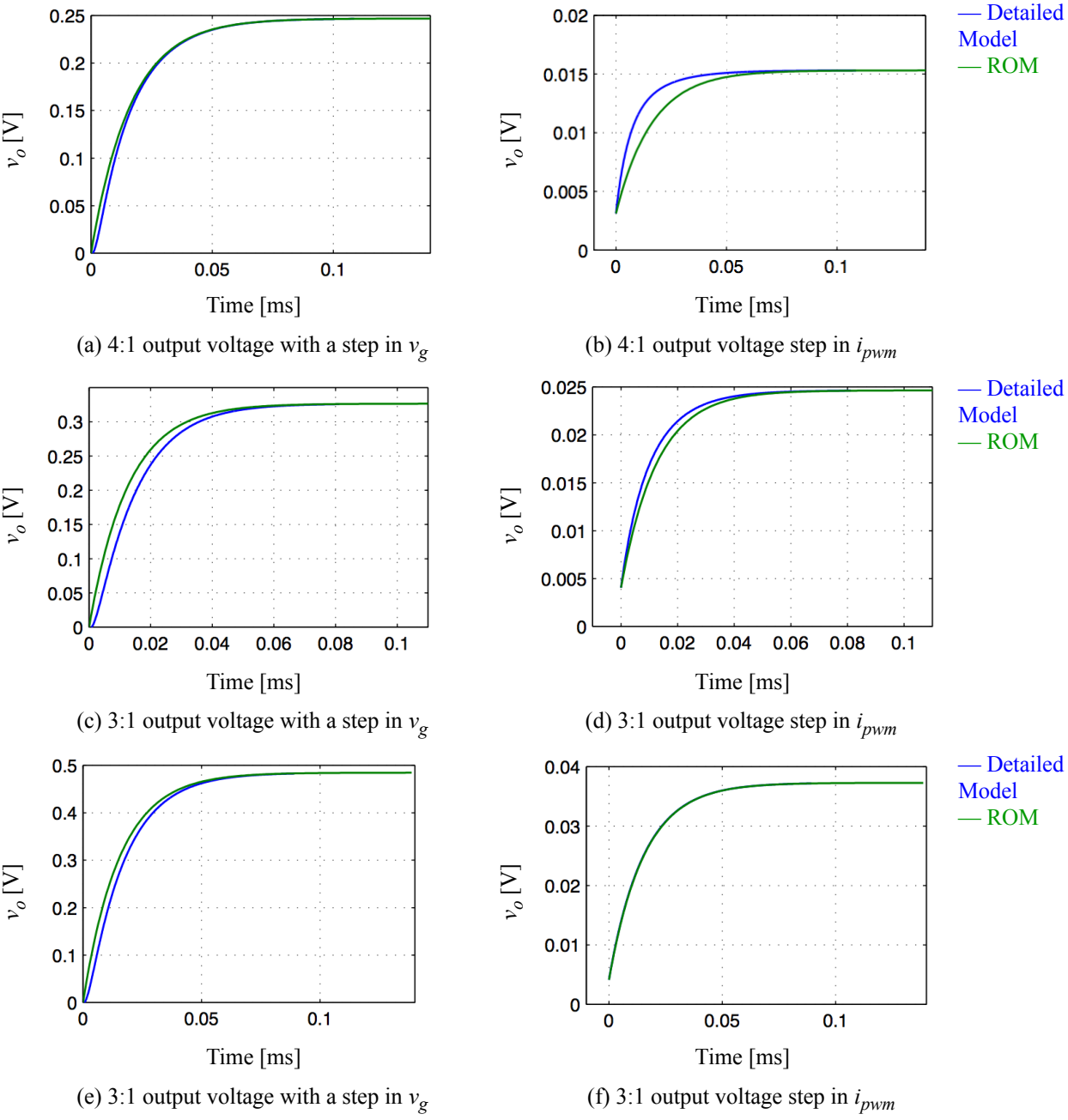
$$i_{in}(s)\approx\frac{k_{11}\left(s+\zeta_{11}^{n:1}\right)}{s+a}v_g(s)+\frac{\alpha_{12}a}{s+a}v_{th}(s)+\frac{\alpha_{13}a}{s+a}i_{pwm}(s) \tag{3.44}$$

$$v_o(s)\approx\frac{\alpha_{21}a}{s+a}v_g(s)+\frac{k_{22}\left(s+\zeta_{22}^{n:1}\right)}{s+a}v_{th}(s)+\frac{k_{23}\left(s+\zeta_{23}^{n:1}\right)}{s+a}i_{pwm}(s) \tag{3.45}$$

The reduced-order models can be compared to detailed (full order) models by step response and frequency response plots. The output voltages are best evaluated with a plot of the step response. The output impedance and the input admittance are better suited for evaluation with frequency response plots.

The ROM of the output voltage is best compared using the step response to the various inputs. A comparison of the detailed and reduced order repose to a step in the input voltage reveals good agreement as shown in Fig. 3.29(a,c,e) for 4:1, 3:1, and 2:1 operation. There is some error in the initial response but the overall dynamics of the response is accurately modeled by the ROM. A comparison of the models response to a step change in the load current, in this case due a change in the H-Bridge

current i_{pwm}, is made in Fig. 3.29(b,d,f) for 4:1, 3:1, and 2:1 operation. From Fig. 3.29(b), for 4:1 operation, it appears that the ROM does not accurately model the dynamics of the output voltage step response. By design, the reduced order does accurately model steady state and the initial response (at time zero). For 3:1 and 2:1 operation the ROM does well in capturing the dynamics of the response seen in Fig. 3.29(d) and Fig. 3.29(f).



(a) 4:1 output voltage with a step in v_g

(b) 4:1 output voltage step in i_{pwm}

(c) 3:1 output voltage with a step in v_g

(d) 3:1 output voltage step in i_{pwm}

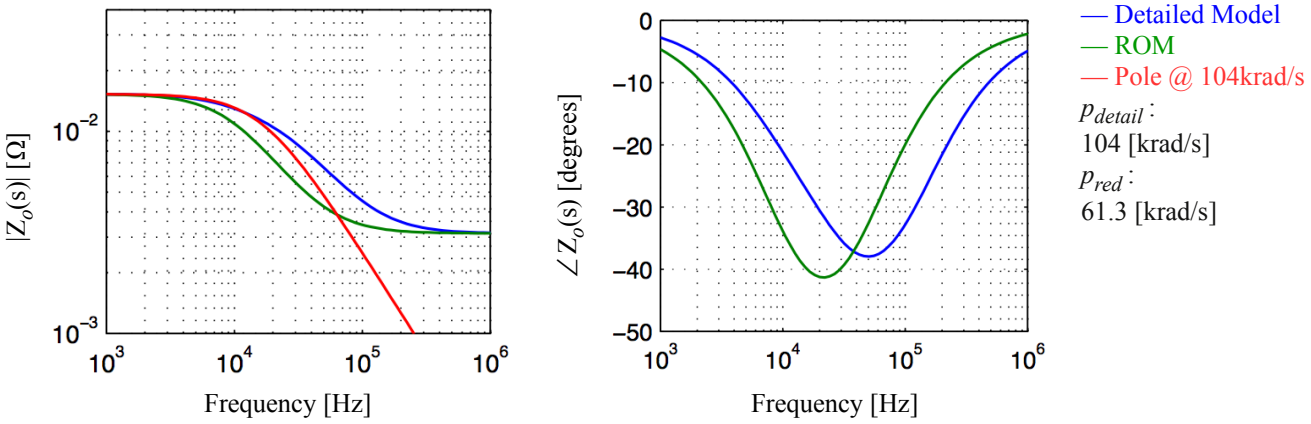
(e) 3:1 output voltage with a step in v_g

(f) 3:1 output voltage step in i_{pwm}

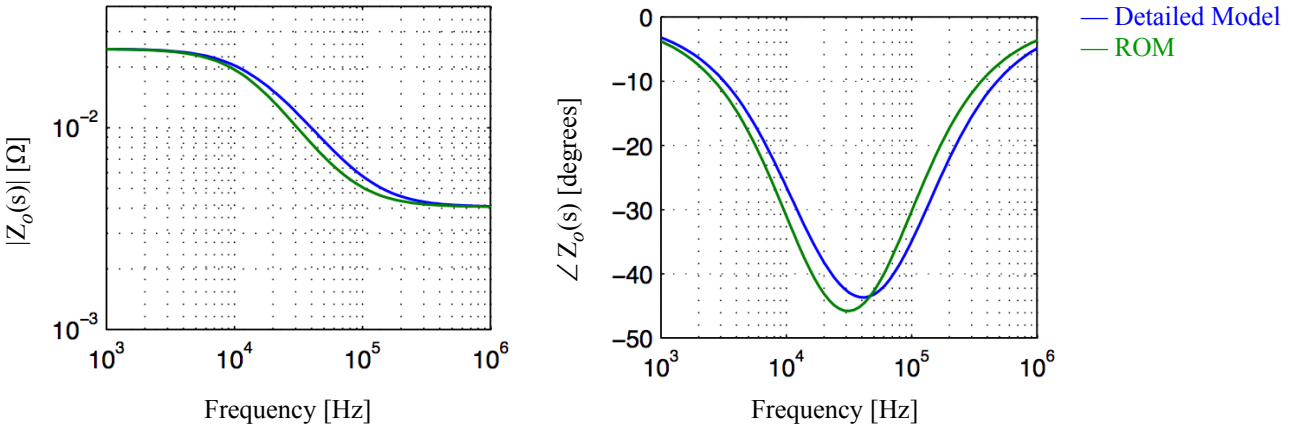
Fig. 3.29. Comparison of the responses of the 4:1, 3:1, and 2:1 MMSCC detailed and ROM to a step in (a,c,e) input voltage and (b,d,f) H-Bridge current i_{pwm}.

The ROM's poor estimation of the output voltage response to a step in load current is illustrated by analysis of its output impedance frequency response plotted in Fig. 3.30. For 4:1 operation, shown in Fig. 3.30(a), the DC output impedance and high frequency output impedances agree perfectly but the ROM's pole occurs at a too low frequency. Approximating the detailed model's output impedance as a first order system gives a pole of p_{des}=104krad/s as shown by the red line in the magnitude plot of Fig. 3.30(a). This pole is more than twice the eigenvalue a=61.3krad/s used for the ROM. The shape of the detailed model's output impedance is first order but has a different dominating eigenvalue than the input to output voltage transfer function. As the MMSCC operates from a 3:1 to 2:1 the ROM output impedance becomes a better approximation of the detailed model's output impedance (Fig. 3.30(b,c)). In fact at operation of 2:1 the reduced order output model is nearly a perfect approximation of the detailed model.

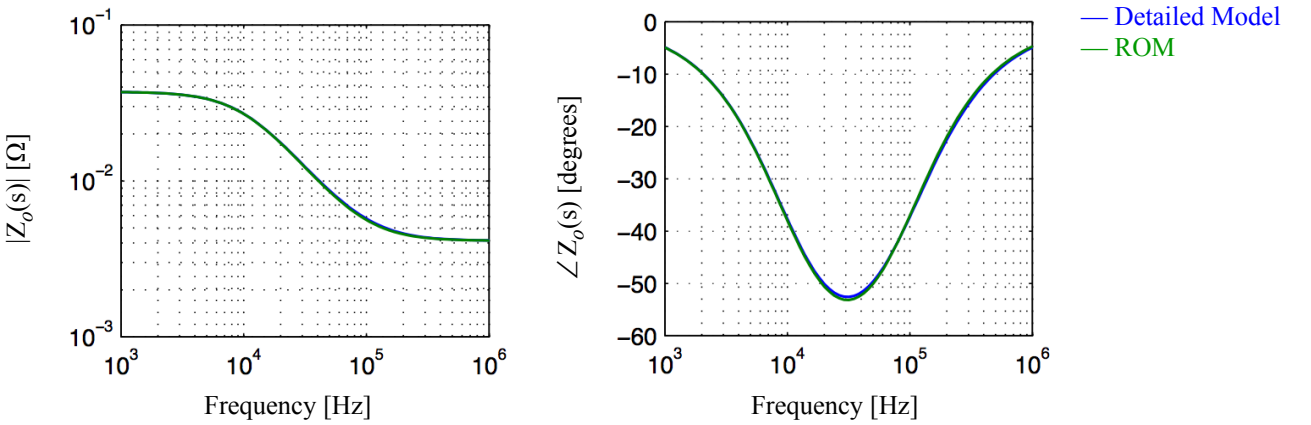
Overall the ROM does an accurate job portraying the output voltage dynamics of the isolated MMSCC to changes in the input voltage and load current. The ROM is inaccurate in its description of the output impedance in 4:1 operation as seen by the frequency response plot in Fig. 3.30(a), but not so in 3:1 or 2:1 operation. In order to account for the differences, a second order system would be needed to model the MMSCC. The main motivation for using the first order model is to generate a simplified small-signal equivalent circuit model for the isolated MMSCC. Due to time constraints, the first order approximation of the output voltage dynamics is accepted allowing for the generation of a small-signal equivalent circuit model for the isolated MMSCC from the ROM.



(a) 4:1 Output Impedance Frequency Response



(b) 3:1 Output Impedance Frequency Response



(c) 2:1 Output Impedance Frequency Response

Fig. 3.30. Comparison of the detailed model and ROM frequency response of the MMSCC output impedance for (a) 4:1, (b) 3:1, and (c) 2:1 operation

With the ROM accepted as a reasonable approximation of the isolated MMSCC output voltage, an appropriate circuit model of the ROM can be generated. The basis of the model is the steady-state model of DC transformer with turns ratio n:1 and a series output impedance R_o. To model the input to

output voltage transient behavior a capacitor C_1 is needed on the output side to form a RC low pass circuit. The time constant τ_1 represents the dominant eigenvalue of the input to output voltage transfer function. For example the 4:1 MMSCC ROM has the continuous time eigenvalue λ_1=61.3krad/s, thus $\tau_1 = 1/\lambda_1$. In order to model the dynamics of the output impedance there needs to be a zero in the output impedance transfer function and a different high frequency gain. This can be done with a T-circuit, a series resistance, parallel capacitor, and followed by a series resistance. This gives the circuit model shown in Fig. 3.31 where the resistances R_1 and R_2 and the capacitance C_1 can be found using (3.46), (3.47), and (3.48). The continuous time eigenvalue λ_1 refers to the dominating eigenvalue for the input to output voltage transfer function. The gain k refers to the high frequency gain of the output impedance.

$$R_2 = \frac{R_{th} k}{R_{th} - k} \approx k \tag{3.46}$$

$$R_1 = R_o - R_2 \tag{3.47}$$

$$C_1 = \frac{1}{\lambda_1 R_1} \tag{3.48}$$

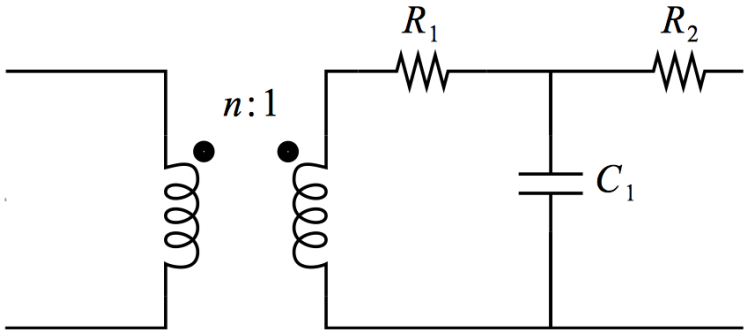


Fig. 3.31. Averaged small-signal circuit model of the output voltage dynamic behavior

The last step in generating the small-signal equivalent circuit model is to replicate the input impedance of the detailed model. Like the output voltage, the input current has been modeled by the ROM with the eigenvalue λ_1 as its pole. The reduced-order input admittance, the transfer function of a change in input current due to a change in input current, will have λ_1 as its pole and thus the input impedance will see λ_1 as a zero. If the Thévenin equivalent load is added to the output of the circuit in Fig. 3.31 as with the dynamic model then with v_{th} = 0 the input impedance is written as (3.49). The steady state input

impedance is the output impedance and R_{th} reflected to the input side of the transformer and the λ_1 appears as a zero.

$$Z_{in}(s)=n^2\left(\frac{(R_1+R_2+R_{th})(s\,R_1\,\mathrm{II}\,(R_2+Rth)+1)}{s\,C_1\,R_2+1}\right)\approx\left(\frac{n^2(R_1+R_2+R_{th})(s\,R_1+1)}{s\,C_1\,R_2+1}\right) \qquad (3.49)$$

Plotting the frequency response of the circuit model's input impedance (3.49) and the full order dynamic model for 4:1 operation in Fig. 3.32 reveals that the circuit model does a poor job modeling the input impedance. Although the pole for the circuit model does occur later than desired that will be addressed later. Of more importance is the error in the high frequency value of the impedance for the circuit model. At high frequencies, the capacitor C_1 of the circuit model in Fig. 3.31 is a short and the input impedance is modeled as $n^2\,R_1$.

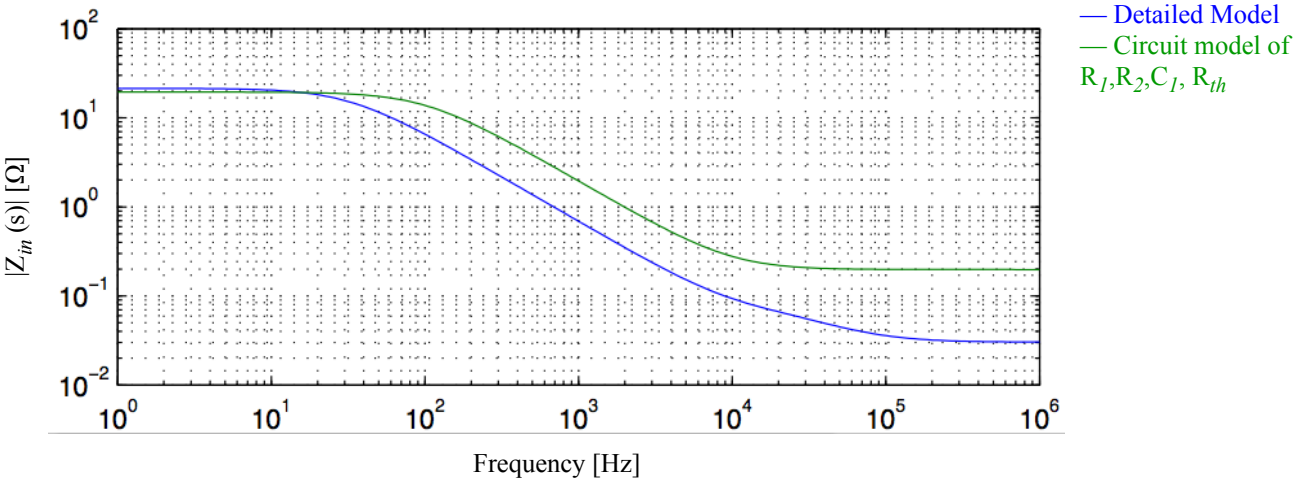


Fig. 3.32. Input impedance frequency response of the averaged small-signal circuit model and the detailed model for 4:1 operation.

Inspection of the isolated MMSCC schematic reveals that the input impedance is the voltage seen due to a current into the first capacitor through two switches and the capacitor's ESR. At higher frequencies the capacitor is a short and only the switch's resistance and ESR remain. Thus to rectify the high frequency error in the input impedance a resistance R_3 and capacitor C_2 can be added in parallel, with the input as shown in Fig. 3.33. This addition does not change the input to output voltage or output impedance transfer function. At high frequencies the input impedance of the circuit model is $n^2\,R_1\,\mathrm{II}\,R_3$ providing a degree of freedom with R_3 to set the high frequency input impedance. Further the addition of the capacitor C_2 prevents a change to the DC input impedance and allows for a second order approximation.

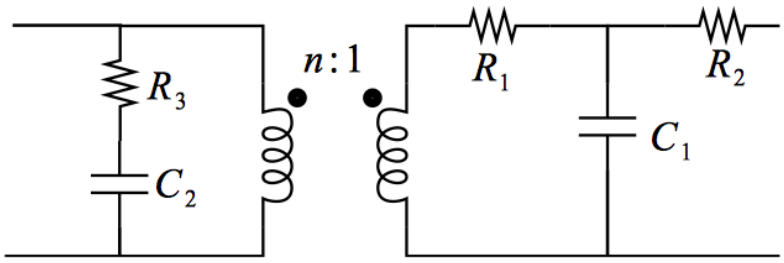


Fig. 3.33. Completed averaged small-signal circuit model of the MMSCC

The resistance R_3 can be calculated as in (3.50), where k_{in} is the high frequency gain of the input impedance. The gain k_{in} can be found by inspection of the input impedance transfer function in zero-pole-gain form which is easily derived by using the MATLAB function `zpk()`. The capacitance of C_2 is less straightforward but is easily solved using MATLAB. The input impedance is now defined by the transfer function written in (3.51). Using the MATLAB symbolic toolbox the input impedance transfer function can be separated into its numerator and denominator, the denominator can be solved for a specific pair of poles in terms of values of C_2. The pair of poles desired can be found by either using the `minreal()` function to achieve two poles or by using `balred()`.

$$R_3 = \frac{n^2 R_1 k_{in}}{n^2 R_1 - k_{in}} \tag{3.50}$$

$$Z_{in}(s) = \left(R_3 + \frac{1}{s C_2} \right) \text{II} \left(\frac{n^2 (R_1 + R_2 + R_{th})(s R_1 \text{II}(R_2 + Rth) + 1)}{s C_1 R_2 + 1} \right) \tag{3.51}$$

Plotting the input impedance for the 4:1 complete circuit model shown in Fig. 3.33 reveals a good match with the detailed model's input impedance. The modified circuit model provides accurate representation of the DC and high frequency gains as seen by the magnitude plot of Fig. 3.33. More importantly it provides a good approximation of the phase of the input impedance. Proper modeling of the input impedance is imperative for use of the circuit model in a larger configuration such as the QPRSCC. The QPRSCC has input capacitors for both the switched-capacitor converter and the regulating PWM converter. The interaction of the isolated MMSCC with it's input capacitor is important as to the effect it will have on the both the voltage seen by either the MMSCC or the regulating PWM converter.

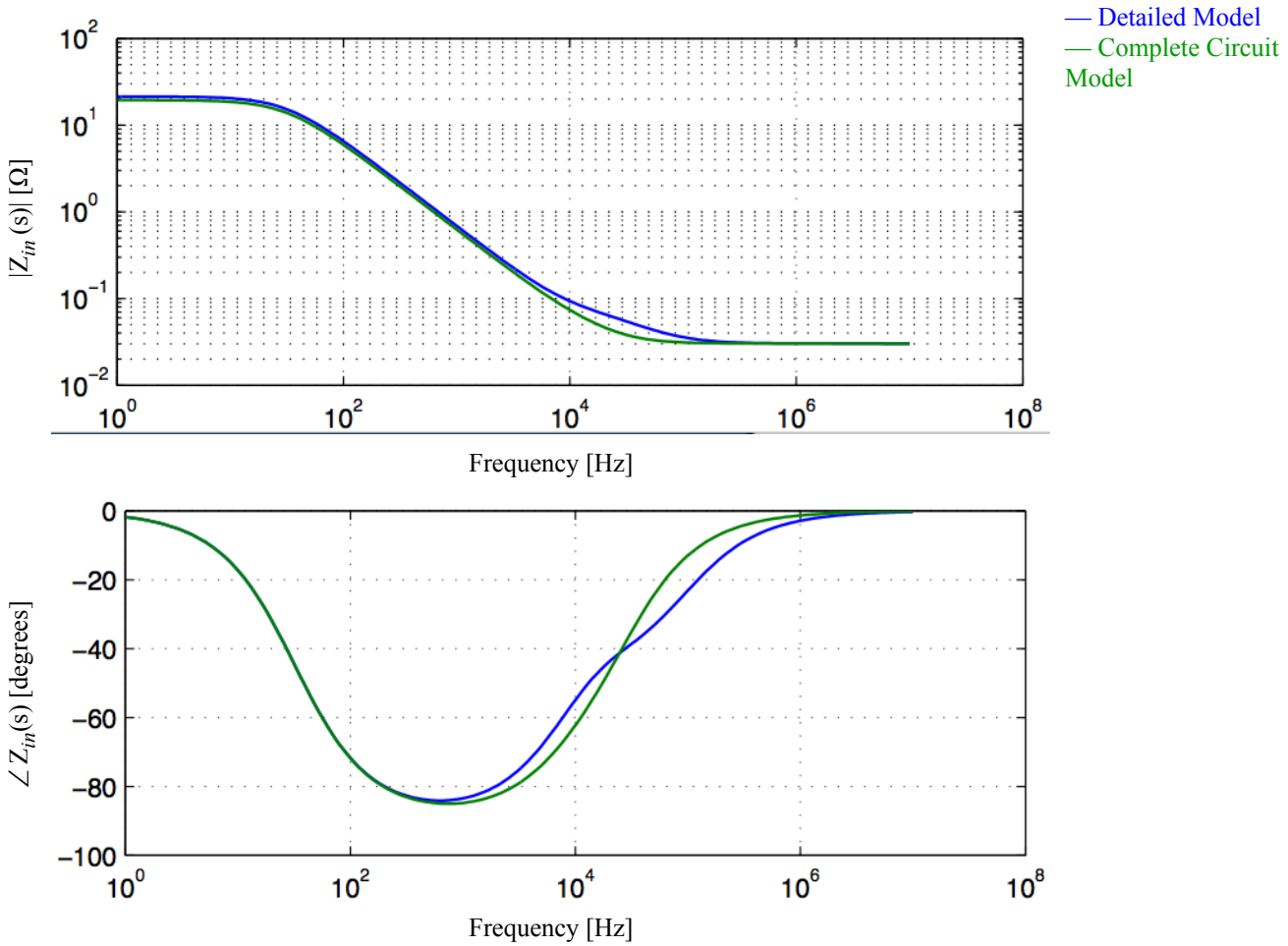


Fig. 3.34. Input impedance frequency response of the complete averaged small-signal circuit model and the detailed model for 4:1 operation.

3.2.3 Completed Average Dynamic Circuit Model of the Isolated MMSCC

An equivalent small-signal circuit model has been developed for the isolated MMSCC using a modified ROM based on the ROM proposed in [29]. The small-signal circuit is a second order circuit model as shown Fig. 3.35. The calculation of the resistances and capacitances have been outlined in the previous section 3.2.2. This section will compare the small-signal model to a switching model through SPICE simulations in LTSpice for each operating mode.

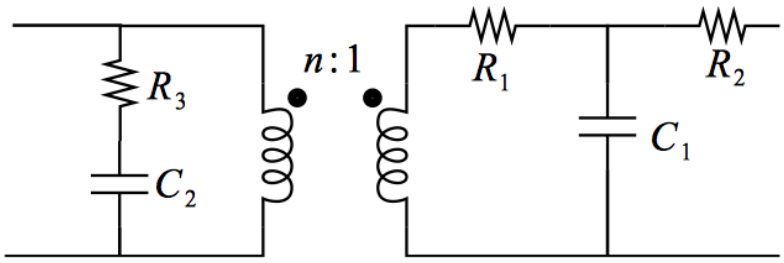


Fig. 3.35. Averaged small-signal circuit model of the MMSCC

The same switching SPICE model used before, depicted in Fig. 3.22, is compared to the developed small-signal circuit model in LTSpice. For the designed isolated MMSCC, the small-signal circuit model parameters are calculated, the results shown in Table 3.10. The models are given step changes in the input voltage v_g, Thévenin equivalent load voltage v_{th}, and the H-Bridge current i_{pwm}. Both the output voltage and the input current are compared for each operating mode. Note that the input current by the small-signal circuit model is the average input current while the switching model is the instantaneous input current.

TABLE 3.10: MMSCC SMALL-SIGNAL CIRCUIT MODEL PARAMETERS USED FOR SIMULATION

Conversion Ratio	R_1	R_2	R_3	C_1	C_2
4:1	12.367 mΩ	3.138 mΩ	35.856 mΩ	1318.97 µF	173.57 µF
3:1	21.094100845009	4.060 mΩ	32.344 mΩ	598.91 µF	166.14 µF
2:1	34.340564066457	4.133 mΩ	34.526 mΩ	449.56 µF	129.53 µF

The step responses for 4:1 operation are shown in Fig. 3.36. As expected the small-signal model does an excellent job of approximating the output voltage for a step change in the input voltage, Fig. 3.36(a), but does poorly modeling the dynamics of load changes as evident in Fig. 3.36(b) and Fig. 3.36(c). The small-signal circuit model does accurately depict the initial voltage response and steady state value for a step in the current. The input current step responses to each system input are compared in Fig. 3.36(d-f) and illustrate that the average input current, i.e. input impedance, is accurately modeled by the small-signal circuit model.

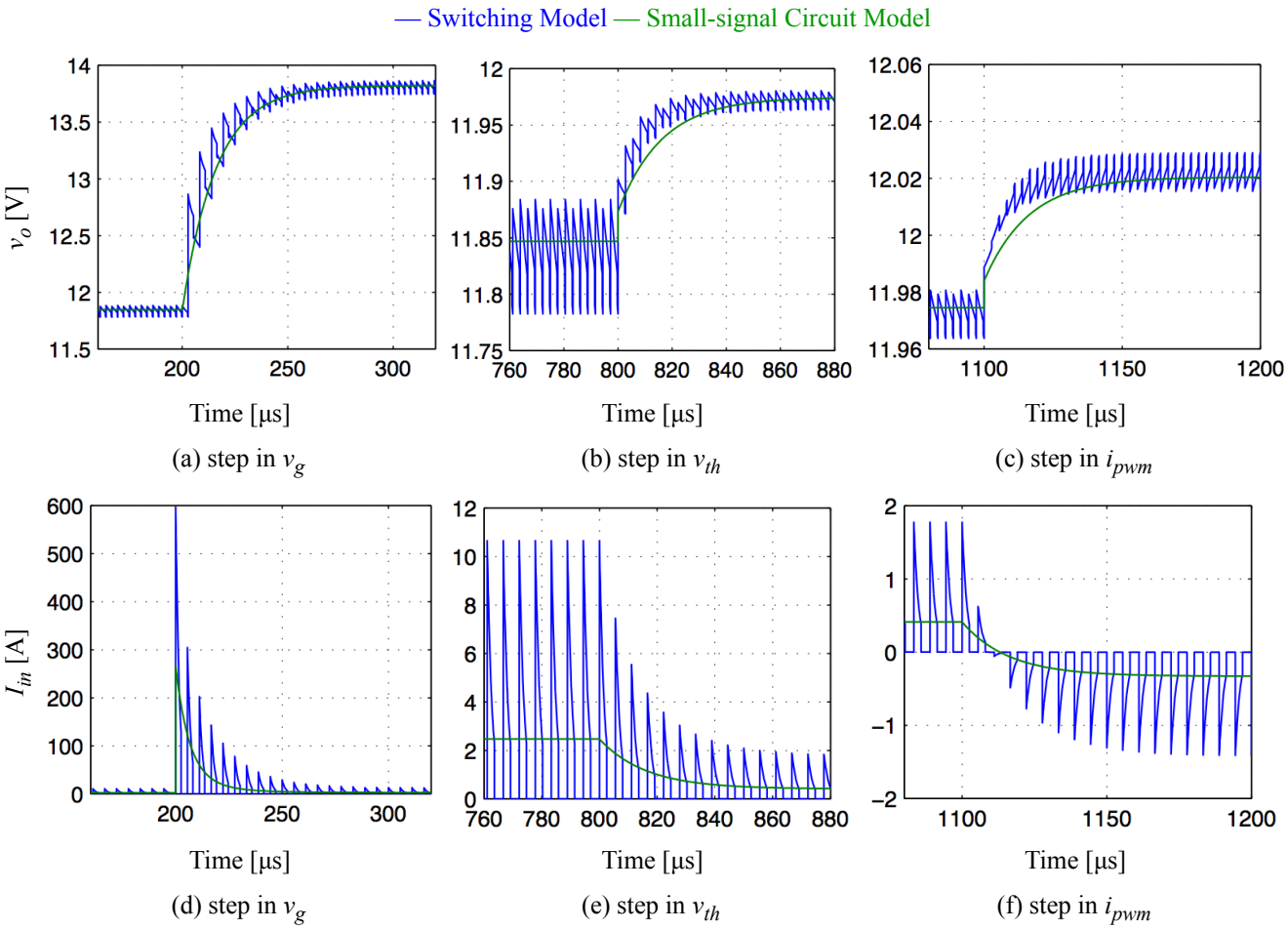


Fig. 3.36. Comparison of the output voltage and input current responses of the 4:1 MMSCC Switching SPICE Model and Small-Signal Circuit Model to a step in (a,d) v_g, (b,e) v_{th}, and (c,f) i_{pwm}.

The step responses for 3:1 operation are shown in Fig. 3.37. As expected the small-signal model does a excellent job approximating the output voltage for a step in the input voltage, Fig. 3.37(a), but reasonably models the dynamics of load changes as evident in Fig. 3.37(b) and Fig. 3.37(c). The small-signal circuit model accurately depicts the initial voltage response and steady state value for a step change in the current. The input current step response to the various system inputs are compared in Fig. 3.37(d-f) and demonstrate that the small-signal circuit model correctly model the average input current dynamics.

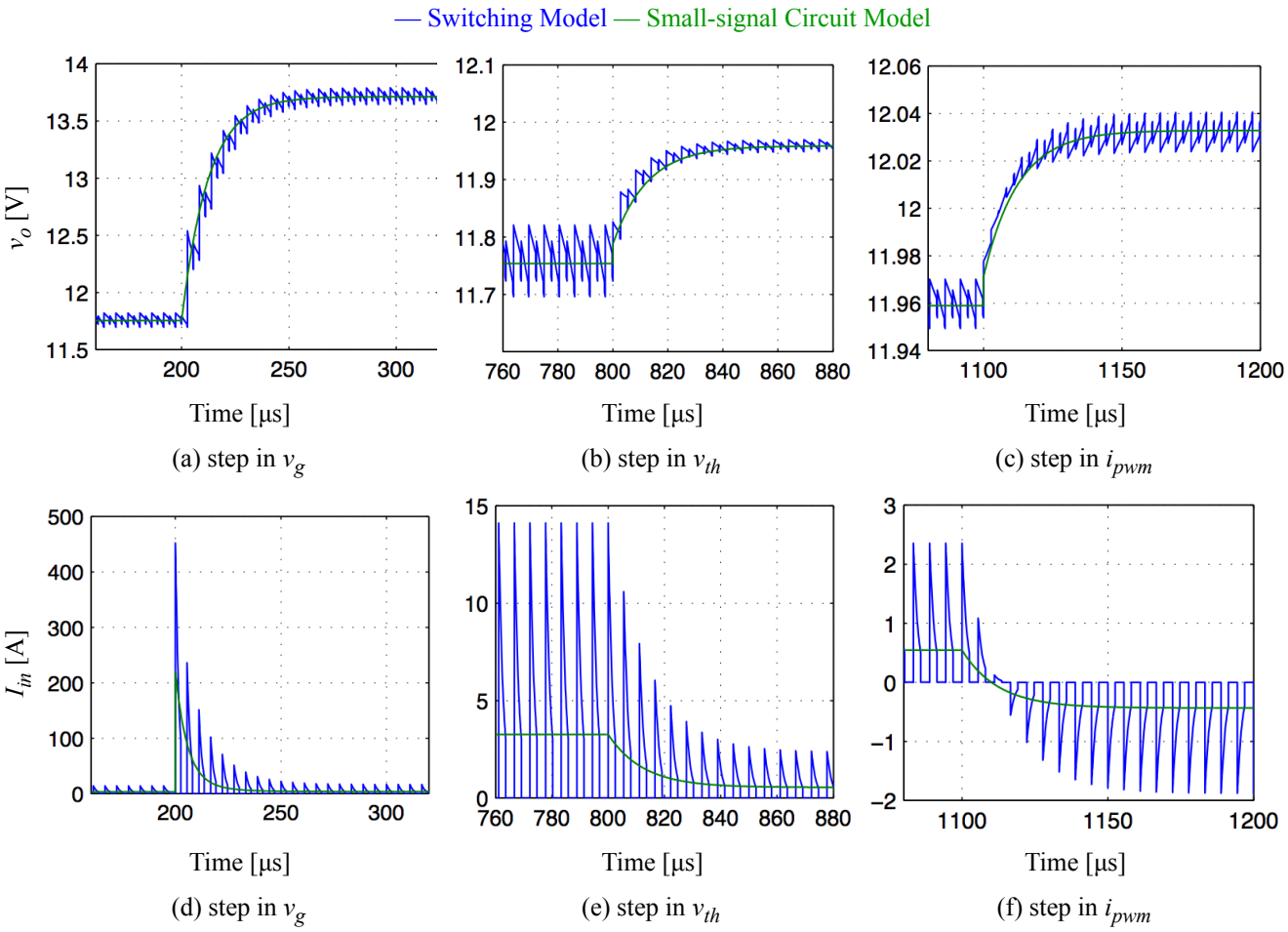


Fig. 3.37. Comparison of the output voltage and input current responses of the 3:1 MMSCC Switching SPICE Model and Small-Signal Circuit Model to a step in (a) v_g, (b) v_{th}, and (c) i_{pwm}.

The step responses for 2:1 operation are shown in Fig. 3.11. Again, the small-signal model does an excellent job approximating the output voltage for a step in the input voltage, Fig. 3.11(a), and for changes in the load current evident in Fig. 3.11(b) and Fig. 3.11(c). The small-signal circuit model accurately models both the input to output voltage dynamics as well as the output impedance for 2:1 operation. The input current step response to each system input is compared in Fig. 3.11(d-f) and shows that the small-signal circuit model correctly models the average input current dynamics.

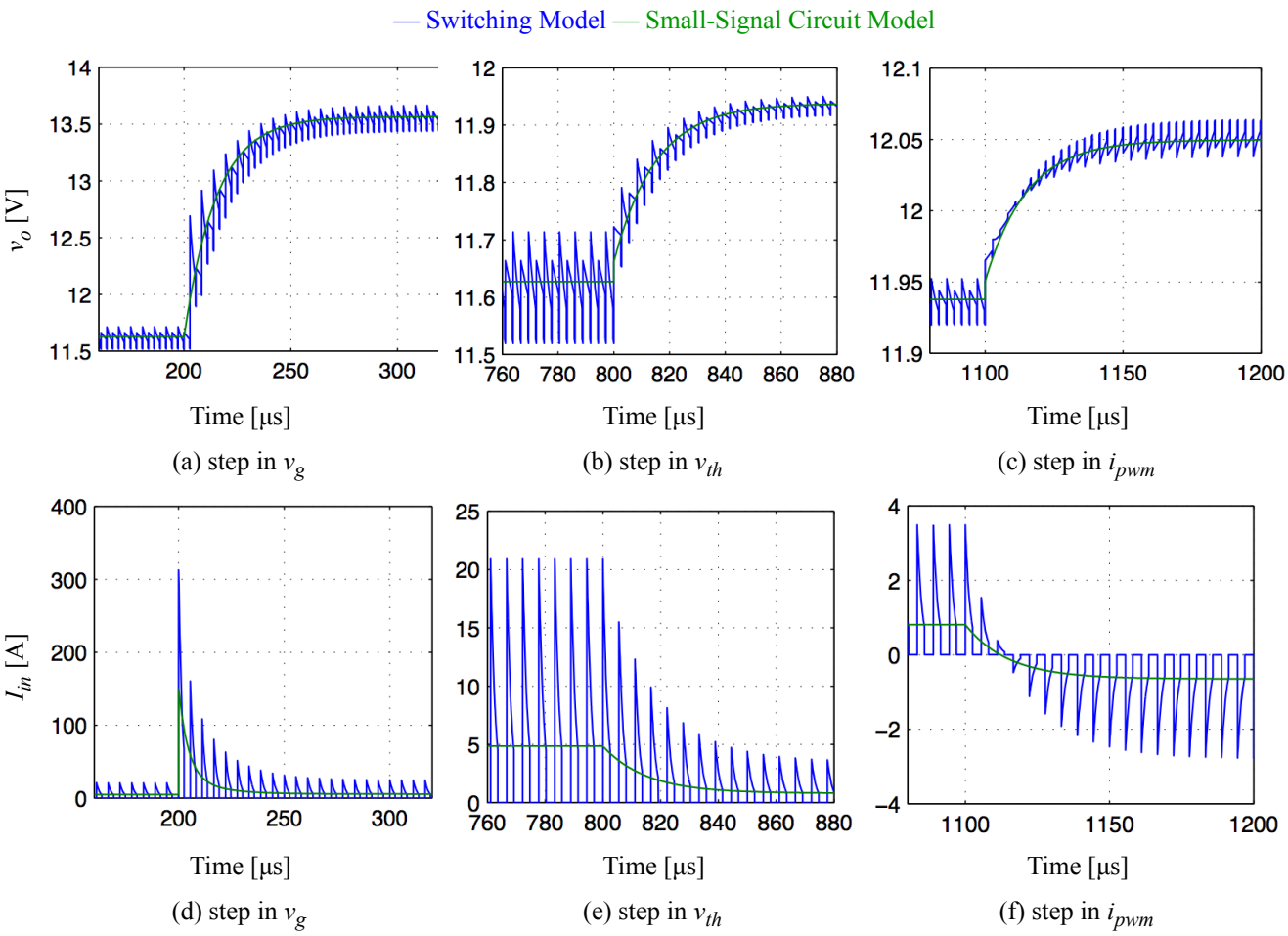


Fig. 3.38. Comparison of the output voltage and input current responses of the 2:1 MMSCC Switching SPICE Model and Small-Signal Circuit Model to a step in (a,d) v_g, (b,e) v_{th}, and (c,f) i_{pwm}.

3.3 H-Bridge DC/DC Converter

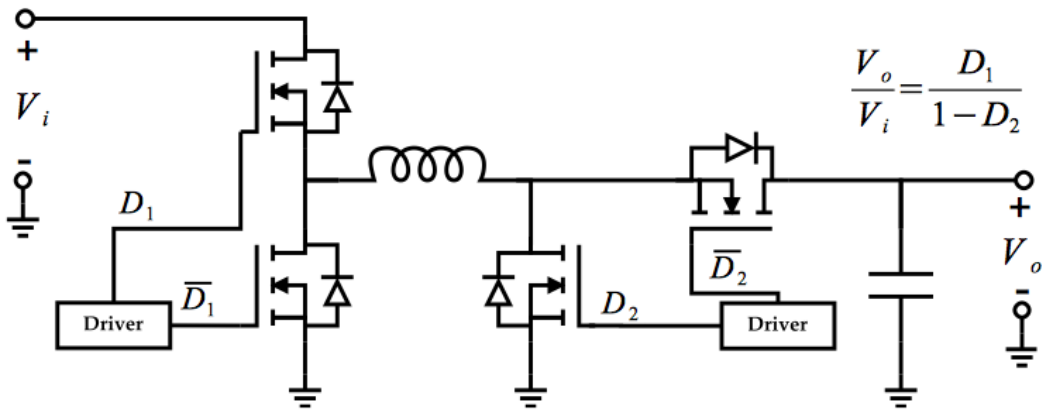


Fig. 3.39. The H-Bridge DC/DC Converter utilizes one inductor and an output capacitor

The DC/DC H-Bridge converter allows for buck-boost operation while offering high efficiencies and standard control [64,65]. Unlike the Zeta or SEPIC converters [57,62] which are fourth order systems with two inductors and two capacitors, the H-Bridge has one inductor and one output capacitance as shown in Fig. 3.38. The SEPIC (and sometimes the Zeta) suffer from right half plane (RHP) zeros causing for careful control design. The H-Bridge is a second order system and with a RHP pole seen in all boost converters. Overall the control of the H-Bridge is less complicated, easily implemented, and achieves higher bandwidths than the slower Zeta and SEPIC converters [64,65]. A high efficiency voltage-control strategy for the H-Bridge is already well documented and circuit implementation has been designed [64,65]. A commercially available power regulator IC, the LT8705 from Linear Technologies, provides all necessary functions: gate drive, control, and voltage and current limits, and is utilized in this prototype. Being able to use a commercially available chip allows the QPRSCC to be viable in terms of mass production.

3.3.1 Design of the H-Bridge Converter

The LT8705 is to be used to provide the control and gate drive of the H-Bridge. The H-Bridge will be operated in forced continuous conduction mode to simplify the analysis and design of the QPRSCC. This will lead to lower efficiency in the H-Bridge at light load operation but future revisions can utilize the LT8705 “Burst Mode” to improve light load efficiencies. The H-Bridge is designed to use LT8705 maximum switching frequency of 400kHz. This switching frequency is chosen to allow for higher control bandwidth (generally designed to a tenth of the switching frequency) but more so to decrease

the size of the inductor.

The design guide, [69], provided by Linear Technology is used to select the minimum needed inductance and the feedback resistors for the regulated output voltage. Design of the current sensing network, current monitor, and other auxiliary control will not be covered in this paper. The focus in this section is the selection of the power components such as the MOSFETs and inductor. The design of current sensing and control aspects of the H-Bridge can be seen in the LT8705 datasheet [69].

The selection of output capacitance is neglected from this section as output capacitance needed by the SCC is significantly larger and will provide the stable output voltage for the H-Bridge as well. The input capacitance selection will be covered in Chapter 5 Experimental Results. The only requirements for the H-Bridge input capacitance is that it remains stable over one switching period. Beyond that the selection of input capacitance in Chapter 5 will be due to system dynamics explored in Chapter 4 QPRSCC Modeling and Analysis.

A. Inductance and Inductor Selection

Following the LT8705 design guide, the current sense resistor R_{sense} is chosen to be 8mΩ and the switching frequency is chosen to be 400kHz. Since the input voltage can vary from twice to less than half the output voltage the inductor's inductance must satisfy (3.52) and (3.53) to prevent subharmonic oscillations. The subharmonic oscillations are a known issue with current mode control when the duty cycle is above 50%. The LT8705 utilizes slope compensation to rectify the issue but the inductance must meet (3.52) and (3.53) to effectively prevent subharmonic oscillations.

$$L_{BOOST(MIN)} > \frac{\left(V_{o(max)} - \left(\frac{V_{in(min)} V_{o(max)}}{V_{o(max)} - V_{in(min)}}\right)\right) R_{sense}}{0.08 f_{sw}} [\mathrm{H}] \tag{3.52}$$

$$L_{BUCK(MIN)} > \frac{V_{in(max)} \left(1 - \left(\frac{V_{o(max)}}{V_{in(max)} - V_{o(min)}}\right)\right) R_{sense}}{0.08 f_{sw}} [\mathrm{H}] \tag{3.53}$$

The output voltage will be set at a constant 12V. The input voltage for the H-Bridge is set at a minimum 4V and a maximum 24V, these limits were found in section 3.1.3.C. Solving (3.52) and (3.53) gives the minimum inductance needed in (3.54).

$$L_{BOOST(MIN)} > 1.5[\mu \mathrm{H}] \tag{3.54}$$

$$L_{BUCK(MIN)} > 0[\mathrm{H}] \tag{3.55}$$

$$L > MAX\left(L_{BOOST(MIN)}, L_{BUCK(MIN)}\right) > 1.5[\mu\mathrm{H}] \tag{3.56}$$

The inductance must be larger than 1.5μH for proper operation of the current mode control when the input voltage is either half or twice the output voltage. Inductance values must be chosen to allow for a small inductor size but also have a reasonable ripple current. Typically the ripple current is chosen as a percentage of the maximum output current. Due to the structure of the QPRSCC, the H-Bridge will see different output currents depending on the total input voltage. Given ideal converters, the output current of the H-Bridge is proportional to the total QPRSCC output current by the ratio of the H-Bridge input voltage to the total QPRSCC input voltage. The output current of the H-Bridge is plotted in Fig. 3.40 showing that the maximum output current, while in Buck operation, will be 4A and occurring at an input voltage of 36V for the QPRSCC. For Boost mode the worst case ripple occurs while the input voltage is the smallest. This is when the H-Bridge has an input voltage of 4V or 40V and 52V for the QPRSCC. The output current at this time for the H-Bridge is at approximately 1A which correlates to roughly 3A inductor current.

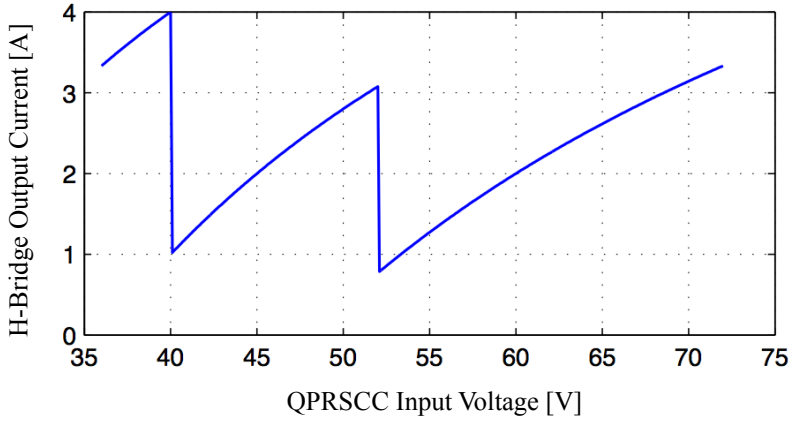


Fig. 3.40. Output current of the H-Bridge across the QPRSCC input voltage range while QPRSCC operates at 120W (10A output current)

Typically a ripple current from 30% to 50% of the inductor current is desired to minimize output capacitance and minimize the peak current in the switches allowing for smaller MOSFETS. The inductance for a given ripple current ΔI, output voltage V_o, switching frequency f_{sw}, and duty ratio D_1 for buck operation can be found with (3.55). For boost operation the inductance can be calculated by (3.56) where D_2 is the Boost mode duty ratio, this is typically calculated at the smallest input voltage which results in worst case ripple current.

$$L_{BUCK} = \frac{(1 - D_1) V_o}{\Delta I f_{sw}} [\mathrm{H}] \tag{3.57}$$

$$L_{BOOST} = \frac{V_{in(min)} D_2}{\Delta I f_{sw}} [\mathrm{H}] \tag{3.58}$$

For Buck operation the maximum ripple current occurs at the maximum input voltage, which is 16V for 2:1 and 3:1 SCC operation and 24V for 4:1 SCC operation. For 2:1 and 3:1 operation the ripple current is selected as 1.5A, 50% of the 3A output current for 16V input to the H-Bridge with 3:1 SCC operation. For Boost mode the ripple current is also 1.5A which is 50% of the maximum inductor current of 3A. The inductance is then calculated for each case in (3.57) and (3.58) and an inductance of 5μH will provide a reasonable ripple current. This ignores the higher input voltages of the QPRSCC where the H-Bridge will have an input voltage up to 24V. With an inductance of 5μH there will be a ripple current of 3A at QPRSCC input voltage of 72V. This is a 100% ripple current but will be considered acceptable for the following reasons. Any savings in output capacitance due to higher inductance is irrelevant as the output capacitance is already determined by the requirements of the SCC. The output capacitance is on the order of hundreds of μF where the output capacitance for the H-Bridge is on the order of tens of μF. Second, increasing the inductance would not result in smaller MOSFETs due to the lowered peak current. The H-Bridge already has a low current and voltage requirement, the slightly larger peak current due to the increased ripple will not require a larger MOSFET. The third and final reason is a huge emphasis is being placed on minimizing the size of the inductor.

$$L_{BUCK} = \frac{(1 - 0.75)12\mathrm{V}}{1.5\mathrm{A}(400\mathrm{kHz})} = 5[\mu\mathrm{H}] \tag{3.59}$$

$$L_{BOOST} = \frac{4\mathrm{V}(0.67)}{1.5\mathrm{A}(400\mathrm{kHz})} = 4.45[\mu\mathrm{H}] \tag{3.60}$$

The chosen inductor, IHLP3232DZER4R7M11, has a nominal inductance of 4.7μH. The thermal current rating of 8A and a saturation current rating of 8.7A. The average inductor current can be approximated by dividing the H-Bridge output current, plotted in Fig. 3.40, by (1-D_2) when the H-Bridge is in boost mode. The average inductor current reaches a maximum of 4A at 40V input to the QPRSCC as shown in Fig. 3.41. With approximately 150% ripple current a peak inductor current of 6A is expected. At 72V input the ripple current is 3.2A with a 4.7μH inductor, resulting in a peak current of roughly 5A.

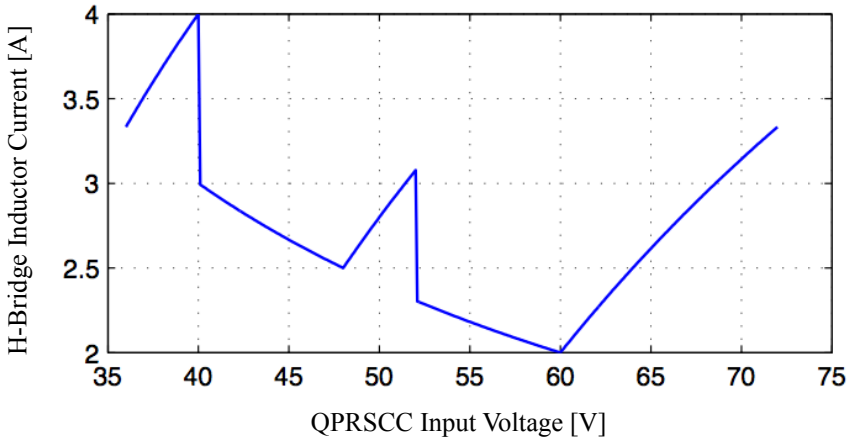


Fig. 3.41. Inductor current of the H-Bridge over the QPRSCC input voltage range while QPRSCC is operating at 120W (current of 10A)

B. Feedback Resistors and Output Voltage

The choice of feedback resistors, although trivial, is included as it will provide the regulated output voltage. The LT8705 datasheet gives (3.59) to calculate the output voltage for a choice in feedback resistors R_{FBOUT1} and R_{FBOUT2} shown in Fig. 3.39.

$$V_o = 1.207\text{V}\left(1 + \frac{R_{FBOUT1}}{R_{FBOUT2}}\right) \tag{3.61}$$

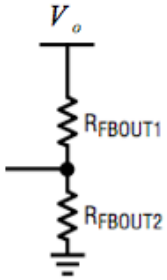


Fig. 3.42. H-Bridge feedback resistors

The feedback resistors are chosen as 102kΩ and 11.3kΩ for R_{FBOUT1} and R_{FBOUT2} respectively. This gives an output voltage of 12.1V. This is above the desired 12V by less than 1% and close enough for any application.

C. MOSFET Selection

The last major power component to be selected is the MOSFET. Efficiency, while important ,is not the driving design constraint for the H-Bridge. As previously shown, the QPRSCC can achieve high efficiency even with a regulating converter achieving efficiencies in high 80% or low 90% range as long as a majority of the power is converted through the SCC. Assuming the SCC is more efficient, the priority is placed on small package size.

The H-Bridge has four switches-two on the input and two on the output side. On the input side the maximum input voltage (i.e. blocking voltage) will be 24V. In an effort to prevent catastrophic failure the input MOSFETs are chosen to be able to block the full input voltage of 72V, where the H-Bridge sees the full QPRSCC input voltage. Future designs can fully utilize the lower voltage stress provided by the QPRSCC on the regulating converter. The output voltage switch's blocking voltage is the 12V output voltage.

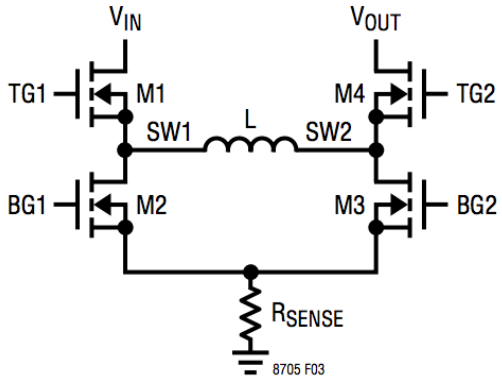


Fig. 3.43. Simplified diagram of the H-Bridge from the LT8705 Datasheet [69]

The switch M1 will see conduction losses in both the Boost and Buck operating modes and will have the same current as the inductor, L. During buck operation the switch M1 will also see switching losses which can tend to dominate the losses. Switching losses are somewhat reduced due to low input voltages and low currents (Fig. 3.41) in buck mode. The switch M2 operates in buck and buck-boost mode and is generally dominated by conduction losses. Again a low on-resistance is desired balanced against package size.

Switch M3 operates in boost and buck-boost mode and similar to M1, the losses are from switching and conduction losses. Also similar to M1 the switches see small currents minimizing the switching losses that may come to dominate the power loss in M1. For switch M4, the switching losses are typically small and conduction losses tend to dominate.

With this in mind the AON7280 and the PSM3R9 are selected for M1,M2 and M3,M4 respectively. Both MOSFETs come in a small 3.3x3.3mm package, providing a small footprint while meeting design requirements. A summary of the MOSFETs properties are given in Table 3.11. The PSM3R9 is the same MOSFET chosen for the SCC. Although it has a higher current rating than needed it is selected to limit the number of different components This is beneficial for bulk ordering and for automated component placing.

TABLE 3.11: SUMMARY OF MOSFET PROPERTIES

MOSFET	V_{DS}	I_D (V_{GS}=10V)	maximum $R_{DS(ON)}$ (V_{GS}=10V) @25ºC	Q_G (V_{GS}=10V)	C_{OSS}
AON7280	80V	50A	8.5mΩ	26.5nC	1000pF (V_{DS}=12V)
PSMN3R9-25MLC	25V	70A	4.15mΩ	24nC	400pF (V_{DS}=12V)

3.3.2 Modeling the H-Bridge Converter

The H-Bridge has been modeled using Averaged State-Space with success as seen in [64,65]. The dynamics of interest for the QPRSCC are the control to output voltage transfer function and the output impedance transfer function. The output impedance of the QPRSCC can be approximated by the SCC and the H-Bridge output impedances in parallel as shown in [48]. The H-Bridge control to output voltage transfer function is to be compared with the transfer function of the QPRSCC. This will be investigated in Chapter 4 QPRSCC Modeling and Analysis demonstrating that the control strategies proposed for the H-Bridge will work for the QPRSCC. This will also validate the use of LT8705 to regulate the H-Bridge and thus the QPRSCC. This section will investigate just the H-Bridge output impedance and the control to output voltage transfer function.

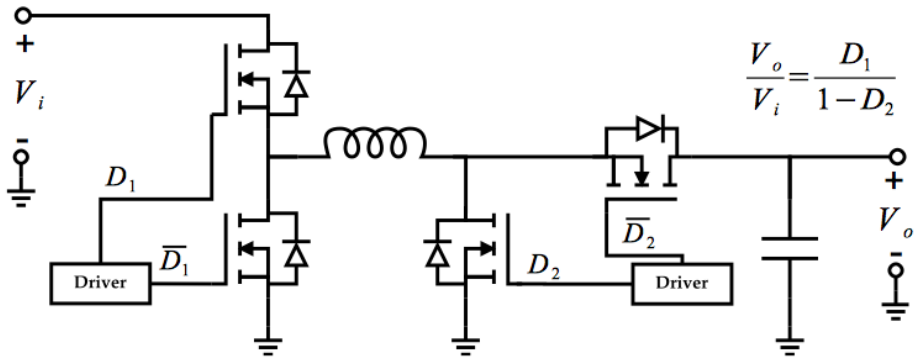
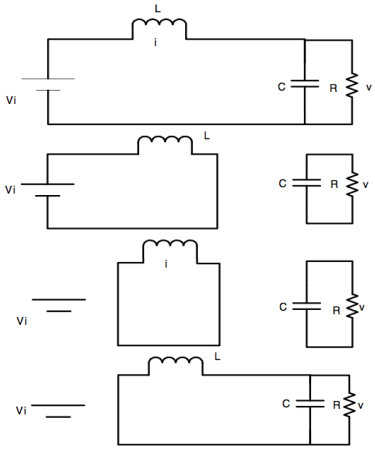
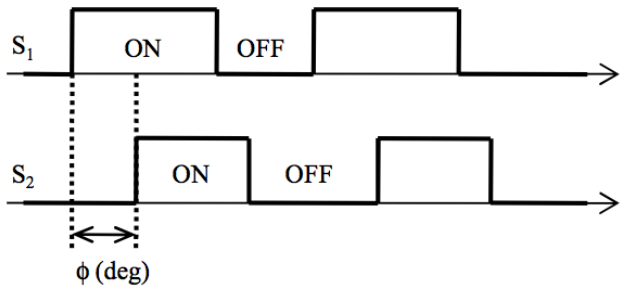


Fig. 3.44. The H-Bridge DC/DC Converter can be controlled by two independent duty ratios D_1 and D_2 controlling the buck and boost portion respectively.

The H-Bridge, shown in Fig. 3.42, will be modeled as in [65]. There are four possible states, Fig. 3.45(a), for the converter depending on the switches. The switches are controlled by D_1, D_2, and by the phase difference ϕ as shown in Fig. 3.45(b).



(a) four states of H-Bridge



(b) example waveforms for switches S1 and S2

Fig. 3.45. The H-Bridge can achieve (a) four different states depending on the switches. (b) The duty ratios D_1, D_2, and the phase difference ϕ control the state of switches S1 and S2 with S3 and S4 acting synchronously.

Using state-space averaging techniques the H-Bridge is described by the state equation (3.60) where $\mathbf{x}=[i_L\ v_C]^T$, $\mathbf{u}=[V_i\ I_z]^T$, and the matrices **A** and **B** are given in (3.61) and (3.62) respectively. The placeholders *r* and α are defined in (3.63) and (3.64). The inductance and output capacitance are given as L and C respectively. The resistances of the switches r_s, the inductance r_L, the capacitor ESR r_C, and the output resistance R are included in this model.

$$\frac{d}{dt}\mathbf{x}=\mathbf{A}\,\mathbf{x}+\mathbf{B}\,\mathbf{u} \tag{3.62}$$

$$\mathbf{A}=\begin{bmatrix} \frac{-r}{L} & \frac{-\alpha}{L}(1-D_2) \\ \frac{\alpha}{C}(1-D_2) & \frac{-\alpha}{CR} \end{bmatrix} \tag{3.63}$$

$$\mathbf{B}=\begin{bmatrix} \frac{D_1}{L} & 0 \\ 0 & \frac{\alpha}{C} \end{bmatrix} \tag{3.64}$$

$$r=(4r_s+2r_L)(D_1-\phi)-\alpha r_c D_2+(\alpha r_c+r_L+2r_s) \tag{3.65}$$

$$\alpha=\frac{R}{R+r_C} \tag{3.66}$$

The output y is the output voltage and given by the state equation (3.65) where **C** is given by (3.66) and **D** by (3.67).

$$y=v_o=\mathbf{C}\mathbf{x}+\mathbf{D}\mathbf{u} \tag{3.67}$$

$$\mathbf{C}=\begin{bmatrix}(1-D_2)\alpha r_C & \alpha\end{bmatrix} \tag{3.68}$$

$$\mathbf{D}=\begin{bmatrix}0 & \alpha r_C\end{bmatrix} \tag{3.69}$$

Using this averaged state space model, the output impedance transfer function will be derived and compared to the SCC in subsection A. The control-to-output voltage transfer function will be briefly investigated in subsection B while comparison to the QPRSCC control-to-output transfer function given in Chapter 4.

A. Output Impedance Transfer Function

The small-signal output impedance of the H-Bridge can be investigated at various DC operating points and compared to the output impedance of the SCC. Provided the SCC output impedance is smaller than it can reasoned that load transients will generally by resolved by the SCC. Given small perturbations in the output current via I_z there will be perturbations in the output voltage proportional to the output impedance. To obtain the small-signal output impedance the duty ratios are held constant thus (3.60) and (3.65) hold true for the small-signal variables $\tilde{\mathbf{x}}$, $\tilde{\mathbf{u}}$, and $\tilde{\mathbf{y}}$. The output impedance is then given as (3.68).

$$Z_o(s)=\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)}=\left(\mathbf{C}[s\mathbf{I}-\mathbf{A}]^{-1}\mathbf{B}+\mathbf{D}\right)\Big|_{\tilde{v}_{in}=0} \tag{3.70}$$

The output impedance will be evaluated at input voltages of 4V, 12V, and 16V and then at low and high load currents. The H-Bridge has a maximum load current of 4A and the minimum load will be approximated by a load of 0.2A. This will adequately show the affect of the DC operating point on the output impedance. As seen in Fig. 3.46 the output impedance is significantly affected by the operating point in boost mode. When DC output impedance can be written as (3.69), it becomes apparent that the output impedance will increase as the input voltage drops (thus increasing D_2).

$$Z_o = \frac{r}{(1-D_2)^2} \tag{3.71}$$

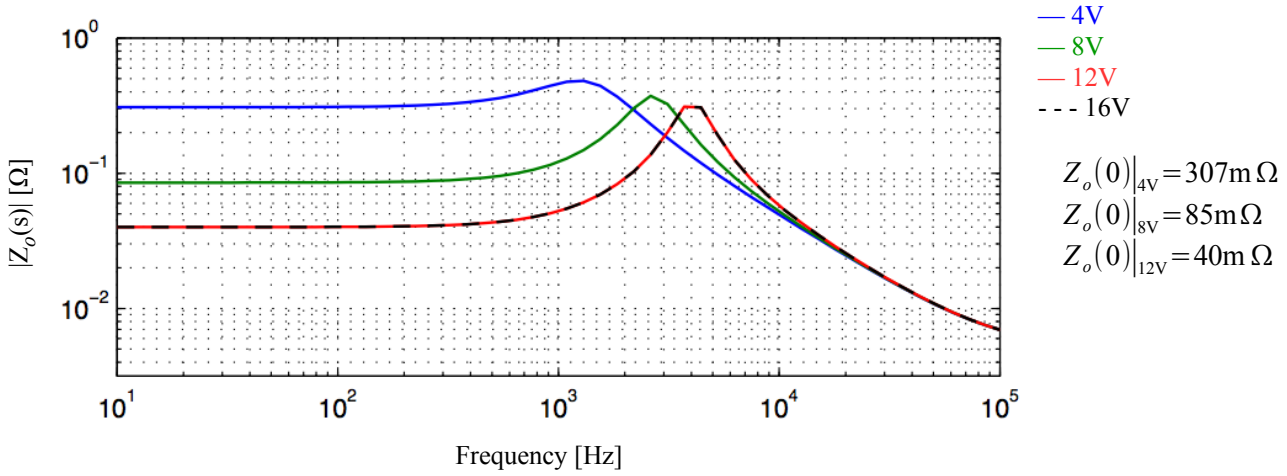


Fig. 3.46. The output impedance frequency response of the H-Bridge at different input voltages.

Other variations at the operating point are due to the load current represented by the resistive load R. The load is varied from 0.2A to 4A at 4V and at 12V in Fig. 3.47 showing insignificant variation in the output impedance. As evident in Fig. 3.46, it is variation of D_2 that significantly changes the output impedance.

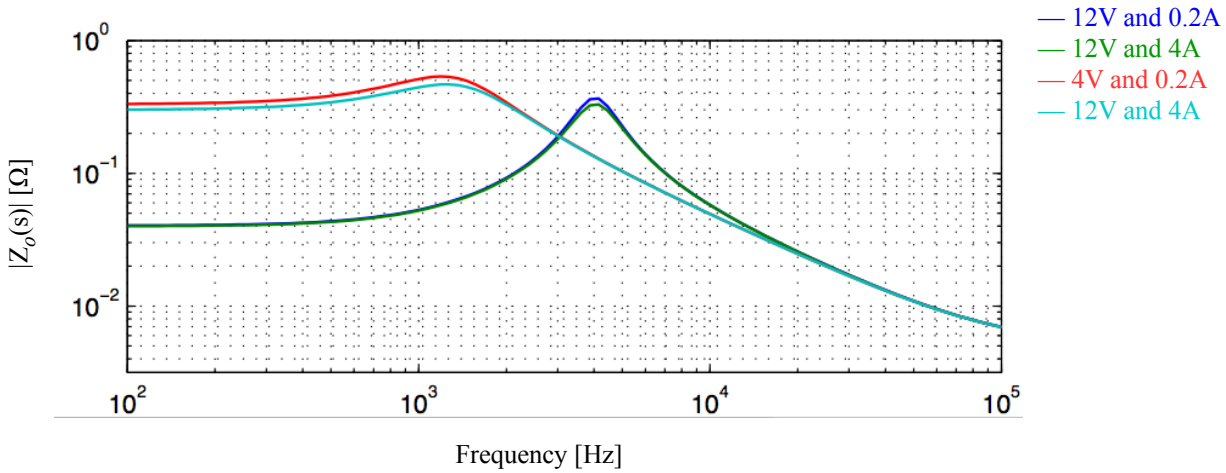


Fig. 3.47. Output impedance frequency response of the H-Bridge for various current loads.

As discussed in [48], during load transients the two converters, H-Bridge and SCC, will each provide current, but how the current is apportioned is dependent on their respective output impedance. The converter with the lower output impedance will handle more of the current during transients. Comparing the output impedances of the H-Bridge and the SCC in Fig. 3.48, shows that the SCC does have a smaller output impedance. An exception is the output impedance for 2:1 operation of the SCC is almost the same as the H-Bridge operating in Buck mode. For 3:1 and 4:1 operation the SCC has a much lower output impedance compared to the H-Bridge.

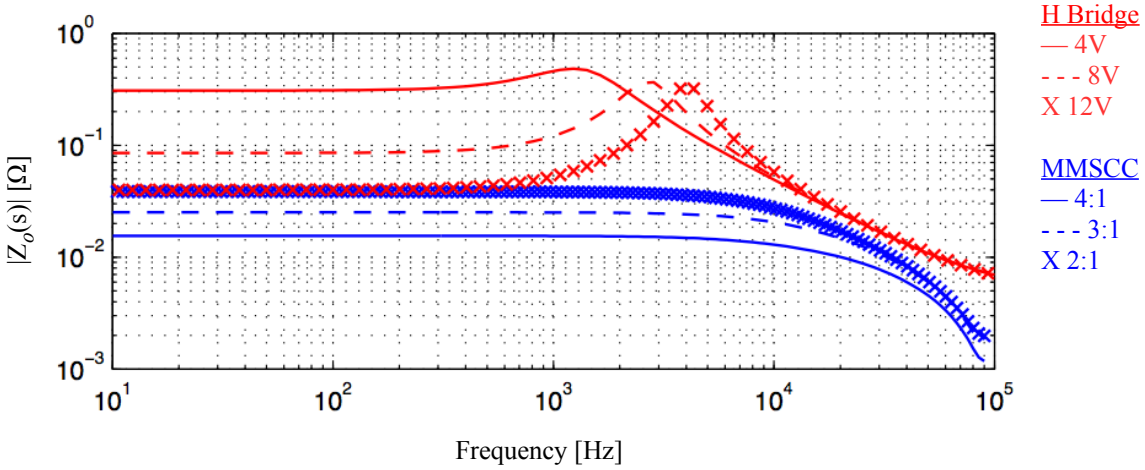


Fig. 3.48. Comparison of the H-Bridge and MMSCC output impedance frequency responses.

B. Control to Output Voltage Transfer Functions

The small-signal control to output voltage transfer function can be derived for each duty ratio D_1 and D_2. As in [64,65] using each duty ratio as separate control variable allows for high efficiency operation and tight control of the H-Bridge. Using LTSpice and investigating their SPICE model of the LT8705

indicates that it follows the general concepts outlined in [65] and achieves high efficiency while providing suitable regulation of the output voltage. The open loop transfer functions for D_1 and D_2 are shown in (3.70) and (3.71) respectively.

$$\frac{\tilde{v}_o(s)}{\tilde{d}_1(s)} = \frac{N_1}{\left(s^2 + \delta\omega_o s + \omega_o^2\right)}\omega_{vdz1} \tag{3.72}$$

$$N_1 = \frac{V_i \alpha}{LC(1-D_2)} \qquad \omega_{vdz1} = \frac{-2(2r_s + r_L)D_1}{R + Z_o} + (1-D_2)^2$$

$$\delta = \frac{\frac{1}{(1-D_2)R}\sqrt{\frac{L}{C}} + \frac{(1-D_2)Z_o}{\alpha}\sqrt{\frac{C}{L}}}{\sqrt{Z_o/R\,\alpha + 1}} \qquad \omega_o = \frac{(1-D_2)\alpha}{\sqrt{LC}}\sqrt{\frac{Z_o}{R\,\alpha} + 1}$$

$$\frac{\tilde{v}_o(s)}{\tilde{d}_1(s)} = \frac{N_2}{\left(s^2 + \delta\omega_o s + \omega_o^2\right)}(s - \omega_{vdz2}) \tag{3.73}$$

$$N_2 = \frac{-D_1 V_i \alpha}{(1 + Z_o/R)(1-D_2)^2 C R} \qquad \omega_{vdz2} = \frac{r - (1-D_2)(4r_S + 2r_L + \alpha r_C + \alpha R(1-D_2))}{L}$$

By inspection of (3.70) it is seen that characteristics of the duty ratio D_1 to the output voltage is essentially the same as a buck converter's transfer function. Similarly inspection of (3.71) shows the duty ratio D_2 to output voltage is much like the boost converter and contains a right half plane zero. The RHP zero is result of the H-Bridge topology and can be resolved with current mode control as is performed in most commercial boost converters. In [65], it is reasoned that this RHP zero makes the duty ratio D_2 undesirable as a feedback control variable and that D_1 is the feedback control variable of choice. The proposed control structure from [65] utilizes a voltage mode feedback type III compensation circuit for D_1 and a dual feedforward circuit for D_2 with feedforward signals of input voltage and output current.

This control strategy allows for the design of the voltage mode feedback type III compensation circuit for D_1 using the frequency response plots of the control D_1 to output voltage transfer function. The frequency response of each control-to-output voltage transfer functions are shown in Fig. 3.49 and illustrates that D_1 frequency response is similar to that of a buck converter. The frequency response of D_2's control-to-output transfer function shows the effect of the RHP zero. The frequency response of each of these transfer functions will be compared in chapter 4 to the control-to-output transfer functions

of the QPRSCC to illustrate that the control strategy employed for the H-Bridge will be suitable for the QPRSCC as well.

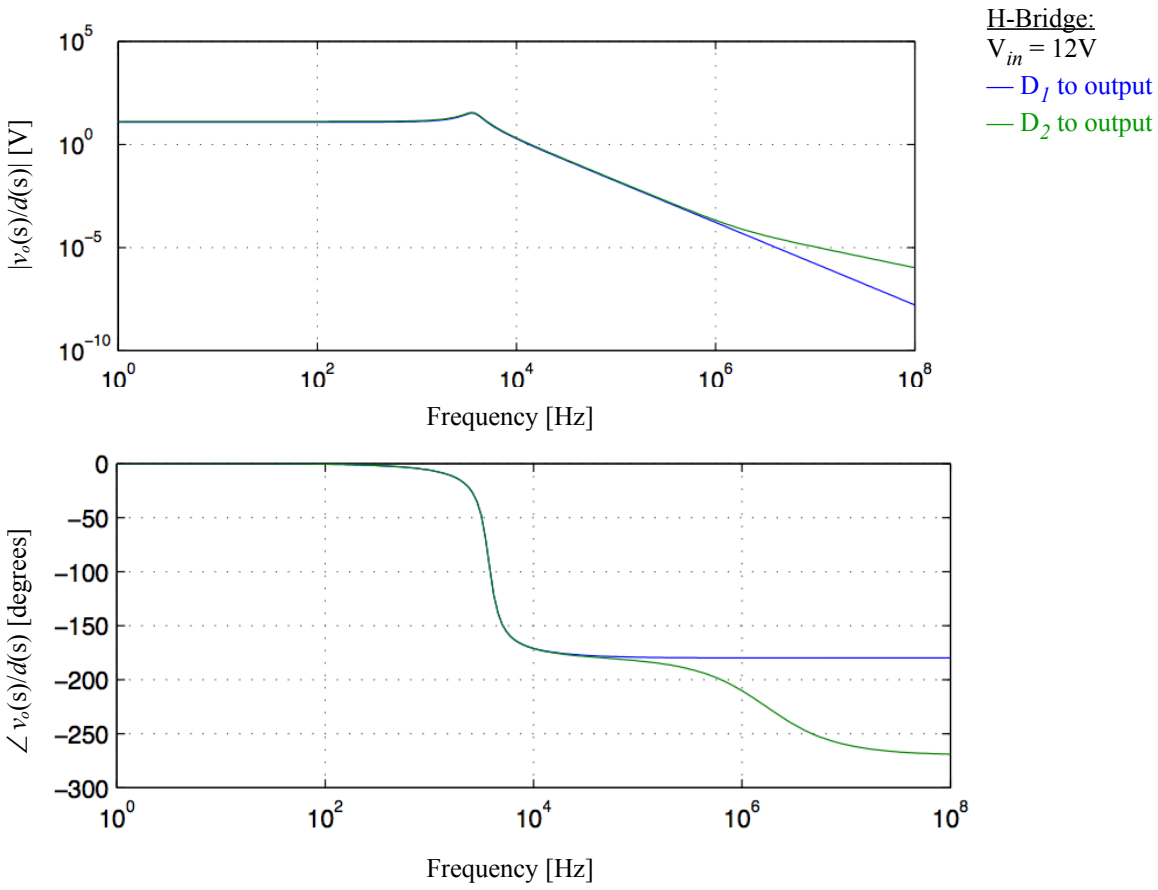


Fig. 3.49. Frequency response of each duty-ratio-to-output voltage showing the Buck and Boost nature of D_1 and D_2 respectively. The RHP zero in D_2 can be seen at 1MHz.

Chapter 4 Quasi-Parallel Regulated Switched-Capacitor Converter Modeling and Analysis

The quasi-parallel configuration has been previously used and analyzed with magnetic based converters [48,49]. Although the behavior in steady-state of the unregulated SCC is similar to unregulated magnetic converters, the dynamics differ. It is necessary to model the dynamics of the quasi-parallel regulated switched-capacitor converter (QPRSCC) for selections of passive elements such as the input capacitors can be made to mitigate such things as line voltage variations, and model the control-to-output voltage dynamics necessary for closed loop design. A commercial chip, the LT8705, will be employed to control the H-Bridge and provide control of the QPRSCC. This work will show that a control strategy for the H-Bridge will be sufficient for control of the QPRSCC. An estimate of the QPRSCC efficiencies will be made by calculating conduction and switching losses of the multilevel modular switched-capacitor converter (MMSCC) and H-Bridge. Finally simulations of the QPRSCC, (utilizing the LT8705), using LTSpice will demonstrate the load and line voltage transient behavior.

To model and analyze the Quasi-Parallel Regulated Switched-Capacitor Converter (QPRSCC) the Vopérian PWM switch model will be employed in addition to with the equivalent reduced order SCC circuit model developed in section 3.3.2. The Vopérian PWM switch model presented in [70] and the alternate form in [71] allow for analytical analysis of DC/DC converters and for simulation in SPICE simulators such as LTSpice. Both DC and small-signal characteristics of converters can be analyzed utilizing these switch models. The equivalent DC and small-signal PWM switch model is shown in Fig. 4.1(a) and Fig. 4.1(b) respectively. The dependent voltage, E, and dependent current, J, of the small-signal model are given in (4.1) and (4.2), the capital letters denote the DC quantities.

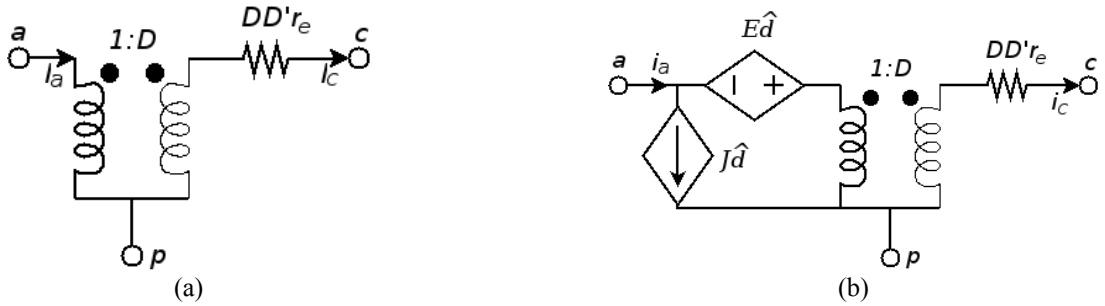
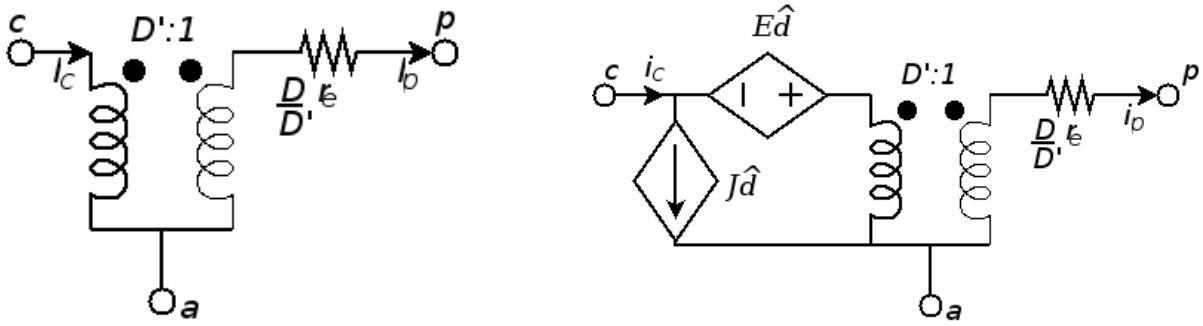


Fig. 4.1. The equivalent (a) DC and (b) small-signal PWM Vopérian switch model

$$E=\frac{1}{D}\left(V_{AP}+I_C(D-D')r_e\right) \tag{4.1}$$

$$J=I_C \tag{4.2}$$

The PWM switch models have a non-linear resistance r_e which is determined by the resistance seen from the *a* and *p* terminals of the PWM switch at high frequencies. Similarly, the DC and small-signal alternate a-PWM switch model from [71] is shown in Fig. 4.2(a) and Fig. 4.2(b) respectively. The dependent voltage, *E*, and dependent current, *J*, of the small-signal model are given in (4.3) and (4.4), the capital letters denote the DC quantities.



(a) (b)

Fig. 4.2. The equivalent (a) DC and (b) small-signal a-PWM Vopérian switch model

$$E=V_{PA}-D'r_eI_C \tag{4.3}$$

$$J=\frac{I_C}{D'} \tag{4.4}$$

The a-PWM switch model is useful for analysis of converters, such as the boost converter, that have an active element connected to ground. With the a-PWM switch model a boost converter enables DC analysis by inspection.

It is also useful to be able to reflect impedances from different ports of a transformer to another when using the Vopérian PWM switch model. The impedance reflections used in the following section will allow impedances from the bottom to be reflected to the right side, from left to right, and then from right to left. For a transformer depicted in Fig. 4.1(a), with labeled ports *a*, *c*, and *p,* an impedance seen at *c* can be moved to port *p* by (4.5). An impedance reflected from port *a* to port *c* is reflected using (4.6). Intuitively, an equivalent impedance reflected from port *c* to port *a* is given by (4.7).

$$R_{eq}=\left(\frac{N_2-N_1}{N_1}\right)^2 R \tag{4.5}$$

$$R_{eq}=\left(\frac{N_2}{N_1}\right)^2 R \tag{4.6}$$

$$R_{eq}=\left(\frac{N_1}{N_2}\right)^2 R \tag{4.7}$$

Using these, a steady state and dynamic small-signal model will be developed for the QPRSCC. The steady state model will provide an ideal conversion ratio of the input to output voltage depending on the duty ratios, D_1 and D_2, of the H-Bridge. The steady state model will also provide a steady state output impedance of the H-Bridge showing the losses due to component resistances. Small-signal models of the QPRSCC will be developed for the line-to-output voltage, the output impedance, and the control duty ratios D_1 and D_2 to output voltage. Finally, efficiency estimates of the QPRSCC will be made. Then simulations of QPRSCC regulated by the LT8705 will be performed in LTSpice.

4.1 Steady-State (DC) Analysis

Steady-state (i.e. DC) analysis of the QPRSCC can be done by replacing the switches with their respective equivalent DC PWM switch models as shown in Fig. 4.3. The buck switches are replaced by the original PWM switch model using the duty cycle D_1. The boost portion uses the alternate a-PWM model and has the independent duty cycle D_2. The switches on resistance is modeled by the resistor r_s, the inductor is given a series resistance of r_L, and the input capacitors ESR are r_{cin1} and r_{cin2}. The resistances r_{e1} and r_{e2} are found from inspection of Fig. 4.3 (at high frequency) and given in (4.8) and (4.9). Recall the resistance r_{ex} is defined by the resistance seen at the p_x and a_x terminals of the respective PWM switch model with the system inputs set to zero. At high frequency, the capacitors are considered shorts and inductors open circuit. At steady state the capacitors are considered open circuits and the inductor a short resulting in the model shown in Fig. 4.4.

$$r_{e1}\approx 2r_s+r_{cin1}\,\text{II}\,r_{cin2}\,\text{II}\,r_3 \tag{4.8}$$

$$r_{e2}=2r_s+R_2\,II\,R_{th}\approx 2r_s+R_2 \tag{4.9}$$

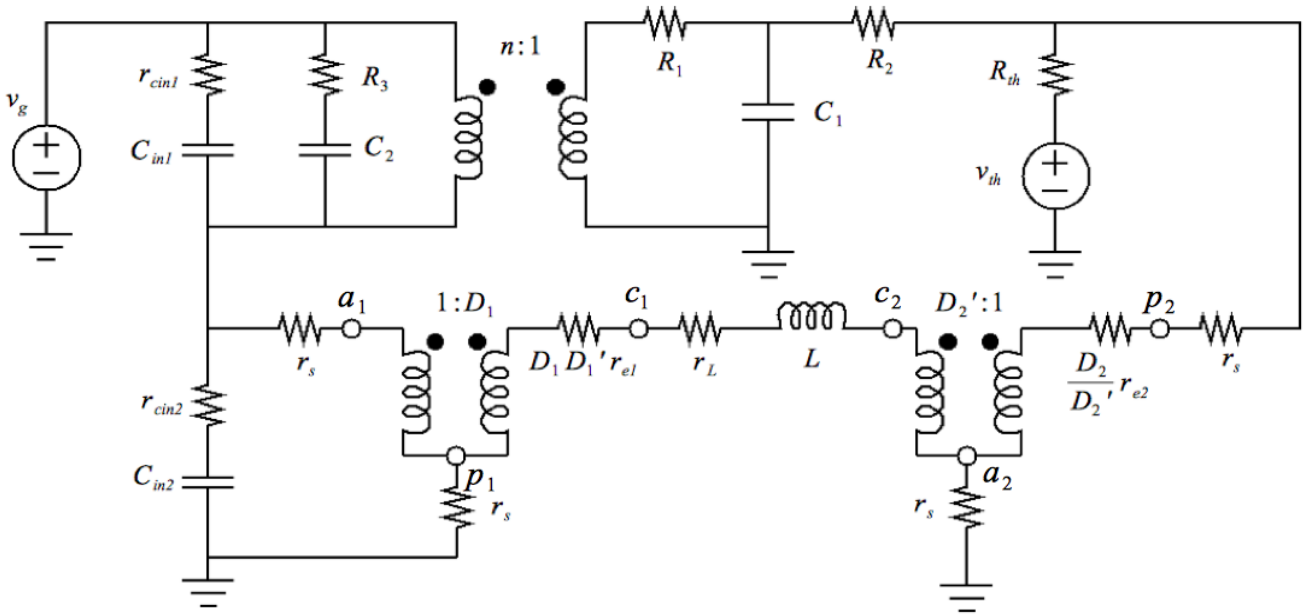


Fig. 4.3. QPRSCC with switches replaced by DC PWM switch models and MMSCC modeled by the averaged reduced-order circuit model.

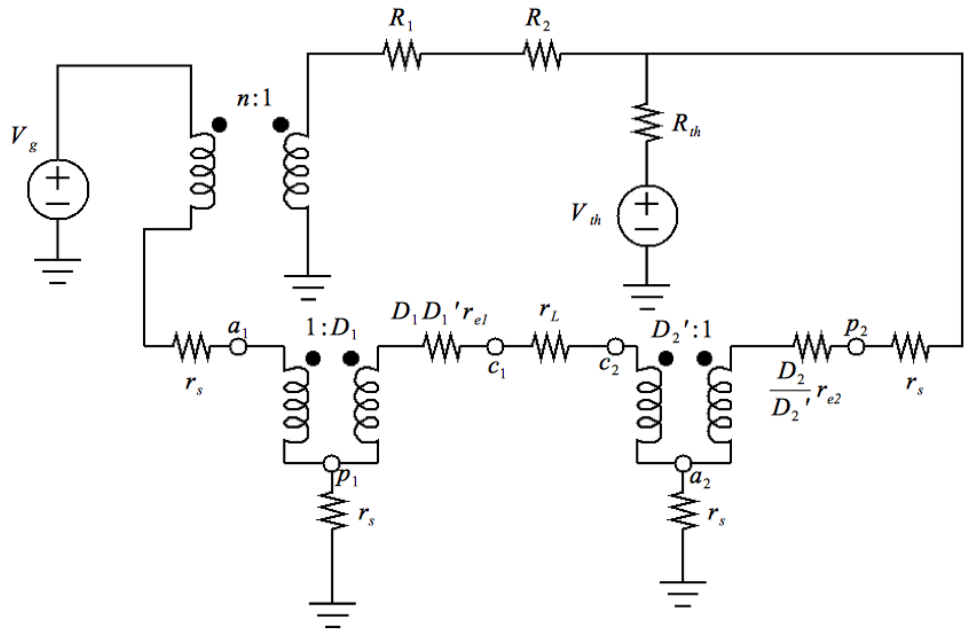


Fig. 4.4. QPRSCC modeled at steady-state

The switch resistances at terminals a_1, p_1, and a_2 can be reflected to the terminals c_1, c_1, and p_2 respectively. This results in two groups of series resistances, the first seen between c_1 and c_2 and other at p_2 . These groups can be combined into resistances r_a and r_b given in (4.25) and (4.11) respectively. The QPRSCC at steady state is now modeled as Fig. 4.5.

$$r_a = D_1 D_1' r_{e1} + r_L + (D_1^2 + D_1'^2) r_s \tag{4.10}$$

$$r_b = \frac{D_2}{D_2'} r_{e2} + \left(1 + \left(\frac{D_2}{D_2'}\right)^2\right) r_s \tag{4.11}$$

The DC currents, I_{c1} and I_{c2}, and the DC voltages, V_{PA2} and V_{AP1}, are needed for small-signal analysis. From inspection of Fig. 4.4, the currents I_{c1} and I_{c2} are equal and can be denoted simply as I_c. The current I_c is also the inductor current and can be related to the input current or the H-bridge output current, I_{pwm}, as in (4.12). The voltages V_{PA2} and V_{AP1} are defined as (4.13) and (4.14).

$$I_{c1} = I_{c2} = I_c = \frac{I_{in}}{D_1} = \frac{I_{pwm}}{D_2'} \tag{4.12}$$

$$V_{PA2} = -r_s I_c + 2 r_s I_{pwm} + V_o \tag{4.13}$$

$$V_{AP1} = V_g - n\left(V_o + I_{sc}(R_1 + R_2)\right) - 2 r_s I_{in} \tag{4.14}$$

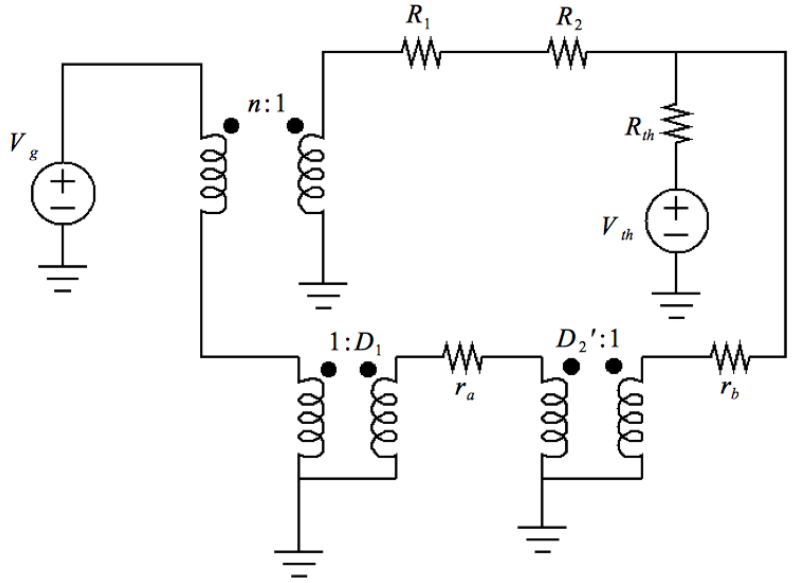


Fig. 4.5. QPRSCC modeled at steady state with combined resistances r_a and r_b

By reflecting r_a to the right side of both DC transformers, Fig. 4.5 and combining the transformers, the QPRSCC in steady state can be modeled by the circuit shown in Fig. 4.6. It is two transformers whose inputs are connected in series and with paralleled outputs, one representing the conversion ratio of the MMSCC, n, and the other of the H-bridge dependent on the duty cycles of the buck and boost section, D_1 and D_2.

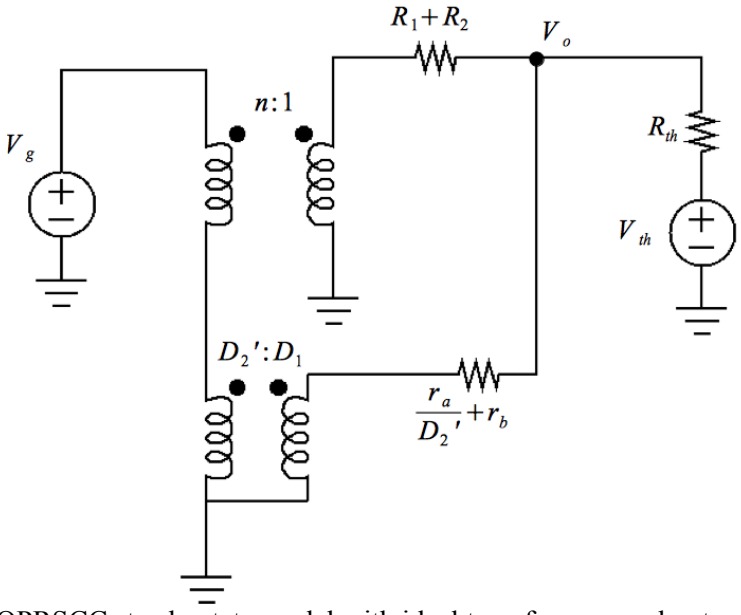


Fig. 4.6. QPRSCC steady-state model with ideal transformers and output resistance

The steady-state output resistances of the MMSCC and H-bridge, r_{sc} and r_{pwm}, can be found by inspection and are (4.15) and (4.16) respectively.

$$r_{sc}=R_1+R_2 \tag{4.15}$$

$$r_{pwm}=\frac{r_a}{D_2'}+r_b \tag{4.16}$$

The DC conversion ratio can be defined from analysis of Fig. 4.6. The input voltage Vg can be expressed as (4.17) and input current can be written as (4.18). Substituting (4.18) into (4.17) gives the input voltage in terms of the duty cycles, output voltage, and the Thévenin voltage (4.19).

$$V_g=I_{in}\left(n^2 r_{sc}+\left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right)+\left(n+\frac{D_2'}{D_1}\right)V_o \tag{4.17}$$

$$I_{in}=\left(\frac{V_o-V_{th}}{R_{th}}\right)\frac{1}{\left(n+\frac{D_2'}{D_1}\right)} \tag{4.18}$$

$$V_g=\left(\frac{V_o-V_{th}}{R_{th}}\right)\frac{1}{\left(n+\frac{D_2'}{D_1}\right)}\left(n^2 r_{sc}+\left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right)+\left(n+\frac{D_2'}{D_1}\right)V_o \tag{4.19}$$

The ideal conversion ratio M is found either by inspection of Fig. 4.6 ignoring output resistances or by solving (4.19) with the output resistances set as zero. The ideal conversion ratio for the QPRSCC is (4.20).

$$M = \frac{1}{\left(n + \frac{D_2'}{D_1}\right)} = \frac{D_1}{n D_1 + D_2'} \tag{4.20}$$

Rewriting (4.19) with M gives (4.21) which can be solved for the output voltage in terms of the system inputs, the input voltage and the Thévenin voltage as in (4.23).

$$V_g = V_o\left[M\left(\frac{1}{R_{th}}\right)\left(n^2 r_{sc} + \left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right) + \frac{1}{M}\right] - \frac{V_{th}}{R_{th}} M\left(n^2 r_{sc} + \left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right) \tag{4.21}$$

$$V_g + \frac{V_{th}}{R_{th}} M\left(n^2 r_{sc} + \left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right) = V_o\left[M\left(\frac{1}{R_{th}}\right)\left(n^2 r_{sc} + \left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right) + \frac{1}{M}\right] \tag{4.22}$$

$$V_o = \frac{1}{\left[M\left(\frac{1}{R_{th}}\right)\left(n^2 r_{sc} + \left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right) + \frac{1}{M}\right]} V_g + \frac{M\left(n^2 r_{sc} + \left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right)}{\left[M\left(n^2 r_{sc} + \left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right) + \frac{R_{th}}{M}\right]} V_{th} \tag{4.23}$$

Ignoring the Thévenin voltage, the DC input to output conversion ratio can be derived as the ideal conversion ratio multiplied against the conduction loss term as in (4.26).

$$\frac{V_o}{V_g} = \frac{1}{\left[M\left(\frac{1}{R_{th}}\right)\left(n^2 r_{sc} + \left(\frac{D_2'}{D_1}\right)^2 r_{pwm}\right) + \frac{1}{M}\right]} \tag{4.24}$$

$$\frac{V_o}{V_g} = M\left(\frac{1}{\left[M^2\left(n^2 \frac{r_{sc}}{R_{th}} + \left(\frac{D_2'}{D_1}\right)^2 \frac{r_{pwm}}{R_{th}}\right) + 1\right]}\right) \tag{4.25}$$

$$\frac{V_o}{V_g} = M\left(\frac{1}{\left(\frac{n D_1^{\,2}}{(n D_1 + D_2')^2}\right)\frac{r_{sc}}{R_{th}} + \left(\frac{D_2'^2}{(n D_1 + D_2')^2}\right)\frac{r_{pwm}}{R_{th}} + 1}\right) \tag{4.26}$$

Any DC operating point can be modeled using (4.26). By ignoring V_{th} (setting it to zero), the load line characteristics are removed but can adequately by modeled by holding the input voltage constant and varying R_{th}. By eliminating one of the system inputs in the DC model, the equations for I_C , V_{PA2}, and V_{AP1} are simplified, allowing for simplified use in the small-signal analysis in the following section.

With V_{th} = 0, the input current is (4.27) and the current I_C, equivalent to the inductor current, previously defined by (4.12) can be written as (4.24).

$$I_{in}=\left(\frac{V_o}{R_{th}}\right)M \tag{4.27}$$

$$I_c=\frac{M}{R_{th}D_1}V_o=\frac{1}{R_{th}}\left(\frac{V_o}{n\,D_1+D_2'}\right) \tag{4.28}$$

With the current I_C defined the currents I_{pwm} and I_{in} can then be replaced in (4.13) and (4.14) to give (4.29) and (4.22) respectively.

$$V_{PA2}=(2D_2'-1)r_s I_c+V_o \tag{4.29}$$

$$V_{API}=V_g+(n^2(R_1+R_2)-2r_s-\frac{n\,R_{th}}{M})\frac{M}{R_{th}}V_o \tag{4.30}$$

4.2 Small-Signal Analysis

Small-signal analysis of the Quasi-Parallel Regulated Switched-Capacitor Converter (QPRSCC) can also be done by employing the Vopérian PWM switch model. Depending on the characteristic in question, e.g. output impedance or control-to-output, the equivalent DC PWM model or the small-signal PWM switch model can provide a simple circuit analysis. For the line-to-output, output and input impedances, the DC PWM switch models shown in Fig. 4.1(a) and Fig. 4.2(a) of section 4.1, will be used for analysis. These analyses hold the duty cycle constant so the dependent voltage and current in the small-signal PWM switch models disappear as $\tilde{d}=0$.

Regardless of which PWM switch model is employed to provide the dynamic characteristics, the impedances of the switched-capacitor converter (SCC) and the H-bridge will all be reflected to one side of their respective DC transformers. Manipulating the circuit results in either one or two DC transformers, some small signal voltage and/or current source, and impedance networks. Such circuits can be readily solved with matrix analysis and two port impedance network models. For the analysis the QPRSCC small-signal characteristics, two port theory will be utilized. A brief overview of two port theory and various models will be covered first in section 4.2.1. Analysis of the line-to-output voltage, output impedance, input impedance, and lastly the control-to-output voltage small-signal characteristics will be investigated in their own sections. Examination of the control-to-output voltage for each duty cycle of the H-bridge will be discussed in their own subsection. H-bridge control strategies, outlined in

[64] and [65], will proven viable in the control of the QPRSCC by comparing the control-to-output characteristics of a H-bridge DC/DC converter to one that is in a quasi-parallel configuration with an unregulated SCC.

4.2.1 Two Port Theory

For a network of linear passive elements such as resistors, inductors, and capacitors where only the behavior at a pair of specific nodes are of interest, utilizing two port theory is appropriate. Given a pair of nodes and some linear passive network, as shown in Fig. 4.7, the network can be described in terms of a set of parameters; commonly these are Impedance, Admittance, Transmission Line (ABCD), and Hybrid parameters. A useful property of the ABCD parameters is that they can be found for a complex impedance network easily by combining the parameters of the individual impedance elements. An overview of the four aforementioned parameters and a method for converting the ABCD parameters to impedance, admittance, or hybrid parameters will be covered at the end of this section.

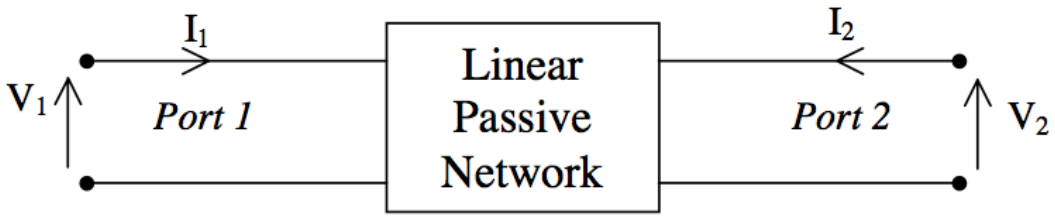


Fig. 4.7. A two port model with a general linear passive network

The impedance parameters provide the relation between the voltages and the currents of the network. The impedance parameter matrix for the two port model in Fig. 4.7 is given as (4.31).

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{4.31}$$

The parameters z_{11}, z_{12}, z_{21}, and z_{22} are found from analysis of the impedance network at different ports while one of the currents is set to zero as defined in (4.32).

$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} \quad z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} \quad z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} \quad z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} \tag{4.32}$$

The admittance parameters matrix for the two port model in Fig. 4.7 is (4.33). The elements of the matrix are found in a similar fashion as the impedance parameters, but by shorting the port (zero voltage) instead of open circuit ports (zero currents).

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{4.33}$$

The transmission line (ABCD) parameters represent the relation between the input to the output of the a two port network as defined in Fig. 4.8. Unlike the other parameters, because of the input to output relation, the ABCD parameters are defined for the output current leaving the port instead of entering it.

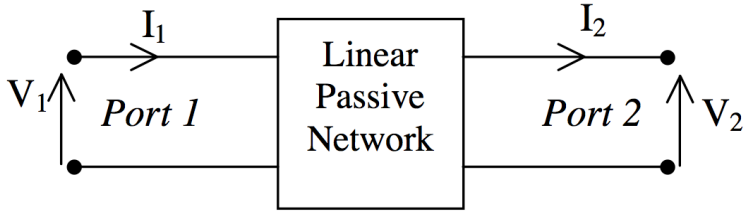


Fig. 4.8. A two port model defined for ABCD parameters

The ABCD parameters for the two port model in Fig. 4.8 are written as (4.34). The parameters A, B, C, and D are defined by the network where port 2 is either a short circuit or an open circuit.

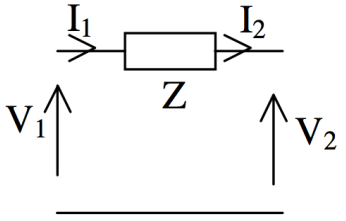
$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{4.34}$$

The hybrid parameters are defined for the two port model presented in Fig. 4.7 where currents flow into the ports. Hybrid parameters give a mixed relation between the voltages and currents as in (4.35).

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \tag{4.35}$$

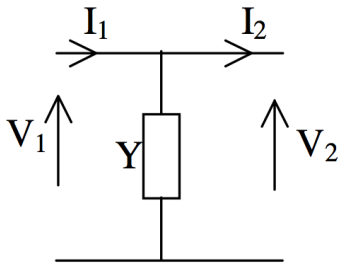
A. Cascaded ABCD Parameters

The ABCD parameters of complex impedance networks can easily be found from the ABCD parameters of the individual impedances. For a series impedance, the corresponding ABCD parameters are shown in Fig. 4.9(a). A parallel admittance and the corresponding ABCD parameters are shown in Fig. 4.9(b).



$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}$$

(a)



$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}$$

(b)

Fig. 4.9. ABCD parameters for a single (a) series impedance and (b) parallel admittance

As combinations of these basic impedances are cascaded the cumulative ABCD parameters are simply the multiplication of the individual ABCD parameters matrices. For example, a π-network shown in Fig. 4.10, the ABCD parameters can be found from cascading the individual impedances' ABCD parameters shown in (4.36).

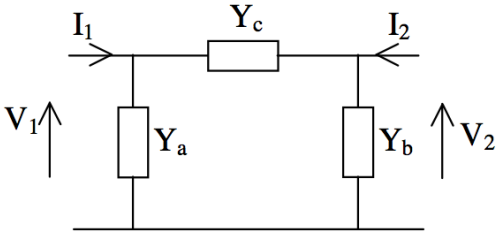


Fig. 4.10. π-network of admittances

$$ABCD_{\pi} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y_a & 1 \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{Y_c} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_b & 1 \end{bmatrix} \tag{4.36}$$

B. Parameter Transformations

In the following work the impedance networks encountered in the analysis of the QPRSCC small-signal behavior will be initially described using ABCD parameters. For some applications the voltage and current relations are best described by Impedance, Admittance, or Hybrid parameters. In such situations the Impedance, Admittance, and Hybrid parameters can be defined in terms of the ABCD parameters by (4.37), (4.38), and (4.39) respectively.

$$Z = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} \frac{A}{C} & \frac{AD-BC}{B} \\ \frac{1}{C} & \frac{D}{C} \end{bmatrix} \tag{4.37}$$

$$Y=\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}=\begin{bmatrix} \frac{D}{B} & \frac{BC-AD}{B} \\ \frac{-1}{B} & \frac{A}{B} \end{bmatrix} \tag{4.38}$$

$$H=\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}=\begin{bmatrix} \frac{B}{D} & \frac{BC-AD}{D} \\ \frac{-1}{D} & \frac{C}{D} \end{bmatrix} \tag{4.39}$$

4.2.2 Open Loop Line-to-Output Voltage Transfer Function

A. Derivation of Line-to-Output Voltage Transfer Function

To find the small-signal line voltage-to-output voltage transfer function, both H-bridge duty cycles are held constant, i.e. no small-signal duty cycle variations, and a perturbation is considered on the line voltage. The average reduced order SCC circuit model from section 3.3.2 will be used along with the DC PWM switch model resulting in Fig. 4.11. The output is simply modeled as a resistive load, where the output resistance R_{th} can be varied to simulate different DC load operating points. The resistances r_{e1} and r_{e2} are the same as defined previously in section 4.1 (as (4.8) and (4.9)) but are repeated here in (4.40)and (4.41) for convenience

$$r_{e1} \approx 2r_s + r_{cin1} \,\text{II}\, r_{cin2} \,\text{II}\, r_3 \tag{4.40}$$

$$r_{e2} = 2r_s + R_2 \,II\, R_{th} \approx 2r_s + R_2 \tag{4.41}$$

The switch resistances at terminals a_1, p_1, and a_2 can be reflected to terminals c_1, c_1, and p_2 respectively and then combined with neighboring resistances in series. The capacitors C_{in1} and C_2, and their corresponding series resistance can be reflected across the SCC transformer. The input capacitor, C_{in2}, and its series resistance can be reflected across the transformer representing the buck portion of the H-bridge. This gives the small-signal circuit model in Fig. 4.12. The lumped resistances r_a and r_b are (4.42)and (4.43) respectively.

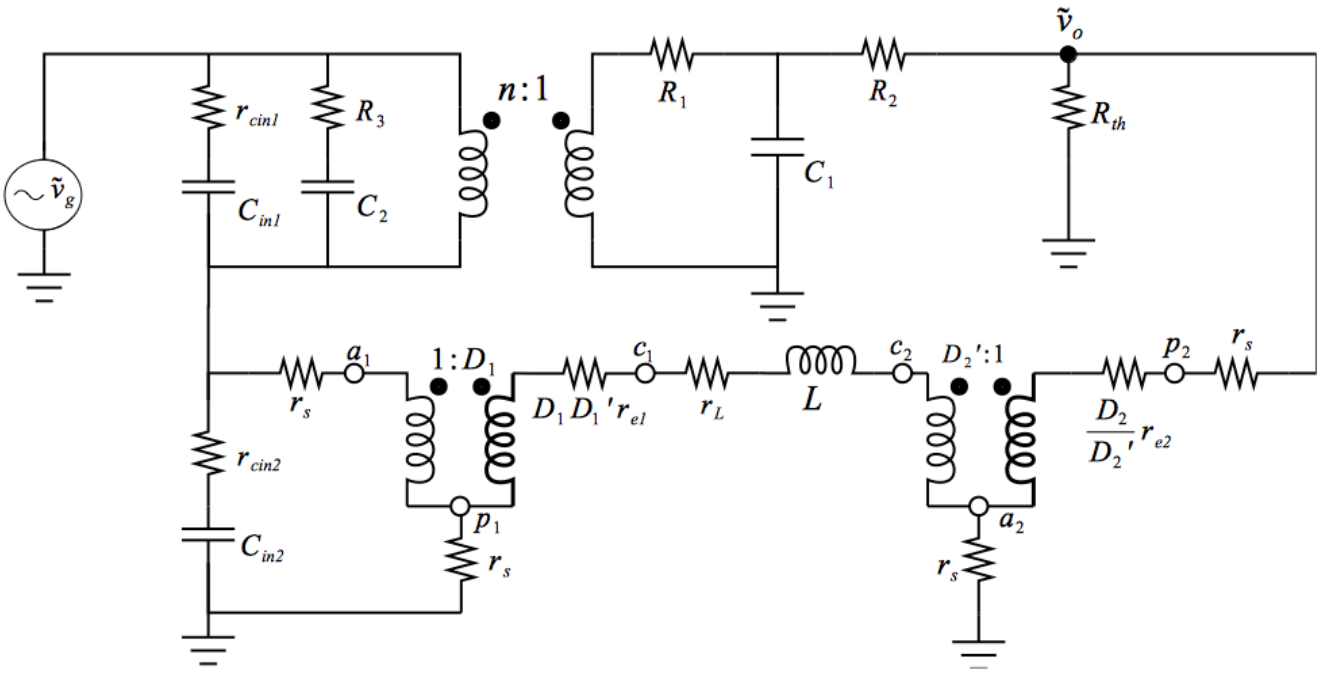


Fig. 4.11. QPRSCC modeled with the averaged small-signal SCC circuit model and the DC PWM switch model for small-signal line-to-output voltage model.

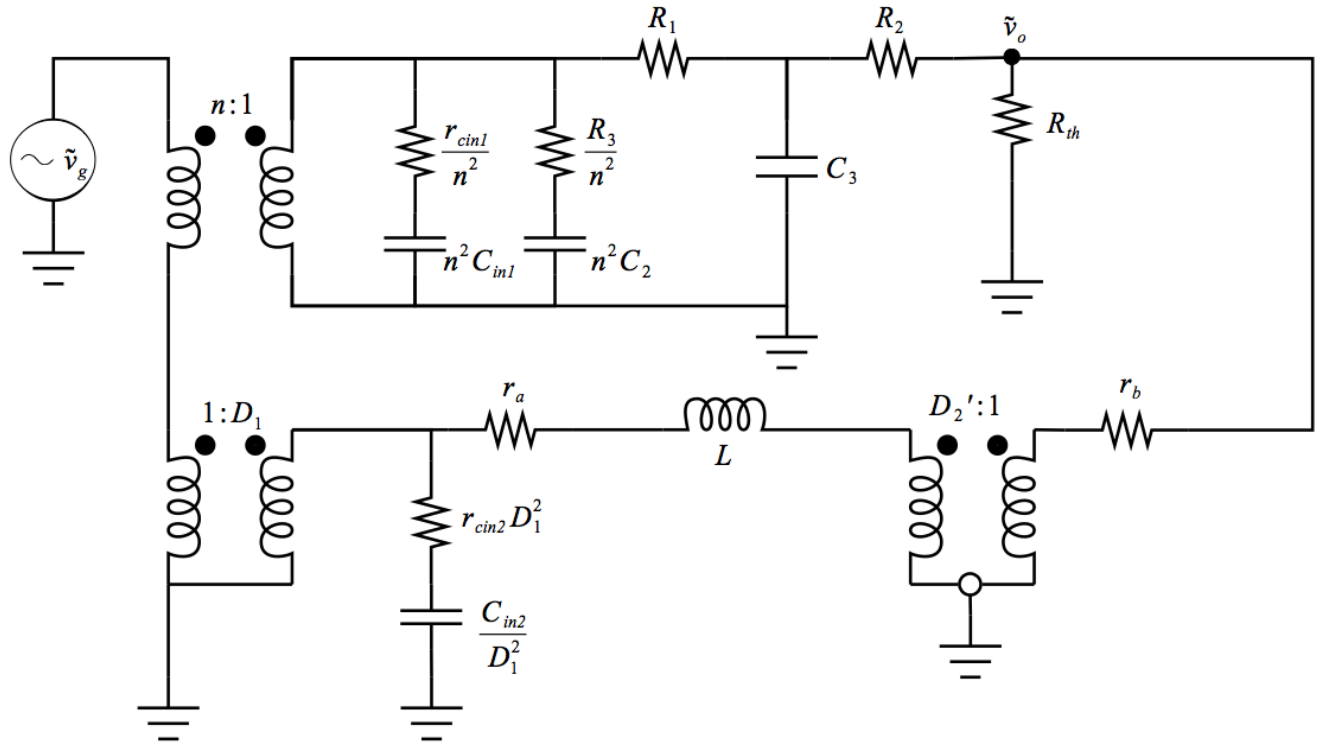


Fig. 4.12. The input capacitors are reflected across their corresponding DC transformers and the resistances at p_1 and a_2 are reflected to their right sides for QPRSCC small-signal line-to-output voltage analysis.

$$r_a = D_1 D_1' r_{e1} + r_L + (D_1^2 + D_1'^2) r_s \tag{4.42}$$

$$r_b = \frac{D_2}{D_2'} r_{e2} + \left(1 + \left(\frac{D_2}{D_2'}\right)^2\right) r_s \tag{4.43}$$

For clarity define $Z_{cin1} = r_{cin1} + \frac{1}{s C_{in1}}$, $Z_{cin2} = r_{cin2} + \frac{1}{s C_{in2}}$, and $Z_{C2} = R_3 + \frac{1}{s C_2}$. The inductor, resistance r_a, and the impedance Z_{cin2} can be reflected to the right side of the transformer, with turns ratio $D_2' : 1$, representing the boost portion of the H-bridge thereby allowing the buck and boost transformers to be joined as a single transformer with a turns ratio of $D_2' : D_1$. This results in the circuit shown in Fig. 4.13. There are two transformers, one representing the SCC ideal conversion ratio with turns ratio $n:1$, the other representing the H-bridge conversion ratio with turns ratio $D_2' : D_1$.

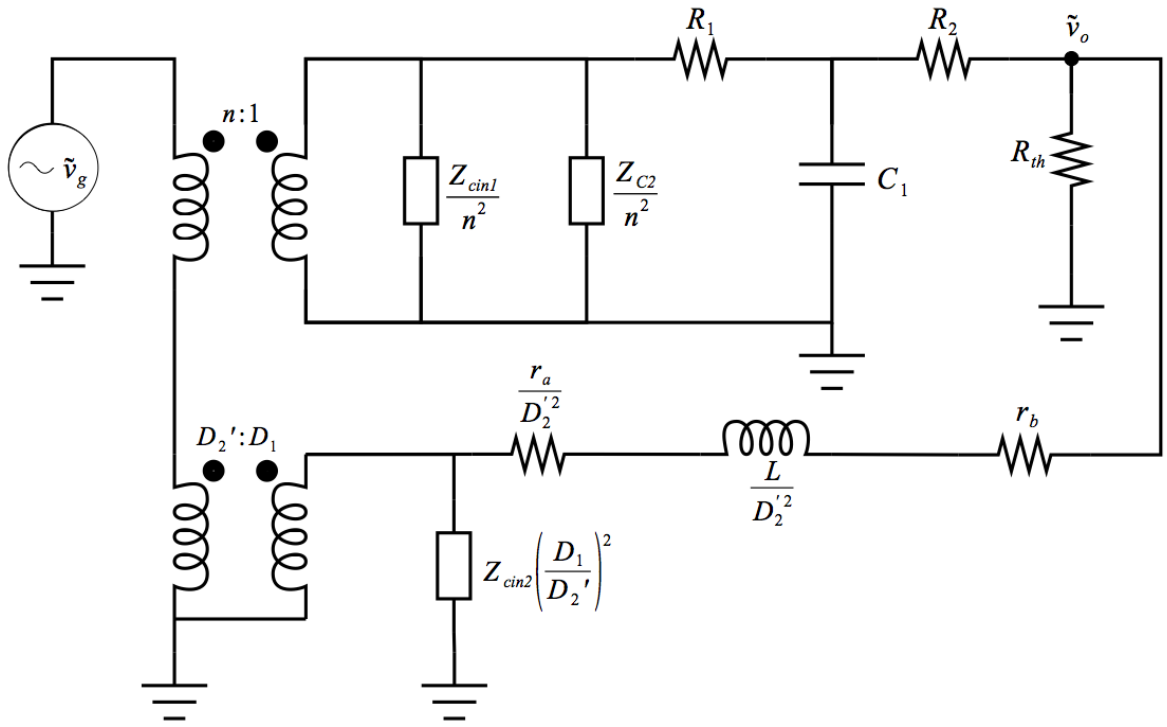
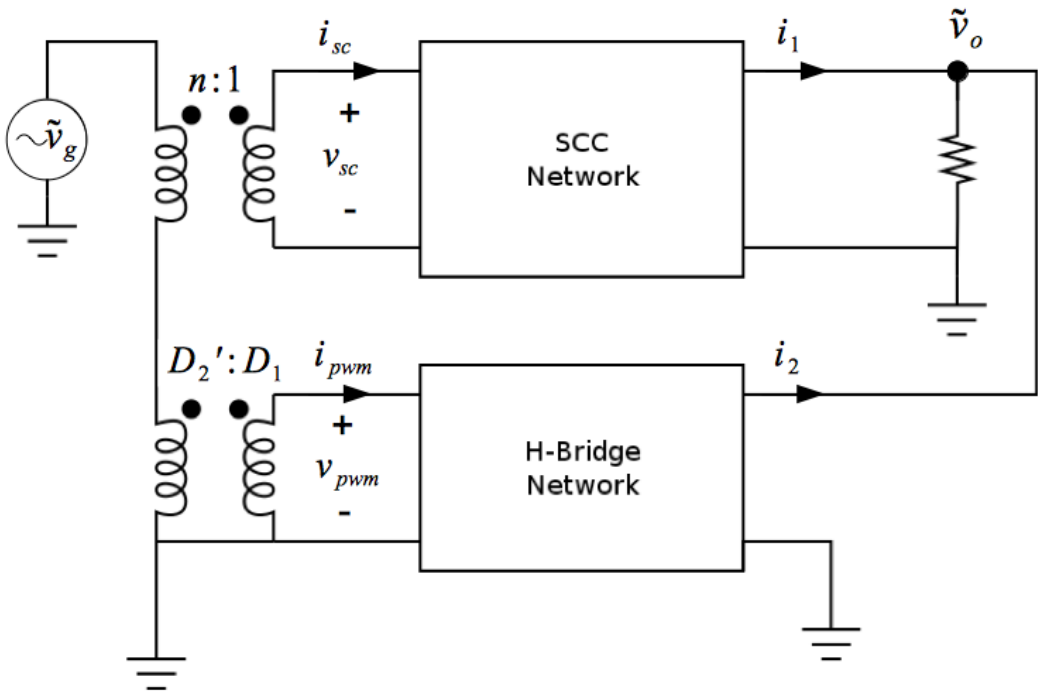
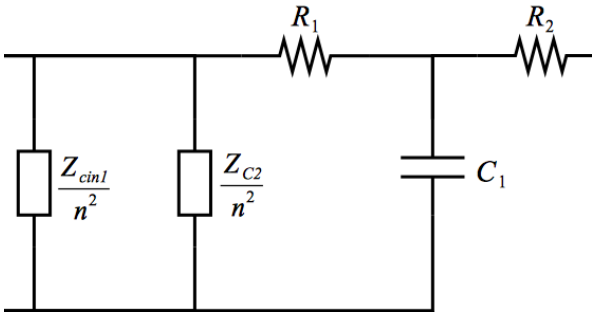


Fig. 4.13. Reflecting impedances allows for the H-Bridge to be reduced to a single transformer and an impedance network, enabling use of a two port model for the QPRSCC line-to-output voltage analysis.

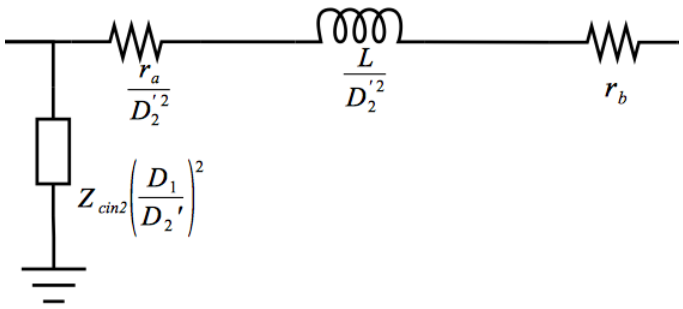
There are two transformers, one representing the SCC ideal conversion ratio with turns ratio $n:1$, the other representing the H-bridge conversion ratio with turns ratio $D_2' : D_1$. These are connected in series and each has a linear impedance network connected to their respective outputs. The SCC impedance network and the H-bridge impedance network, shown in Fig. 4.14(b) and Fig. 4.14(c), can be replaced with their two port impedance network models giving a simple circuit to derive the line-to-output voltage transfer function as shown in Fig. 4.14(a).



(a) line-to-output voltage model with two port networks



(b) SCC impedance network



(c) H-bridge impedance network

Fig. 4.14. The QPRSCC (a)line-to-output voltage small-signal model with two port impedance networks one for the (b) SCC impedance network and the (c) H-bridge impedance network.

The governing equations from the circuit model in Fig. 4.14(a) are (4.44) through (4.48).

$$\tilde{v}_g = n\,v_{sc} + \frac{D_2'}{D_1}v_{pwm} \tag{4.44}$$

$$0 = \frac{i_{sc}}{4} - \frac{D_1}{D_2'}i_{pwm} \tag{4.45}$$

$$0 = \tilde{v}_o - R_{th}(i_1 + i_2) \tag{4.46}$$

$$\begin{bmatrix} v_{pwm} \\ i_{pwm} \end{bmatrix} = ABCD_{pwm}\begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.47}$$

$$\begin{bmatrix} v_{sc} \\ i_{sc} \end{bmatrix} = ABCD_{sc} \begin{bmatrix} v_o \\ i_1 \end{bmatrix} \tag{4.48}$$

The equations can be written together as a system of linear equations as in (4.49).

$$\begin{bmatrix} v_g \\ 0 \end{bmatrix} = \begin{bmatrix} n & 0 \\ 0 & \frac{1}{n} \end{bmatrix} \begin{bmatrix} v_{sc} \\ i_{sc} \end{bmatrix} + \begin{bmatrix} \frac{D_2'}{D_1} & 0 \\ 0 & \frac{-D_1}{D_2'} \end{bmatrix} \begin{bmatrix} v_{pwm} \\ i_{pwm} \end{bmatrix} \tag{4.49}$$

Substituting in (4.47) and (4.48) gives (4.50) which can be further reduced into a more compact form of (4.52).

$$\begin{bmatrix} v_g \\ 0 \end{bmatrix} = \begin{bmatrix} n & 0 \\ 0 & \frac{1}{n} \end{bmatrix} ABCD_{sc} \begin{bmatrix} v_o \\ i_1 \end{bmatrix} + \begin{bmatrix} \frac{D_2'}{D_1} & 0 \\ 0 & \frac{-D_1}{D_2'} \end{bmatrix} ABCD_{pwm} \begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.50}$$

$$\begin{bmatrix} v_g \\ 0 \end{bmatrix} = \begin{bmatrix} n A_{sc} & n B_{sc} \\ \frac{C_{sc}}{n} & \frac{D_{sc}}{n} \end{bmatrix} \begin{bmatrix} v_o \\ i_1 \end{bmatrix} + \begin{bmatrix} \frac{D_2'}{D_1} A_{pwm} & \frac{D_2'}{D_1} B_{pwm} \\ \frac{-D_1}{D_2'} C_{pwm} & \frac{-D_1}{D_2'} D_{pwm} \end{bmatrix} \begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.51}$$

$$\begin{bmatrix} v_g \\ 0 \end{bmatrix} = \begin{bmatrix} \left(n A_{sc} + \frac{D_2'}{D_1} A_{pwm} \right) & n B_{sc} & \frac{D_2'}{D_1} B_{pwm} \\ \left(\frac{C_{sc}}{n} + \frac{-D_1}{D_2'} C_{pwm} \right) & \frac{D_{sc}}{n} & \frac{-D_1}{D_2'} D_{pwm} \end{bmatrix} \begin{bmatrix} v_o \\ i_1 \\ i_2 \end{bmatrix} \tag{4.52}$$

The remaining equation (4.46) can be added to the system to make it a square matrix and a solvable system (4.53).

$$\begin{bmatrix} v_g \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \left(n A_{sc} + \frac{D_2'}{D_1} A_{pwm} \right) & n B_{sc} & \frac{D_2'}{D_1} B_{pwm} \\ \left(\frac{C_{sc}}{n} + \frac{-D_1}{D_2'} C_{pwm} \right) & \frac{D_{sc}}{n} & \frac{-D_1}{D_2'} D_{pwm} \\ 1 & -R_{th} & -R_{th} \end{bmatrix} \begin{bmatrix} v_o \\ i_1 \\ i_2 \end{bmatrix} \tag{4.53}$$

Equation (4.53) is of the form of **Y**=**AX** and both sides can be premultiplied by $\mathbf{A}^{-1}$, the inverse of **A**, to get (4.54).

$$\begin{bmatrix} v_o \\ i_1 \\ i_2 \end{bmatrix} = \mathbf{A^{-1}} \begin{bmatrix} v_g \\ 0 \\ 0 \end{bmatrix} \tag{4.54}$$

where

$$A^{-1} = \begin{bmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{bmatrix} = \begin{bmatrix} \left(n\,A_{sc} + \dfrac{D_2'}{D_1} A_{pwm} \right) & n\,B_{sc} & \dfrac{D_2'}{D_1} B_{pwm} \\ \left(\dfrac{C_{sc}}{n} + \dfrac{-D_1}{D_2'} C_{pwm} \right) & \dfrac{D_{sc}}{n} & \dfrac{-D_1}{D_2'} D_{pwm} \\ 1 & -R_{th} & -R_{th} \end{bmatrix}^{-1} \tag{4.55}$$

The line-to-output transfer function is then simply the element α_{11} of $\mathbf{A}^{-1}$.

$$\frac{\tilde{v}_o}{\tilde{v}_g} = \alpha_{11} \tag{4.56}$$

The two remaining steps are to solve for the ABCD parameters of the SCC and H-bridge impedance networks. The parameters are found by viewing each network as a set of cascaded impedance networks. The SCC impedance network, shown in Fig. 4.14(b), gives ABCD parameters as (4.57).

$$ABCD_{sc} = \begin{bmatrix} 1 & 0 \\ \dfrac{n^2}{Z_{cin1}} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \dfrac{n^2}{Z_{C2}} & 1 \end{bmatrix} \begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ s\,C_1 & 1 \end{bmatrix} \begin{bmatrix} 1 & R_2 \\ 0 & 1 \end{bmatrix} \tag{4.57}$$

The H-bridge impedance network, shown in Fig. 4.14(c), has ABCD parameters given by (4.58).

$$ABCD_{sc} = \begin{bmatrix} 1 & 0 \\ \left(\dfrac{D_2'}{D_1} \right)^2 \dfrac{1}{Z_{cin2}} & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_{ser} \\ 0 & 1 \end{bmatrix} \tag{4.58}$$

where $Z_{ser} = \dfrac{r_a}{(D_2')^2} + \dfrac{s\,L}{(D_2')^2} + r_b$

B. Analysis of Open Loop Line-to-Output Voltage Transfer Function

In Fig. 4.15, the frequency response of the QPRSCC input to output voltage transfer function is plotted for three different operating points. The three operating points all are 12V output voltage and 12V on the H-Bridge, but the MMSCC operates as a 2:1, 3:1, and 4:1 corresponding to QPRSCC input voltages of 36V, 48V, and 60V. For the frequency response in Fig. 4.15, the MMSCC and H-Bridge are modeled with their designated parameters used in Chapter 3. This only leaves selection of the input capacitors

C_{in1} and C_{in2}, corresponding to MMSCC and H-Bridge input capacitors. As the QPRSCC input voltage increases the resonance peak decreases in magnitude and at slightly lower frequency. At low voltages there is a pole-zero cancellation and the overall behavior is somewhat first order (ignoring the resonant peak). At higher voltages the pole and zero separate leading to a steeper slope past the resonance point until reaching the zero. The interaction between the moving poles and zero is more pronounced at high voltages evident in the phase response of the input to output voltage transfer function but certainly not problematic.

Inspection of the frequency response of QPRSCC open-loop line-to-output voltage transfer function reveals it is a combination of the MMSCC and H-Bridge line-to-output voltage transfer functions as shown in Fig. 4.15. The MMSCC line-to-output transfer function frequency response is approximately that of a first order filter as discussed in section 3.2.2. The H-bridge exhibits the common LC second order filter as shown in section 3.2.3. The resonance peak of the H-Bridge (created by the LC filter) is seen as well in the QPRSCC. Variations to the H-Bridge inductor or the output capacitor will shift the resonance peak while, variations in the output capacitance and switching capacitance will affect the bandwidth of the first order filter behavior of the MMSCC.

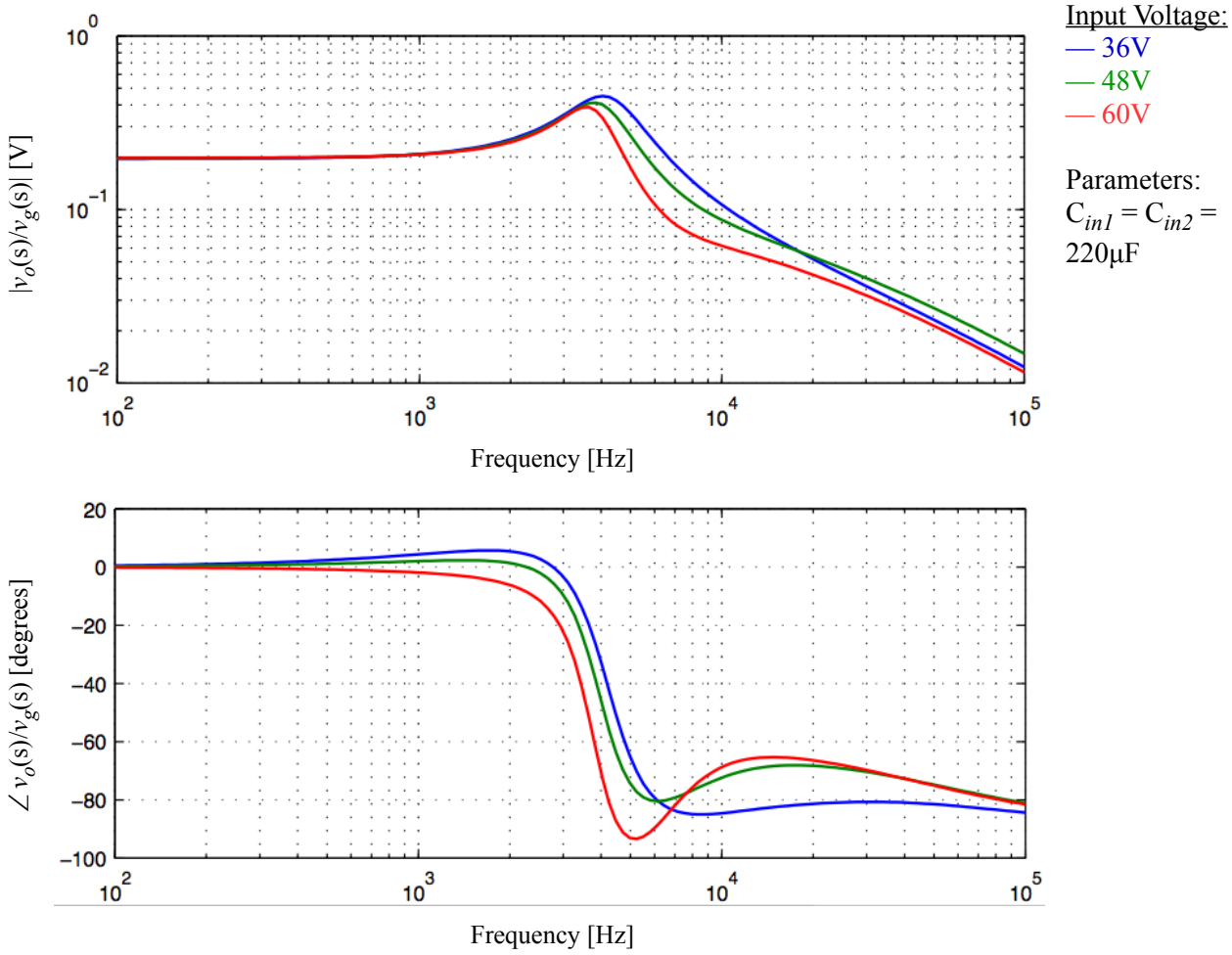


Fig. 4.15. Frequency response of the QPRSCC line-to-output voltage with 12V on the H-Bridge and the MMSCC with input voltages of 36V, 48V, and 60V operating in 2:1, 3:1, and 4:1 respectively.

A pole zero map of the QPRSCC (Fig. 4.16) line-to-output voltage transfer function at input voltages 36V, 48V, and 60V reveal that all poles and zeros are in the right half plane (RHP). There are a pair of complex poles,-1.2 ± 4.05 kHz, which correspond to the resonant peak and do not shift significantly. A pair of complex zeros move closer to the complex poles as the input voltage increases. There also a pole and zero that both migrate closer to zero along the real axis in the tens of kHz range. These correspond the interactions seen past the resonant peak in the magnitude of the QPRSCC line-to-output transfer function frequency response in Fig. 4.15.

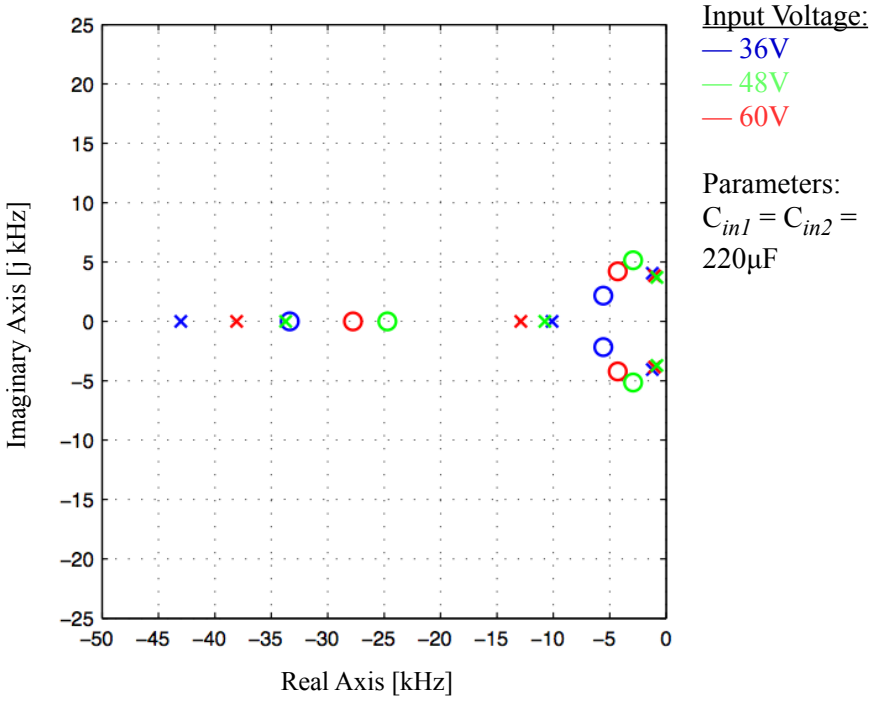


Fig. 4.16. Pole Zero map of the QPRSCC line-to-output voltage transfer function

The frequency response of the QPRSCC line-to-output voltage transfer function is plotted in Fig. 4.17 for input voltages of 4V, 12V, and 16V for the H-Bridge, (over the entire QPRSCC input voltage range). The overall behavior is similar across the input voltage range with minimal movement of the resonant peak (withing the range of 3kHz to 5kHz), with some additional variation in the frequency response just past the resonant peak. The 2nd order resonant behavior is most pronounced when the MMSCC has a conversion ratio of 4:1 and when the H-Bridge is operating in boost mode (input voltage of 4V). The frequency response is closest to first order in nature when the H-Bridge is in buck mode with 16V input to the H-Bridge, especially with the MMSCC operating at 3:1 or 2:1. At low frequencies, changes in the line-to-output voltage transfer function depend only on the voltage seen by the H-Bridge. The conversion ratio of the MMSCC is not a factor in the frequency response at low frequencies only at frequencies just past the resonant frequency.

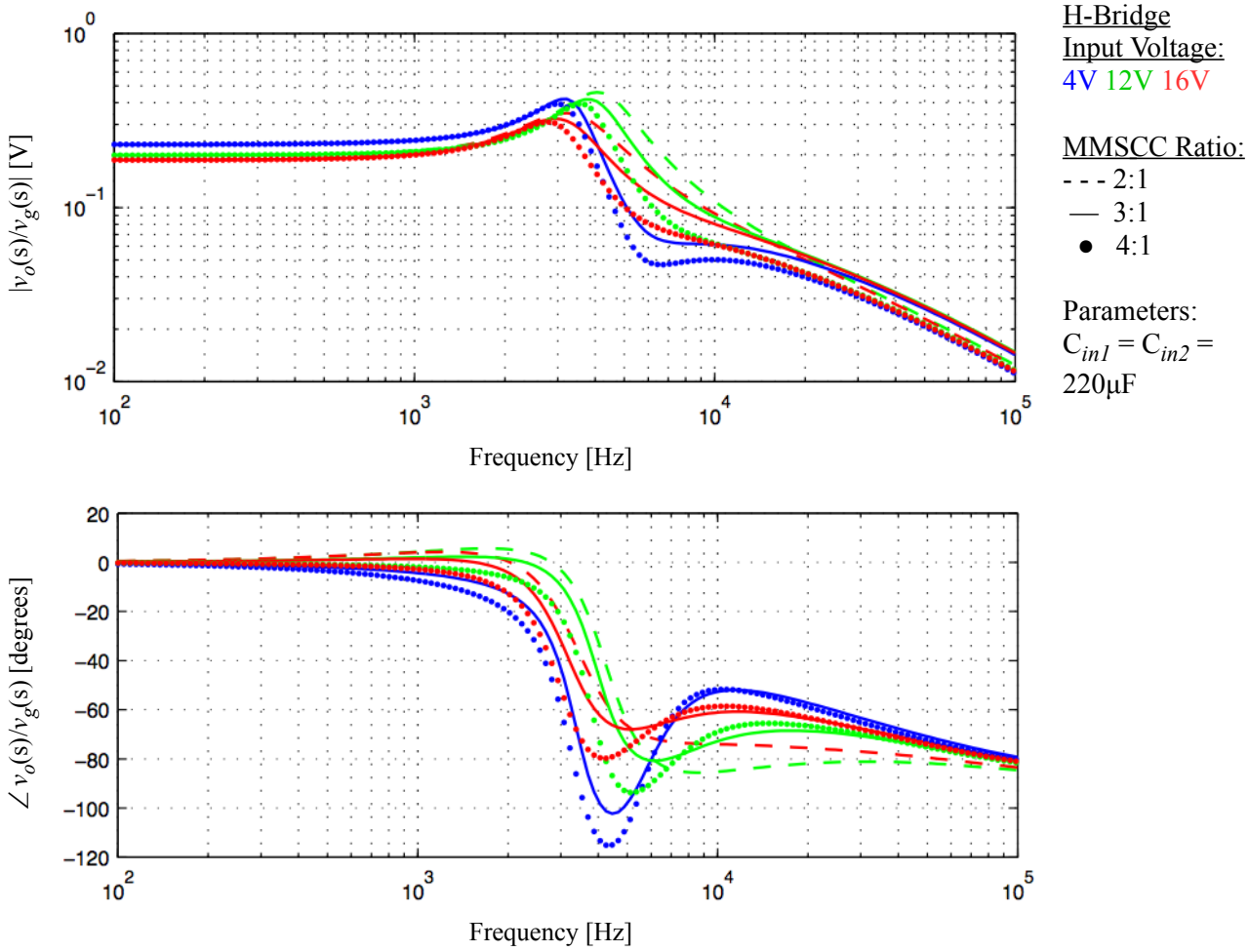


Fig. 4.17. Frequency response of the QPRSCC line-to-output voltage at selected input voltages.

The pole zero map of the QPRSCC line-to-output voltage transfer function (Fig. 4.16) revealed a pair of complex poles, from the H-Bridge, that lead to 2nd order effects in the frequency response. Depending on the input voltage of the H-Bridge and the conversion ratio of the MMSCC, these 2nd order effects are reduced due to a pair of complex zeros arising from the natural feedback of the quasi-parallel configuration. Despite the resonant peak there is only a phase delay of 90 degrees and roughly -20dB/decade decrease in magnitude past the resonant frequency of 3-5kHz. This behavior equates to a first order system with a bandwidth of 3-5kHz. When the H-Bridge is in boost mode (especially with a high step up conversion ratio) the 2nd order effects are more evident.

The inductor, output capacitance, MOSFETs, and switching capacitors capacitance have been selected and together determine the resonant frequency. The only components left to select are the input capacitors. The input capacitors C_{in1} and C_{in2} can be varied in three ways: vary the total capacitance,vary the ratio of the two capacitances, or both. In Fig. 4.18, the total capacitance is varied

while $C_{in1} = C_{in2}$. As the total input capacitance increases, the resonant frequency and peak decrease and the overall frequency response of the QPRSCC is closer to first order in behavior. While the first order behavior is desirable it comes at the cost of higher input capacitance and increased board area. Note the input parasitic inductance is not included.

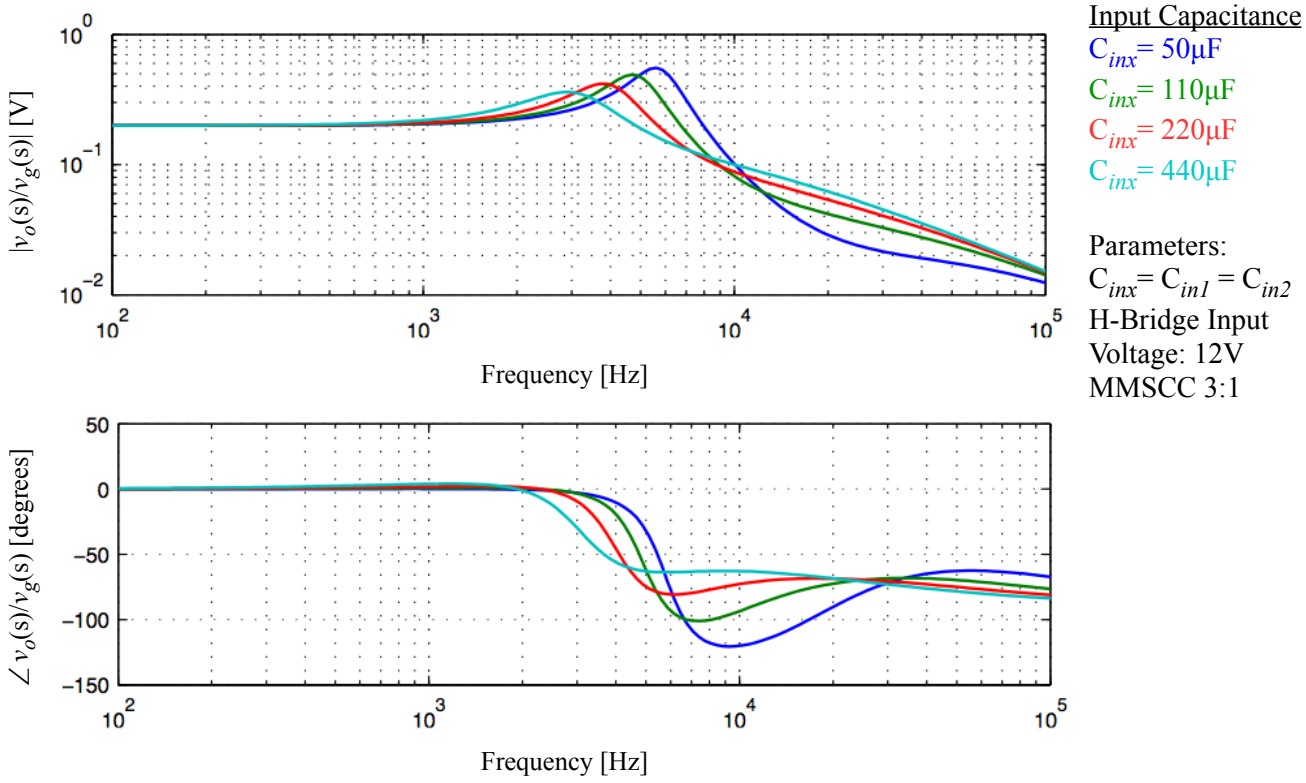


Fig. 4.18. QPRSCC line-to-output voltage frequency response varying input capacitance with $C_{in1} = C_{in2}$

In Fig. 4.19 frequency response of the QPRSCC line-to-output voltage transfer function is evaluated with different total input capacitances and different ratios between C_{in1} and C_{in2}. With increasing total capacitance, the resonant frequency decreases as shown previously in Fig. 4.18, but is not dependent on the ratio (C_{in1} and C_{in2}). The dampening of the 2nd order resonance is proportional to the capacitance C_{in2} (the input capacitance for the H-Bridge). The larger C_{in2}, the more the frequency response behaves as first order. This also indicates that in terms of the QPRSCC dynamics the input capacitance C_{in1} can be comparatively small. This intuitively makes sense as the averaged small-signal model of the MMSCC includes an input capacitance in parallel with the input capacitance C_{in1} seen in Fig. 4.14(a). The modeled input capacitance of the MMSCC is approximately 120µF for the MMSCC in 2:1, 3:1, and 4:1. Thus, there is effectively at least 120µF seen at C_{in1} by the QPRSCC in terms of small-signal

dynamics. Shifting the resonant frequency is not of much value however, increasing the input capacitance for the H-Bridge will cause the QPRSCC line-to-output voltage frequency response to behave more like a first order system. The 2nd order behavior in the output is less effected by changes in the input voltage past 10kHz until reaching the MHz range when the first order behavior is equivalent.

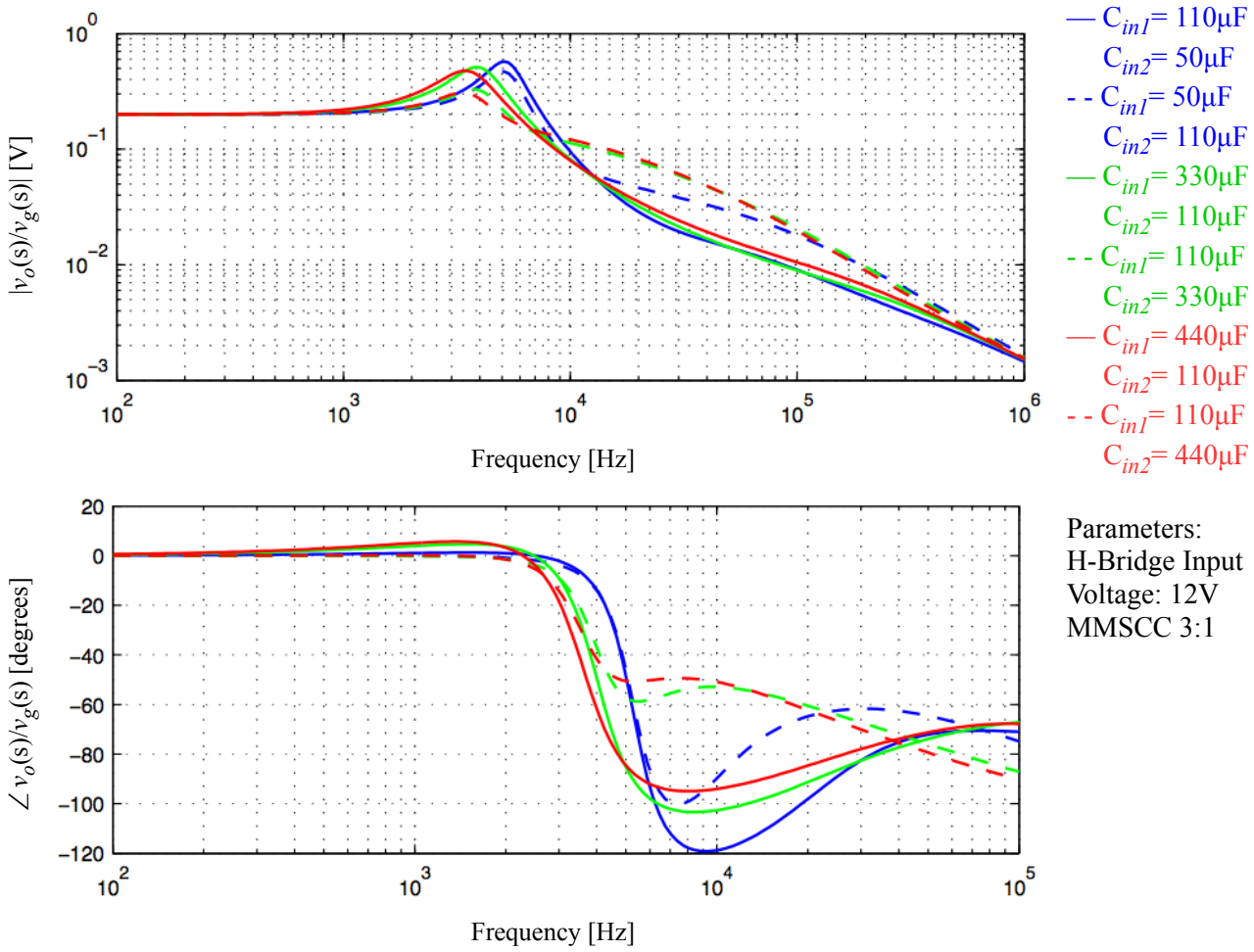


Fig. 4.19. QPRSCC line-to-output voltage frequency response varying the input capacitance ratios ($C_{in1} \neq C_{in2}$)

4.2.3 Open Loop Output Impedance Transfer Function

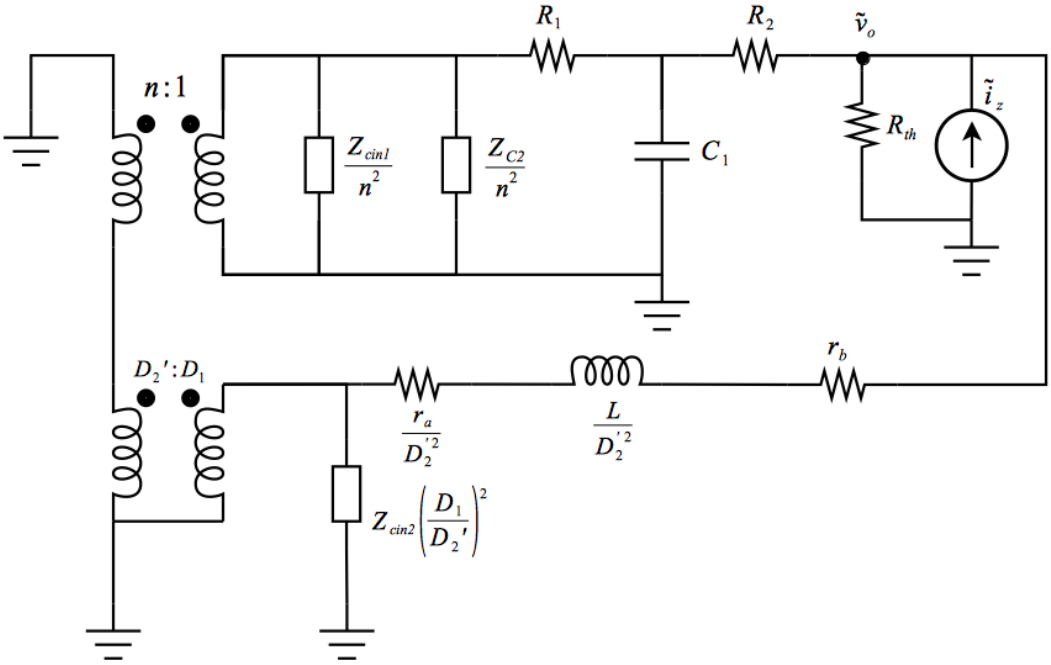
A. Derivation of the Output Impedance Transfer Function

To find the small-signal output impedance, Z_{out}, the duty cycles are held constant, the input voltage is shorted, and one injects a test current $\tilde{i}_z$ solving for the ratio of the output voltage generated over the test current. With constant duty cycles, the DC PWM switch models can be used as in the derivation of the line-to-output voltage transfer function. The same circuit manipulations applied in the line-to-

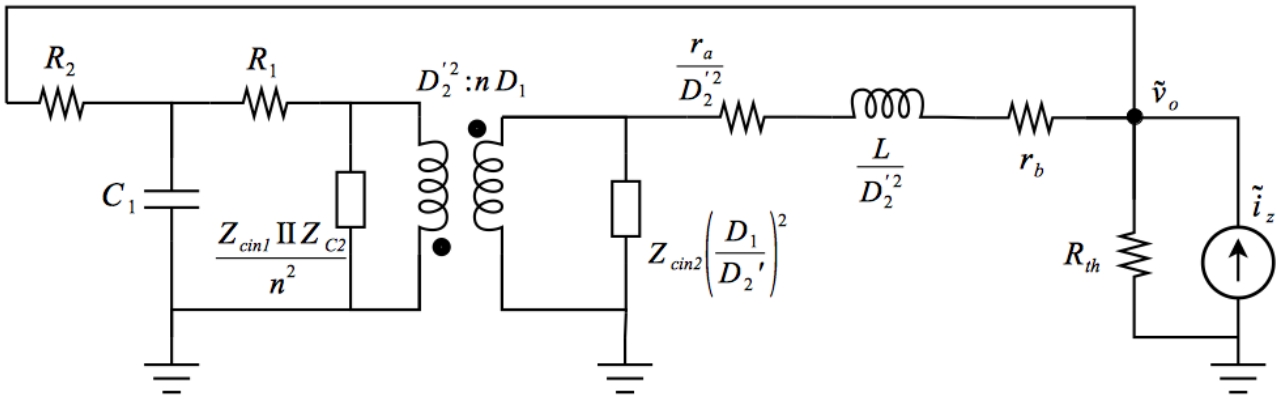
output transfer function can be used producing a similar circuit model as the one in Fig. 4.13 except that the input voltage is shorted to ground and the addition of a test current at the output resulting in the circuit model in Fig. 4.20(a). With the input voltage shorted the transformers can be combined, this results in one transformer with a turns ratio of $D_2' : nD_1$ and with opposite polarity. As in section 4.2.1 the impedances are $Z_{cin1} = r_{cin1} + \frac{1}{s C_{in1}}$, $Z_{cin2} = r_{cin2} + \frac{1}{s C_{in2}}$, and $Z_{C2} = R_3 + \frac{1}{s C_2}$. The resistances r_a and r_a definitions are repeated as (4.59) and (4.60) for convenience. From the circuit shown in Fig. 4.20(a) the transformers can be combined to a single transformer with an equivalent conversion ratio and opposite phase dots as depicted in Fig. 4.20(b).

$$r_a = D_1 D_1' r_{e1} + r_L + \left(D_1^2 + D_1'^2 \right) r_s \tag{4.59}$$

$$r_b = \frac{D_2}{D_2'} r_{e2} + \left(1 + \left(\frac{D_2}{D_2'} \right)^2 \right) r_s \tag{4.60}$$



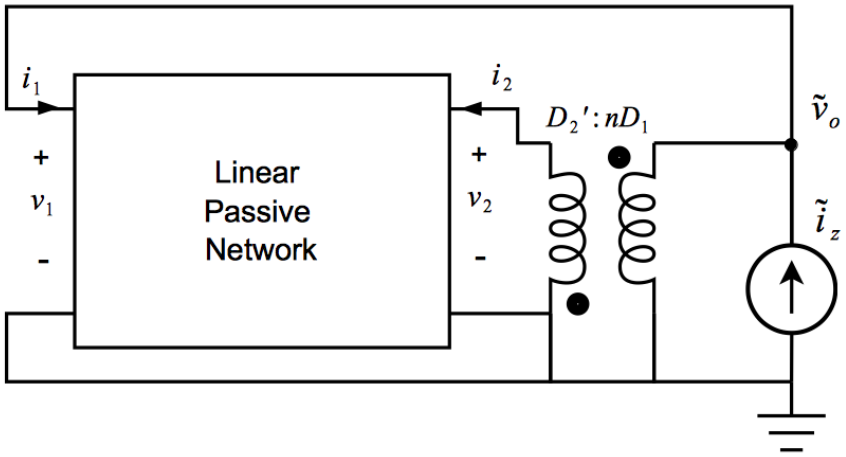
(a)The input voltage is shorted to ground and a test current is injected at the output for output impedance analysis



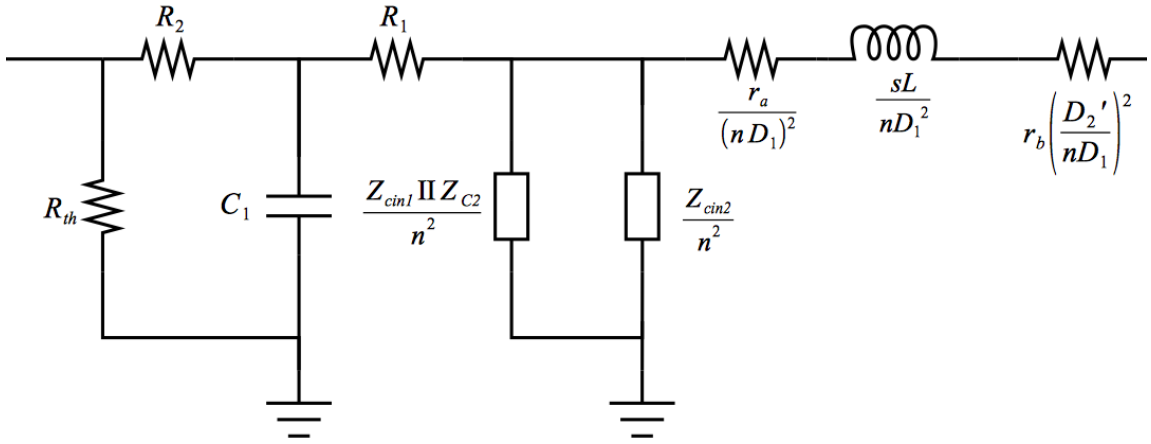
(b) The transformers can be combined allowing for the impedances to be gathered to one side

Fig. 4.20. The small-signal PWM switch models are employed to give a (a) small-signal output impedance circuit model. The two transformers can be combined to give (b) a single transformer circuit model.

The impedances from the H-bridge can be reflected across the transformer, so that all of the impedances are on one side of the transformer. The single impedance network (including R_{th}) is a two port passive network where the currents are related to the voltages by its admittance parameters. Replacing the impedance network with the two port model gives Fig. 4.21(a). The replaced impedance network is shown in Fig. 4.21(b).



(a) Two Port impedance network circuit model for QPRSCC small-signal output impedance



(b) Impedance network

Fig. 4.21. The QRPSCC small-signal output impedance modeled with a (a) two port impedance network replacing the shown (b) impedance network

Using KCL at the output node in Fig. 4.21(a) gives (4.61).

$$i_z = \begin{bmatrix} 1 & -\frac{D_2'}{n D_1} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{4.61}$$

The currents i_1 and i_2 are defined by the admittance parameters and the voltages seen at their respective ports, v_1 and v_2, as in (4.62).

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \mathbf{Y}_{QPRSC} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{4.62}$$

Inspection of Fig. 4.21(a) shows that $v_1 = v_o$ and $v_2 = -D_2'/(n D_2) v_o$. The currents can now be written as (4.63).

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \mathbf{Y}_{QPRSC} \begin{bmatrix} 1 \\ \dfrac{-D_2'}{n D_1} \end{bmatrix} v_o \tag{4.63}$$

Substituting the currents (4.63) into the original equation (4.61) gives (4.64).

$$i_z = \begin{bmatrix} 1 & -\dfrac{D_2'}{n D_1} \end{bmatrix} \mathbf{Y}_{QPRSC} \begin{bmatrix} 1 \\ \dfrac{-D_2'}{n D_1} \end{bmatrix} v_o \tag{4.64}$$

Dividing both side by the output voltage gives the output admittance transfer function (4.65).

$$Y_o(s) = \frac{1}{Z_o(s)} = \begin{bmatrix} 1 & -\dfrac{D_2'}{n D_1} \end{bmatrix} \mathbf{Y}_{QPRSC} \begin{bmatrix} 1 \\ \dfrac{-D_2'}{n D_1} \end{bmatrix} \tag{4.65}$$

The admittance parameters $\mathbf{Y}_{QPRSC}$ are most easily found from ABCD parameters. The ABCD parameters for the impedance network for the QPRSCC output impedance model from Fig. 4.21(b) can then be written as (4.66).

$$ABCD_{QPRSC} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \dfrac{1}{R_{th}} & 1 \end{bmatrix} \begin{bmatrix} 1 & R2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC_1 & 1 \end{bmatrix} \begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \dfrac{1}{Z_{eqin}} & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_{pwm-ser} \\ 0 & 1 \end{bmatrix} \tag{4.66}$$

where $Z_{eqin} = \dfrac{1}{n^2}\left(Z_{in1} \,\text{II}\, Z_{cin2} \,\text{II}\, Z_{C2}\right)$ and $Z_{pwm-ser} = \dfrac{r_a}{(n D_1)^2} + \dfrac{sL}{(n D_1)^2} + \left(\dfrac{D_2'}{n D_1}\right)^2 r_b$

The admittance parameters can be found from the ABCD parameters by (4.67).

$$Y_{QPRSC} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{D}{B} & \dfrac{BC-AD}{B} \\ \dfrac{-1}{B} & \dfrac{A}{B} \end{bmatrix} \tag{4.67}$$

With the admittance matrix defined and the output admittance transfer function found the the output impedance of the QPRSCC is simply (4.68).

$$Z_o(s) = \frac{1}{Y_o(s)} \tag{4.68}$$

B. Analysis of Output Impedance Transfer Function

One limitation of this analysis is the parasitic inductances in the MMSCC and the output capacitance are not modeled. In the MHz range, it is expected that the output impedance will begin to increase due

to these parasitic inductances. Looking at the small-signal circuit model in Fig. 4.21(b), it is evident that the increasing impedance of the H-Bridge inductor is effectively removed at high frequencies as the capacitor's impedances act as shorts. At higher frequencies, the output impedance is dominated by the MMSCC behavior, and the parasitic inductances of the MMSCC and output capacitor will be the determinants of the frequency response. This will have a negligible affect on the analysis.

The output impedance of the QPRSCC will depend on the QPRSCC input voltage as indirectly forces changes of the MMSCC modes from 2:1, 3:1, and 4:1. It was previously assumed in section 3 and [48] that the output impedance of the QPRSCC is equivalently the paralleled output impedances of the MMSCC, H-Bridge, and output capacitor. It is anticipated that the conversion ratio of the MMSCC will be a significant determinant of the QPRSCC output impedance.

The frequency response of the QPRSCC output impedance is plotted with the output impedances of the MMSCC and the H-Bridge at the same operating point. The QPRSCC is at 48V corresponding to the 3:1 MMSCC and 12V input voltage for the H-Bridge. The equivalent paralleled impedance of the H-Bridge and MMSCC output impedance is also included in the frequency responses shown in Fig. 4.22. The paralleled output impedance of the MMSCC and H-Bridge does a reasonable job approximating the QPRSCC output impedance but does not capture completely the frequency response. In most cases this approximation is adequate for understanding the output impedance of the QPRSCC. This approximation does not include the effects of the input capacitors or the effect of having the two converters connected in series.

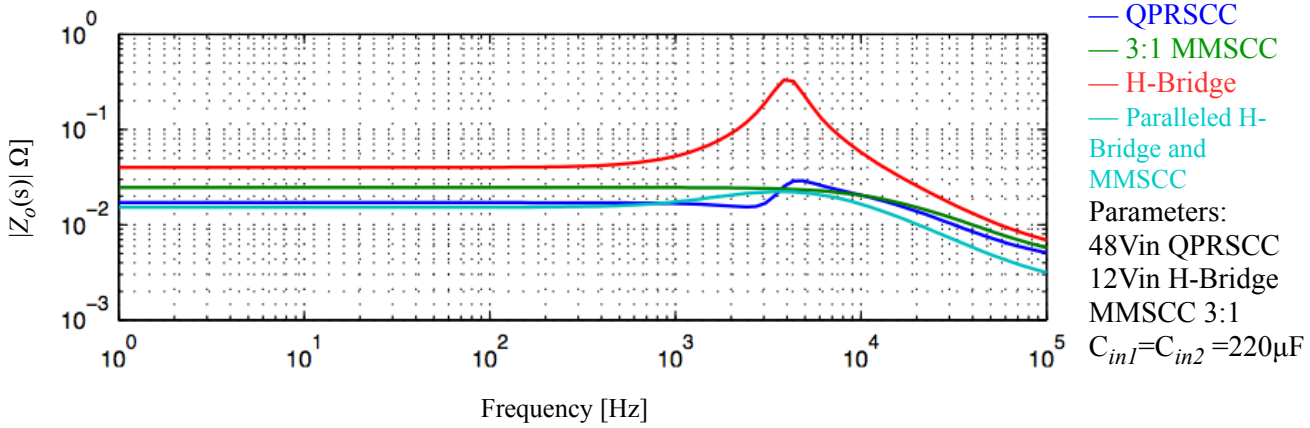


Fig. 4.22. QPRSCC output impedance frequency response compared to equivalent impedance of the H-Bridge and MMSCC output impedances in parallel.

The output impedance frequency response is plotted at different QPRSCC voltages in Fig. 4.23 to analyze the effects of the H-Bridge and MMSCC at different operating points. The input voltages

selected have the H-Bridge in buck, buck-boost, and buck mode of operation and the MMSCC in 2:1, 3:1, and 4:1. The conversion ratio of the MMSCC is shown to have the most significant effect on the output impedance, especially the DC value. The H-Bridge operating as a boost converter has a higher output impedance is reflected in the higher QPRSCC output impedances illustrated by the blue lines. The other major change to the frequency response is in the damping of the resonant peak seen in the 3kHz to 5kHz range by the H-Bridge operating in 4V. As the voltage increases on the H-Bridge, a zero decreases in frequency providing a phase lead and increase in magnitude. At 4V, this zero is effectively canceled so that the output impedance has a more first order frequency response.

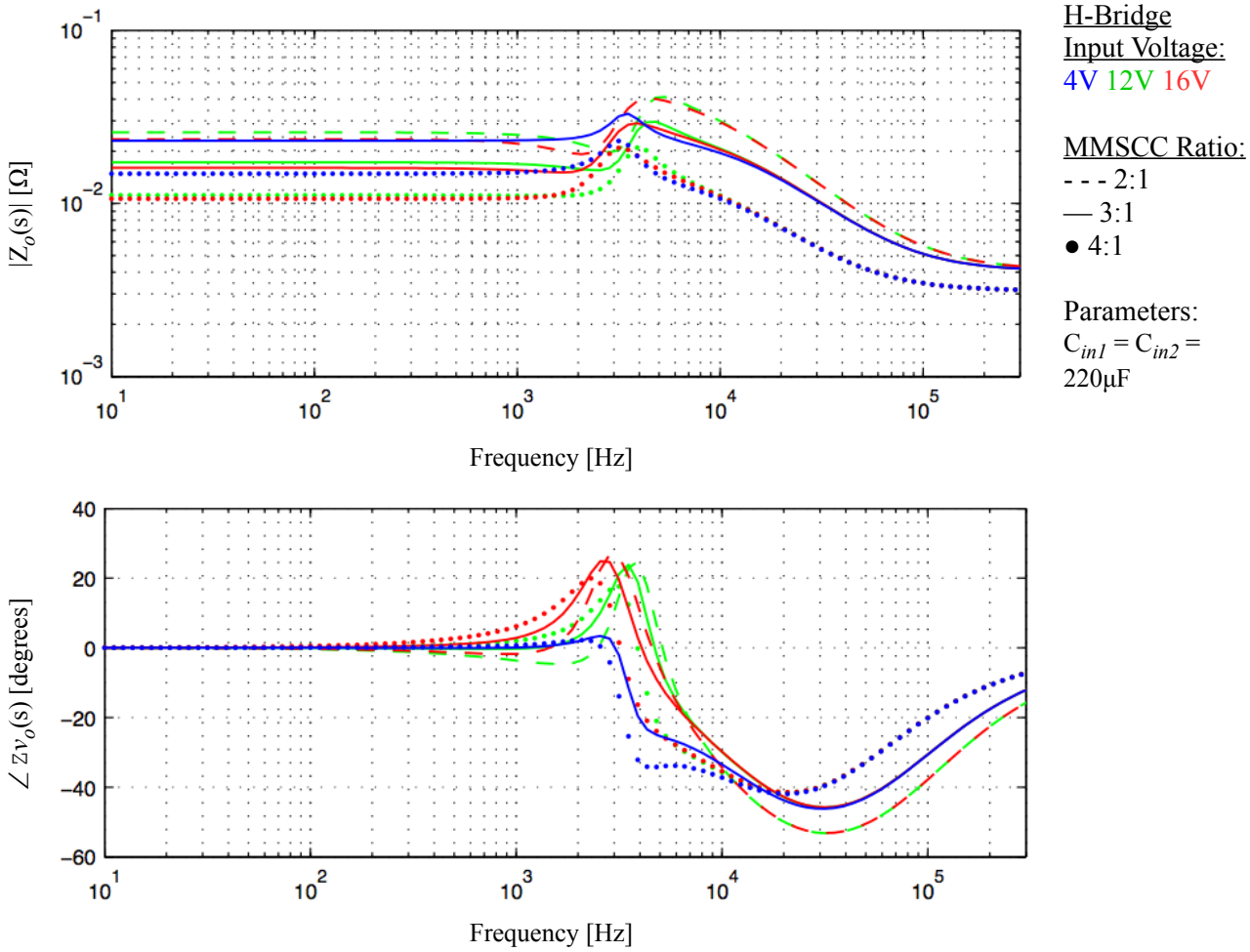


Fig. 4.23. QPRSCC output impedance frequency response at selected QPRSCC input voltages

In the derivation of the output impedance small-signal circuit model, the input capacitors are paralleled (Fig. 4.21(b)) thus the total input capacitance and not the ratio between them will affect the output impedance. The frequency response, of the output impedance with different input capacitors are plotted in Fig. 4.24. As the total input capacitance increases, the resonance peak decreases in frequency and

magnitude. As expected changing the ratios of the input capacitors has no effect on the output impedance.

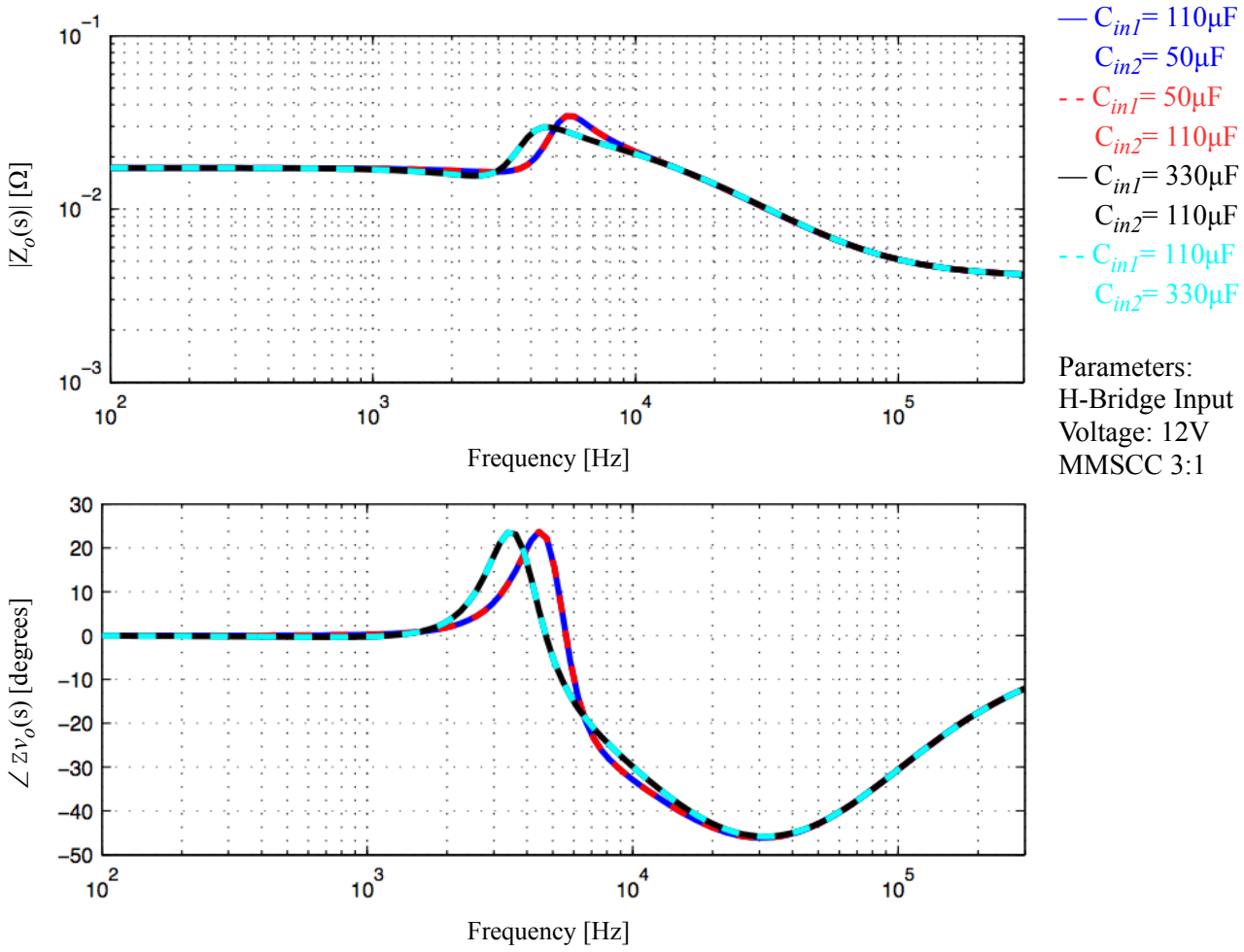


Fig. 4.24. QPRSCC output impedance frequency response with various input capacitances

4.2.4 QPRSCC Control-to-Output Voltage Transfer Function

The QPRSCC like the DC-DC H-Bridge has two independent duty cycles, D_1 and D_2, that can be controlled separately. As in [both h-bridge papers] it is necessary to derive the control-to-output transfer functions from each duty cycle, D_1 and D_2, separately. This can be done by keeping one duty cycle constant and using the Vopérian equivalent DC PWM switch model and perturb the other duty cycle and using the Vopérian small-signal PWM switch model. For example to find the transfer function of the control D_2 to output voltage, D_2 is perturbed while D_1 is held constant and vice versa to derive the transfer function for the control D_1 to the output voltage.

A. Derivation of Control D_2 (Boost) to Output Voltage Transfer Function

To find the control D_2 to output transfer function the control variable D_1 will be held constant and a small perturbation $\tilde{d}_2$ is applied to the other duty cycle D_2. The Vopérian equivalent DC PWM switch model will be used for the switches controlled by D_1 and the small-signal PWM switch model is used for the switches controlled by D_2. For control-to-output analysis, the input voltage is shorted to ground and any load inputs are removed from the system. This gives the control D_2-to-output voltage small-signal circuit model for the QPRSCC shown in Fig. 4.25. The dependent voltage source E and the dependent current source J are defined in (4.69) and (4.70) respectively. The DC quantities I_C and V_{PA2} have been defined previously (section 4.1 DC Analysis) as (4.24)and (4.29). The resistances r_{e1} and r_{e2} have also been defined as (4.8) and (4.9).

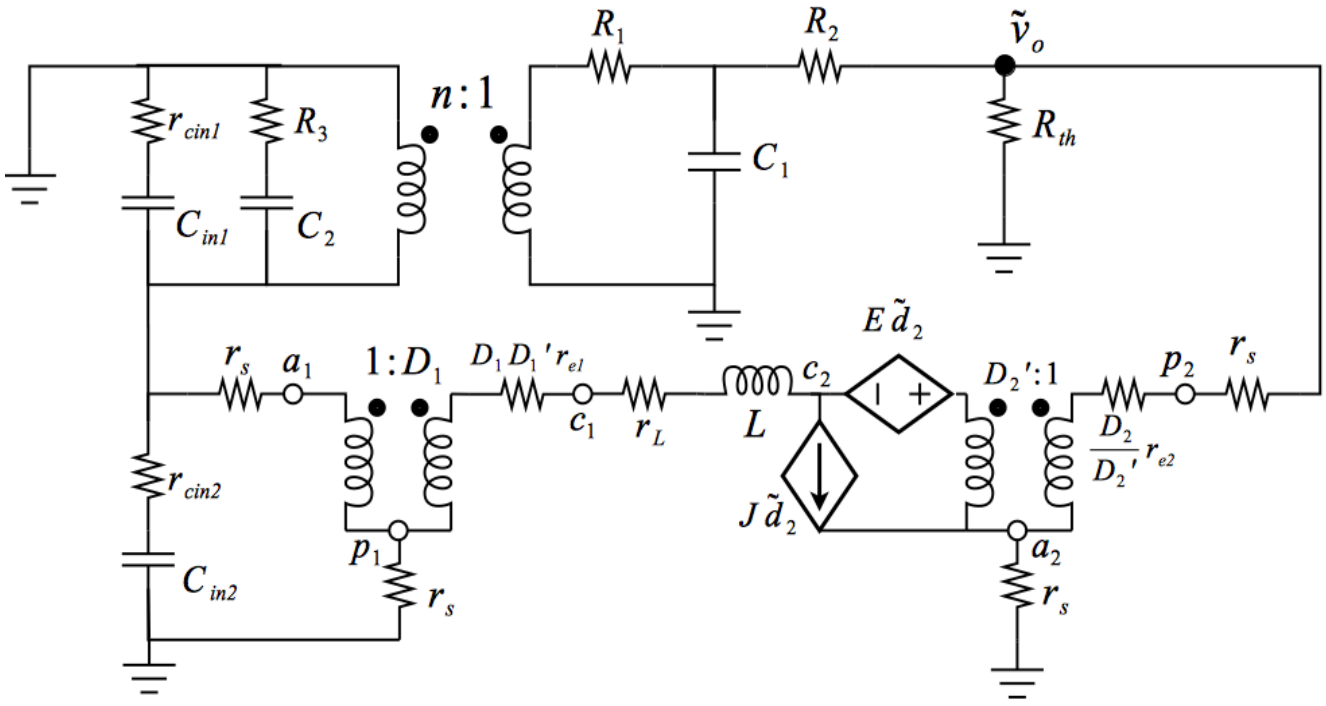


Fig. 4.25. Control-D_2-to-output voltage small-signal circuit model

$$E = V_{PA2} - D_2' r_{e2} I_{C2} = V_{PA2} - D_2' r_{e2} I_{C2} \tag{4.69}$$

$$J = \frac{I_{C2}}{D_2'} = \frac{I_C}{D_2'} \tag{4.70}$$

The capacitors C_{in1}, C_{in2}, and C_2 and their respective series resistance are all in parallel and can be combined as a single impedance Z_{eqin} defined by (4.71). The switch resistances at terminal a_1 and p_1

can both be reflected across the transformer to terminal c_1 and combined with the neighboring resistors to form r_a, defined in (4.2). To move the resistor at terminal a_2 to p_2, the dependent current source must be adjusted to be in parallel with the resistor. The resulting changes are shown in Fig. 4.26(a).

$$Z_{eqin} = (r_{cin1} + 1/sC_{in1}) \text{II} (r_{cin2} + 1/sC_{in2}) \text{II} (R_3 + 1/sC_2) \tag{4.71}$$

$$r_a = D_1 D_1' r_{e1} + r_L + (D_1^2 + D_1'^2) r_s \tag{4.72}$$

Once the current source is in parallel with the resistance at terminal a_2, it can be converted to a Thévenin equivalent circuit (Fig. 4.26(b)). The switch resistance and the newly created voltage source can then be reflected across the transformer (Fig. 4.26(c)). The voltage source is reflected to the left of the transformer to keep the dependent voltage sources together and the switch resistance is reflected to the right of the transformer to create the resistance r_b defined in (4.9). The two dependent voltage sources and the dependent current source can be reflected across the transformer to the right side. The voltage sources are in series with the resistance r_b and can be shifted past the voltage sources but not the current source giving Fig. 4.26(d). The transformer from the SCC and the transformer from the buck portion of the H-bridge can be combined as a single transformer with opposite polarity and a turns ratio $1 : nD_1$. In order to move r_b past the dependent current source an equivalent voltage source must be added as in Fig. 4.26(e). Now r_b can be reflected to the left side of the transformer and be combined with the inductor and r_a to make a series impedance Z_{pwm} defined as (4.8) and depicted in Fig. 4.26(e).

$$r_b = \frac{D_2}{D_2'} r_{e2} + \left(1 + \left(\frac{D_2}{D_2'}\right)^2\right) r_s \tag{4.73}$$

$$Z_{pwm} = r_a + sL + r_b (D_2')^2 \tag{4.74}$$

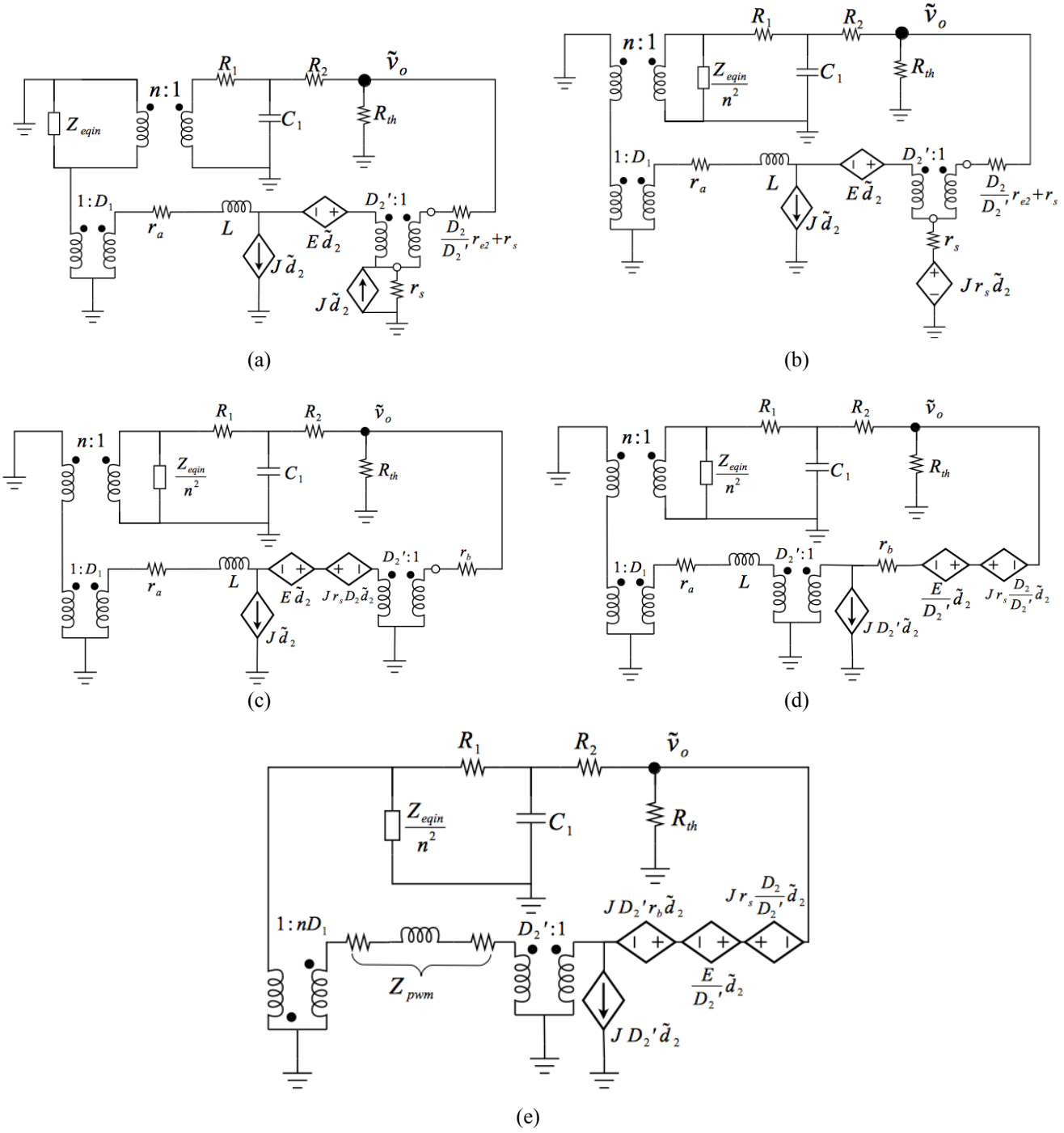
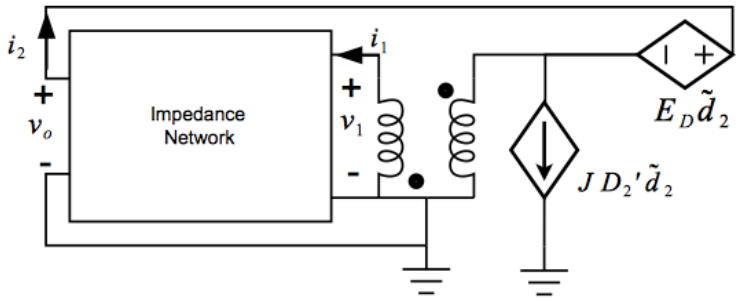


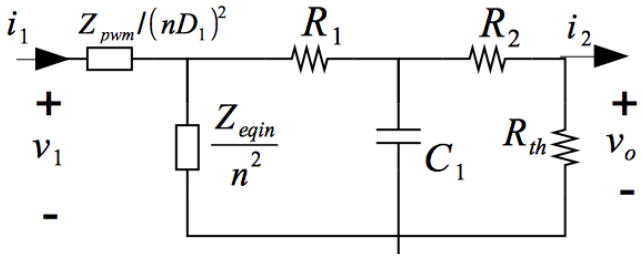
Fig. 4.26. Through circuit manipulation the small-signal circuit model can be modified from (a) to (e)

The impedance Z_{pwm} can then be reflected to the left of the transformer with turns ratio $1:nD_1$. This allows for the circuit model to be reduced to a single impedance network, a single transformer with turns ratio $D_2':nD_1$, and the dependent current and voltage sources. The impedance network, shown in Fig. 4.27(b), can be replaced with a two port model described by ABCD parameters. This provides a simple small-signal model of the QPRSCC for analysis of the control D_2 to output voltage transfer

function shown in Fig. 4.27(a). The combined dependent voltage E_D is (4.39).



(a)simplified control-D_2-to-output voltage small-signal circuit model with two port network.



(b) complex impedance network

Fig. 4.27. The control-D_2-to-output voltage small-signal circuit model using (a) two port impedance network model to replace the (b)complex impedance network

$$E_d=\frac{1}{D_2'}\left(E-J\,r_s\,D_2\right)+J\,D_1'\,r_b \tag{4.75}$$

Analyzing the model in Fig. 4.27(a) gives the governing equations (4.38) through (4.36).

$$E_d\,\tilde{d}_2=v_o+\frac{n\,D_1}{D_2'}\,v_1 \tag{4.76}$$

$$J\,D_2'\,\tilde{d}_2=i_2+\frac{D_2'}{n\,D_1}\,i_1 \tag{4.77}$$

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix}=\mathbf{ABCD}\begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.78}$$

Equations (4.30) and (4.28) can be written as a system of linear equations (4.26). Substituting (4.10) into the system of equations (4.26) gives (4.24).

$$\begin{bmatrix} E_d \\ J\,D_2' \end{bmatrix}\tilde{d}_2=\begin{bmatrix} \frac{n\,D_1}{D_2'} & 0 \\ 0 & \frac{D_2'}{n\,D_1} \end{bmatrix}\begin{bmatrix} v_1 \\ i_1 \end{bmatrix}+\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.79}$$

$$\begin{bmatrix} E_d \\ J\,D_2{}' \end{bmatrix} \tilde{d}_2 = \left(\begin{bmatrix} \frac{n\,D_1}{D_2{}'} & 0 \\ 0 & \frac{D_2{}'}{n\,D_1} \end{bmatrix} \mathbf{ABCD} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \right) \begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.80}$$

Equation (4.45) can be expressed in the form of **C Y** = **A X** as in (4.11). Premultiplying both sides by the inverse of **A** gives (4.25), the multiplication of $\mathbf{A}^{-1}\,\mathbf{C}$ will give a 2x1 matrix whose first row is the desired control-to-output voltage relation.

$$C_{2x1}\,\tilde{d}_2 = A_{2x2} \begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.81}$$

$$A_{2x2}^{-1}\,C_{2x1}\,\tilde{d}_2 = \begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.82}$$

$$\begin{bmatrix} v_o \\ i_2 \end{bmatrix} = A_{2x2}^{-1}\,C_{2x1}\,\tilde{d}_2 \tag{4.83}$$

B. Analysis of Control D_2 to Output Voltage Transfer Function

Analysis of the QPRSCC control is motivated by two questions: how does the quasi-parallel configuration affect the control and can a control strategy designed for the H-Bridge work for the QPRSCC? For a sigma configuration (quasi-parallel) [49] the authors found the intrinsic feedback of the quasi-parallel configuration simply attenuated the control-to-output frequency response. The same effect is expected to be found here implying a control strategy designed for the H-Bridge will adequately regulate the QPRSCC. This allows for the efficient control strategy outlined in [64] and [65] for the H-Bridge and for the use of commercial IC regulators such as the LT8705 for regulation of the QPRSCC. Analysis of the QPRSCC small-signal line output impedance and line-to-output voltage transfer functions have revealed the QPRSCC to behave somewhat like a first order system. The phase change is in total -90 degrees and the magnitude decrease is -20dB/decade. There is some 2nd order affects and resonance seen but this occurs with in a limited frequency range. This means the RHP zero from the H-Bridge, in the control-D_2-to-output voltage transfer function, will add -90 degree to the phase change but will only add up to -180 degrees for the QPRSCC. This will mitigate the control issues associated with the RHP zero.

The H-Bridge control-D_2-to-output voltage transfer function is compared to the QPRSCC transfer

function in Fig. 4.28. The H-Bridge is operated with the same input voltage and load as the H-Bridge in the QPRSCC operating with 40V input voltage and the MMSCC in 3:1 operating at 50% load (60W). The quasi-parallel configuration as expected attenuates the DC gain of the H-Bridge control-to-output transfer function. The frequency response of the QPRSCC is still 2nd order like the H-Bridge with a -40dB/decade slope until reaching the LHP zero from the quasi-parallel intrinsic feedback and the RHP zero of the H-Bridge. In terms of phase change, there is a significant change as the natural feedback of the QPRSCC adds a LHP zero. This LHP zero adds 90 degrees to the phase effectively negating the -90 degrees due to the RHP zero. Thus the QPRSCC phase settles to -180 degrees instead of the -270 degrees for the H-bridge. The quasi-parallel configuration is still affected by RHP zero from the H-Bridge but because the QPRSCC behaves somewhat like a first order system the -90 degree phase from RHP zero is less problematic.

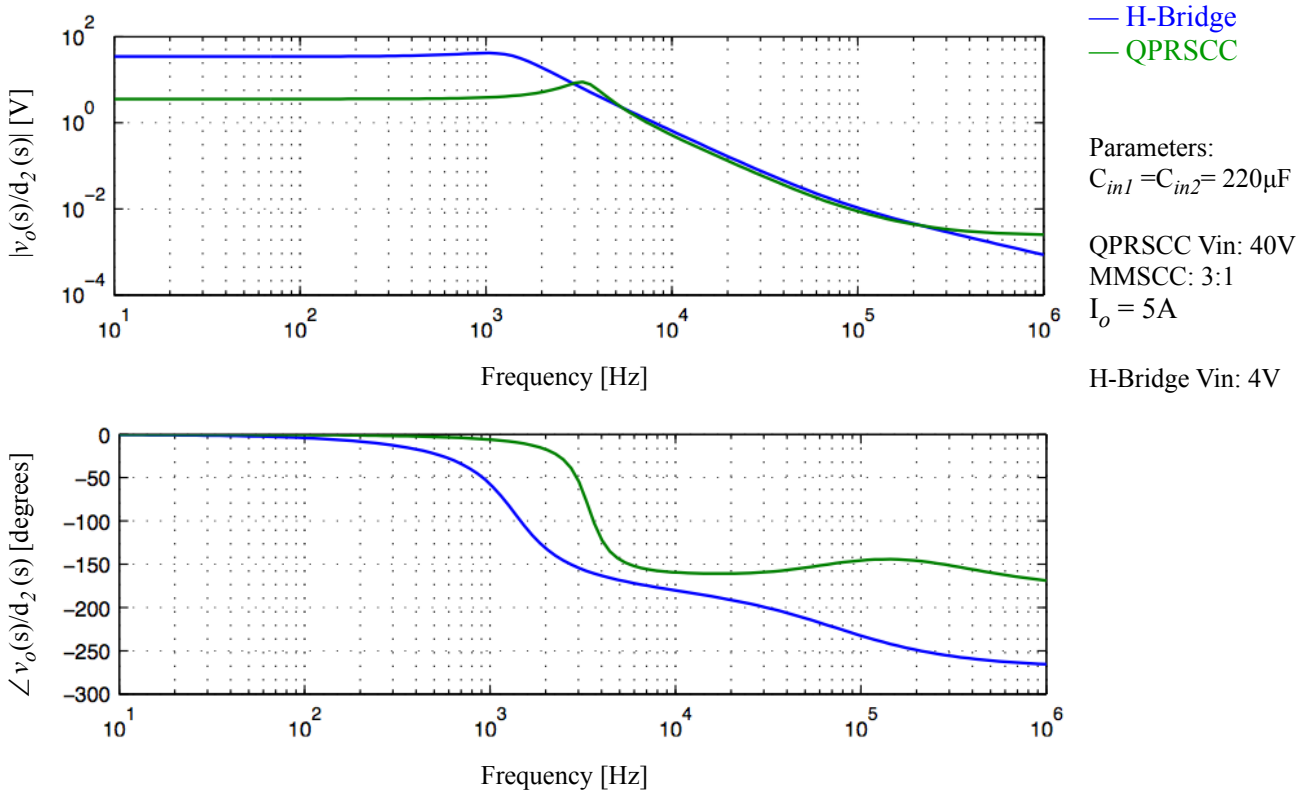


Fig. 4.28. Frequency response of the QPRSCC and H-Bridge control-D_2-to-output voltage transfer function showing the quasi-parallel configuration attenuates DC gain

Next the frequency response of the control-D_2-to-output voltage transfer function of the QPRSCC will be analyzed at different input voltages range, different load conditions, and finally with various input capacitors. The frequency responses at key QPRSCC input voltages are plotted in Fig. 4.29. The behavior of the QPRSCC control-to-output transfer function is as expected in the design of the H-

Bridge converter or a boost converter. The input voltage of the H-Bridge, or alternatively the duty ratio D_2, steady state value has the most significant affect on the frequency response of the QPRSCC control. The different conversion ratios of the MMSCC on the other hand is seen not to have significant affect on the frequency response.

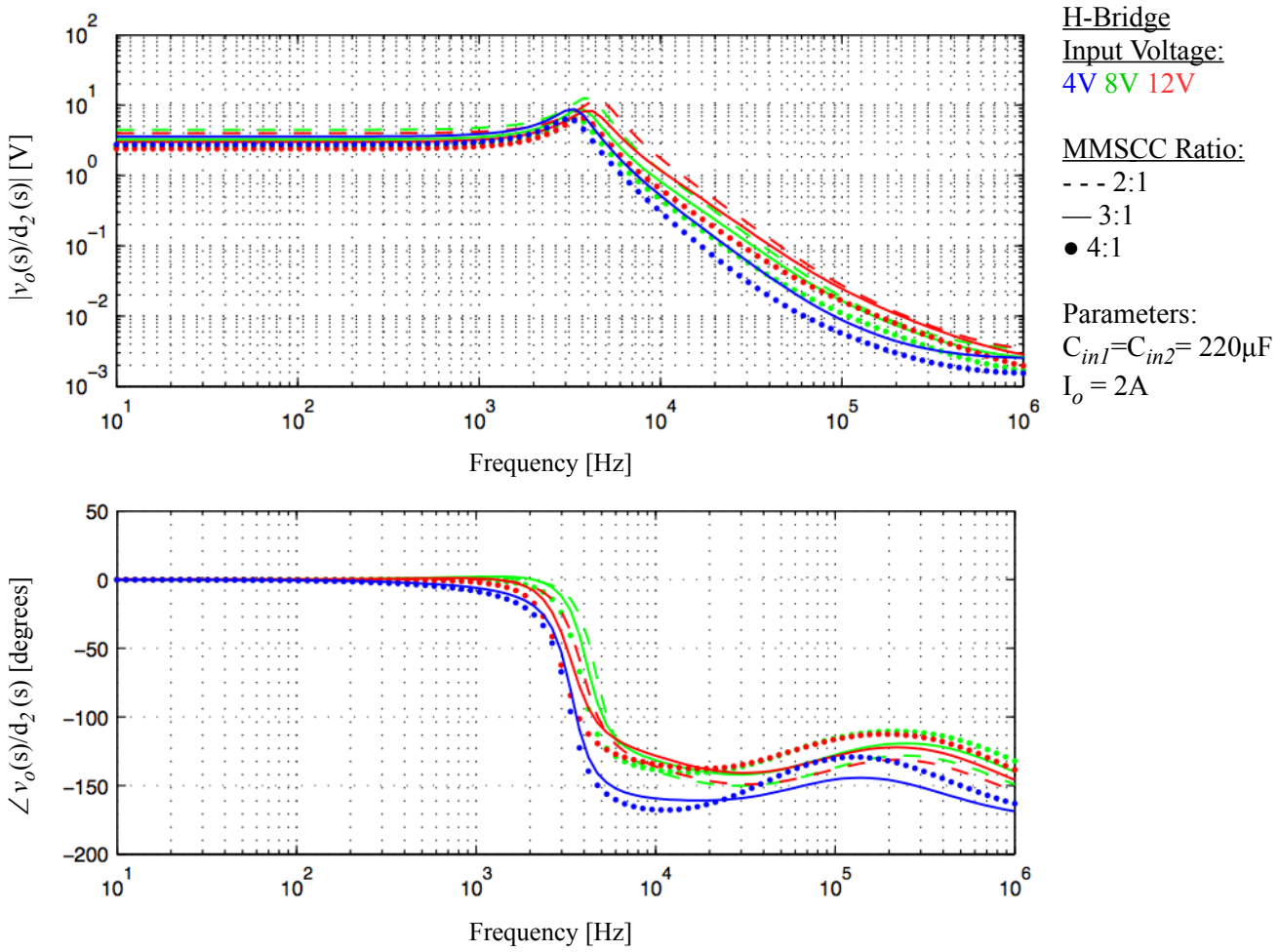


Fig. 4.29. The frequency response of the QPRSCC control-D_2-to-output voltage transfer function does not vary significantly across the QPRSCC input voltage range.

The QPRSCC control D_2 to output voltage transfer function frequency response is evaluated at different load conditions. The QPRSCC is set at an operating point of 42V putting the H-Bridge in boost mode with a conversion ratio of 1:2 and the MMSCC in 3:1. The load is varied from 1A to 10A in Fig. 4.30 showing significant affect on a zero. In the magnitude plot, a zero is seen to decrease in frequency as the load increases. The phase frequency response reveals the problematic RHP zero is still present, but has been negated at light loads. As the load increases the RHP zero decreases in frequency causing the phase to reach -180 degrees at a lower frequency.

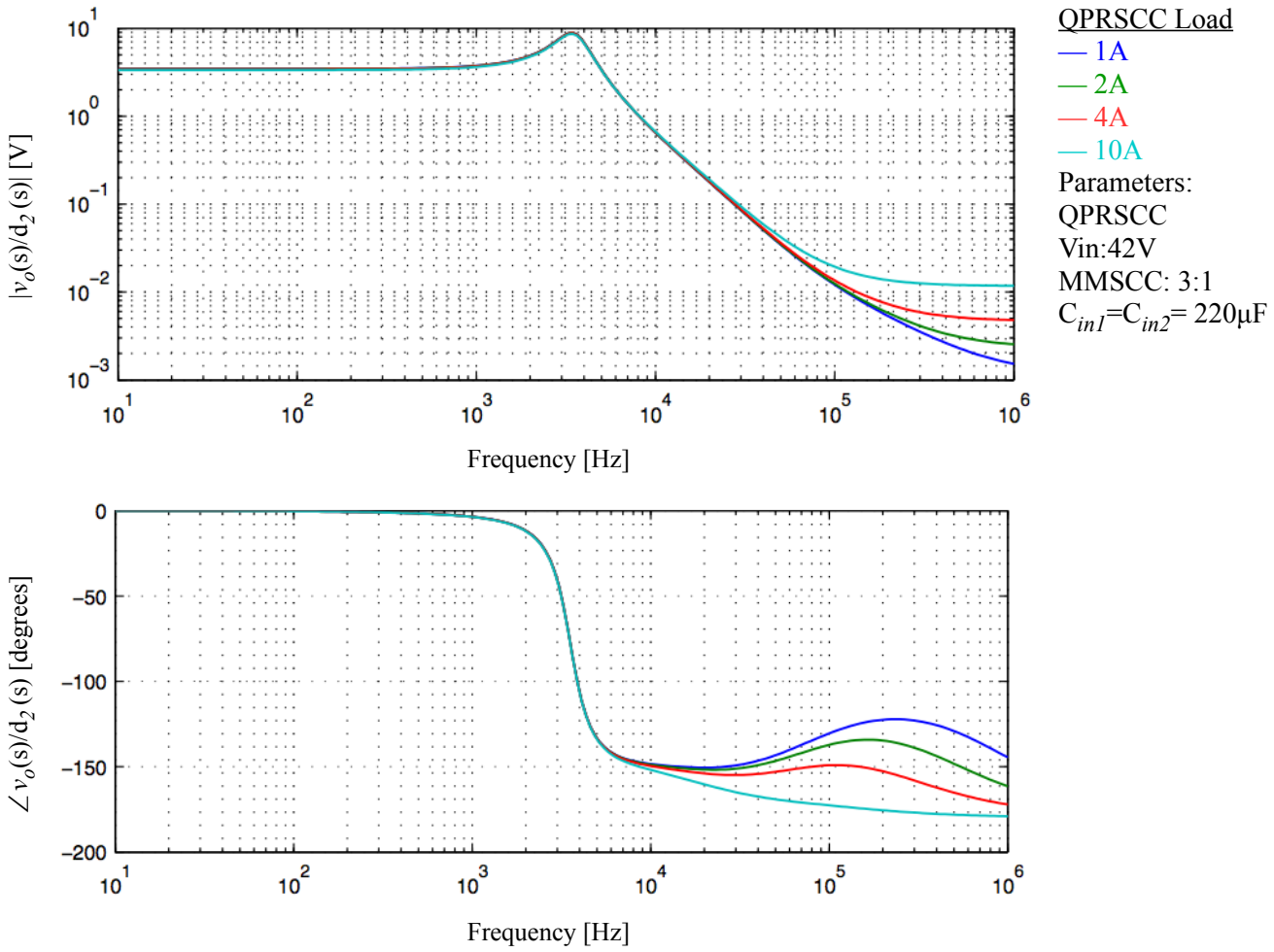


Fig. 4.30. The frequency response of the QPRSCC control D_2-to-output voltage transfer function at different output current loads highlighting an issue in terms of phase margin at high loads.

Finally the effects of the input capacitors on the frequency response of QPRSCC control D_2 to output voltage transfer function are investigated. Previous analysis has indicated that the total input capacitance and the amount of capacitance for the H-Bridge significantly affects the frequency responses depending on the impedance network. Inspection of the impedance network, Fig. 4.27(a), shows the individual capacitors C_{in1} and C_{in2} are paralleled and combined to a single impedance thus only the total input capacitance will affect the frequency response and not the ratio of the input capacitances. If the H-Bridge can quickly change its input voltage then the input voltage for the MMSCC will change quickly as well allowing for the appropriate output voltage to be achieved faster. This implies that a lower input capacitance (thus less current to change the voltage) will provide higher bandwidth for the control but possibly more resonance. This agrees with previous analysis where higher capacitance decreased bandwidth but made the QPRSCC behave more like a first order system. The QPRSCC frequency response of the boost control-to-output voltage transfer function is shown in

Fig. 4.31 indicating this to be the case. It takes a substantial increase in the amount of input capacitance to decrease the resonance peak seen and make the behavior more first order. Additionally it reduces the bandwidth and in terms of control design the benefits of increased input capacitance are negligible.

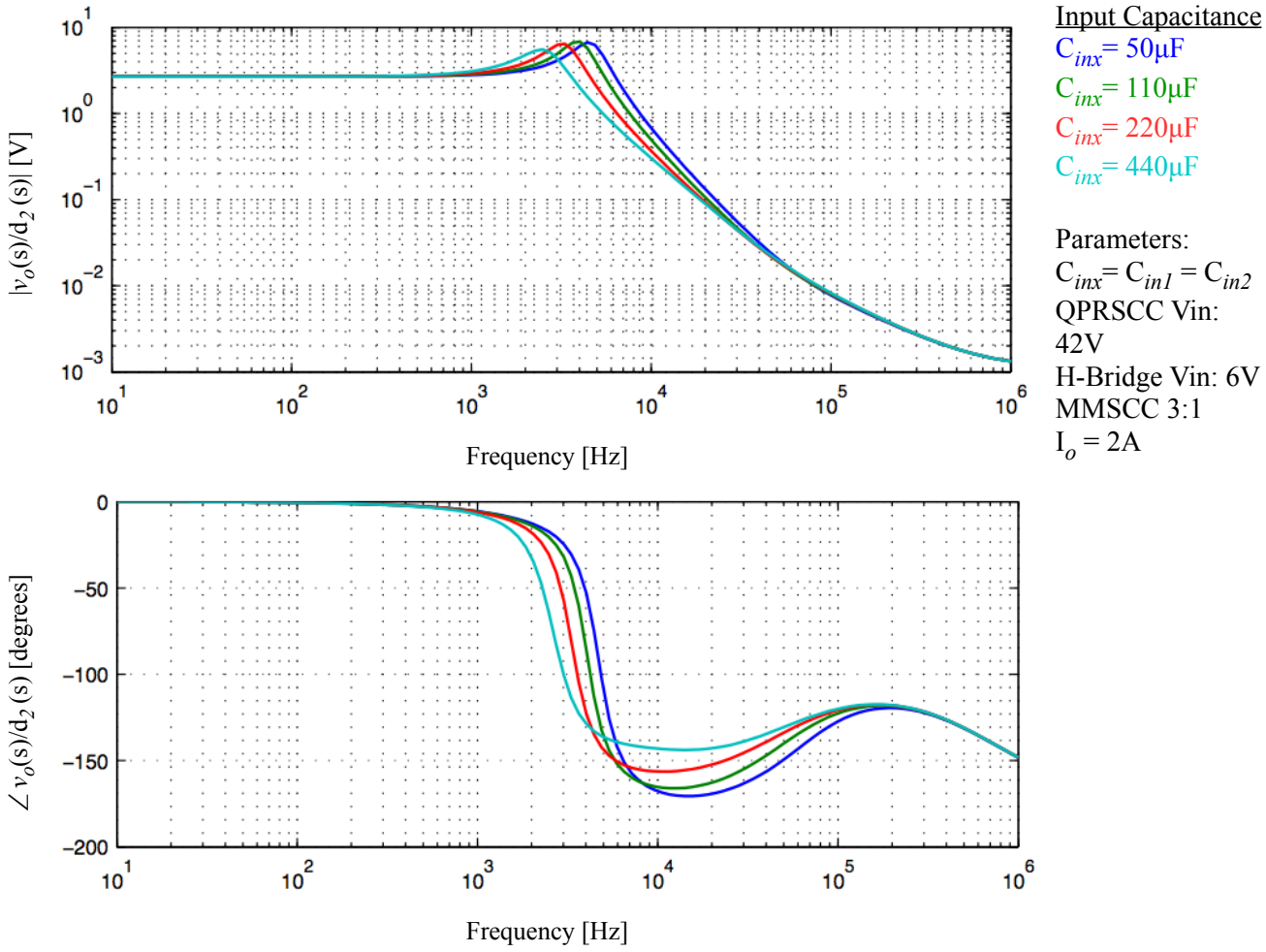


Fig. 4.31. QPRSCC control-D_2-to-output voltage frequency response as the total input capacitance is varied

C. Derivation of Control D_1 (Buck) to Output Voltage Transfer Function

To find the control D_1 to output transfer function the control variable D_2 will be held constant while D_1 is perturbed by $\tilde{d}_1$. This allows the DC PWM switch model to be used for the switches controlled by D_2 and the small-signal PWM switch model for the switches controlled by D_1. Other system inputs such as the input (line) voltage and load transients are set to zero. The control D_1 to output voltage small-signal circuit model for the QPRSCC is as shown in Fig. 4.32. The dependent voltage source E and the dependent current source J are defined in (4.51) and (4.55) respectively. The DC quantities I_C

and V_{AP1} have been defined previously in section 4.1 DC Analysis as (4.24) and (4.22). The resistances r_{e1} and r_{e2} have also been defined in 4.1 DC Analysis as (4.8) and (4.9).

$$E=\frac{1}{D_1}\left(V_{AP1}+\left(D_1-D_1'\right)r_{e1}I_C\right) \tag{4.84}$$

$$J=I_C \tag{4.85}$$

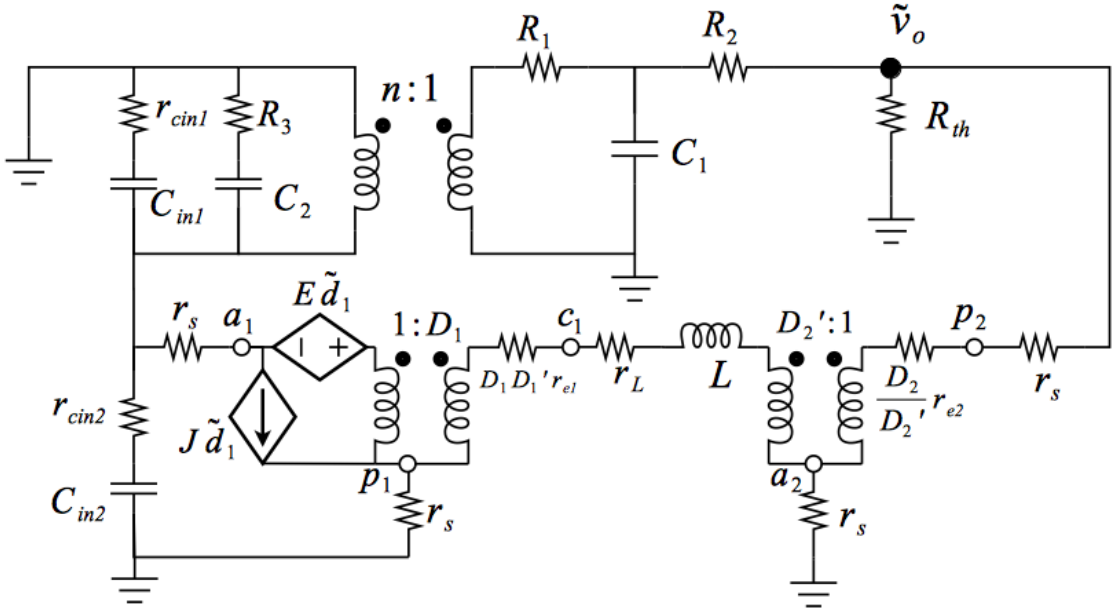


Fig. 4.32. Control-D_1-to-output voltage small-signal circuit model of the QPRSCC

The capacitors C_{in1}, C_{in2}, and C_2 and their respective series resistance are in parallel and can be combined as a single impedance Z_{eqin} defined by (4.56). The switch resistance at terminal a_2 can be reflected across the transformer to terminal c_2 and combined with the neighboring resistors to form r_b defined in (4.72).

$$Z_{eqin}=\left(r_{cin1}+1/sC_{in1}\right)\text{II}\left(r_{cin2}+1/sC_{in2}\right)\text{II}\left(R_3+1/sC_2\right) \tag{4.86}$$

$$r_b=\frac{D_2}{D_2'}r_{e2}+\left(1+\left(\frac{D_2}{D_2'}\right)^2\right)r_s \tag{4.87}$$

To move the resistor at terminal p_1 to c_1, the dependent current source must be manipulated to be in parallel with the resistor. Once in parallel, the current source and resistance can be replaced by a Thévenin equivalent model. The aforementioned changes have been implemented in Fig. 4.33(a). The resistance and voltage source from the newly created Thévenin equivalent can then be reflected from the bottom, p_1, of the transformer to the sides a_1 and c_1. The resistance is reflected to the right, to c_1,

and joined with the non-linear resistance and inductor resistance to form r_c defined in (4.73). The impedance Z_{eqin} is also reflected across the SCC transformer in an effort to gather all impedances together to form a single impedance network. These changes result in Fig. 4.33(b).

$$r_c = D_1 D_1' r_{el} + r_L + D_1'^2 r_s \tag{4.88}$$

The objective is to move all the impedances into a single network and combine all the transformers. The next step is to combine the dependent voltage sources and reflect them and the current source across the transformer. The voltage source is then in series with r_c, L, and r_b and can be moved to the right of those impedances Fig. 4.33(c). The current source can be moved to the right of those impedances as well by adding an equivalent voltage that can be combined to form E_d defined in. This allows the voltage source and current source to be reflected across the last transformer (boost portion of the H-bridge). The impedance r_c, L, and r_b can be reflected left across the transformer representing the buck portion of the H-bridge. The resistance r_c can be joined with the switch resistance r_s resulting in the familiar resistance r_a used in previous sections and defined as (4.74). The impedances r_a, L, and r_b can be represented by a single impedance Z_{pwm} defined in (4.75). This gives the model shown in Fig. 4.33(d).

$$r_a = D_1 D_1' r_{el} + r_L + \left(D_1^2 + D_1'^2\right) r_s \tag{4.89}$$

$$Z_{pwm} = r_a + sL + r_b \left(D_2'\right)^2 \tag{4.90}$$

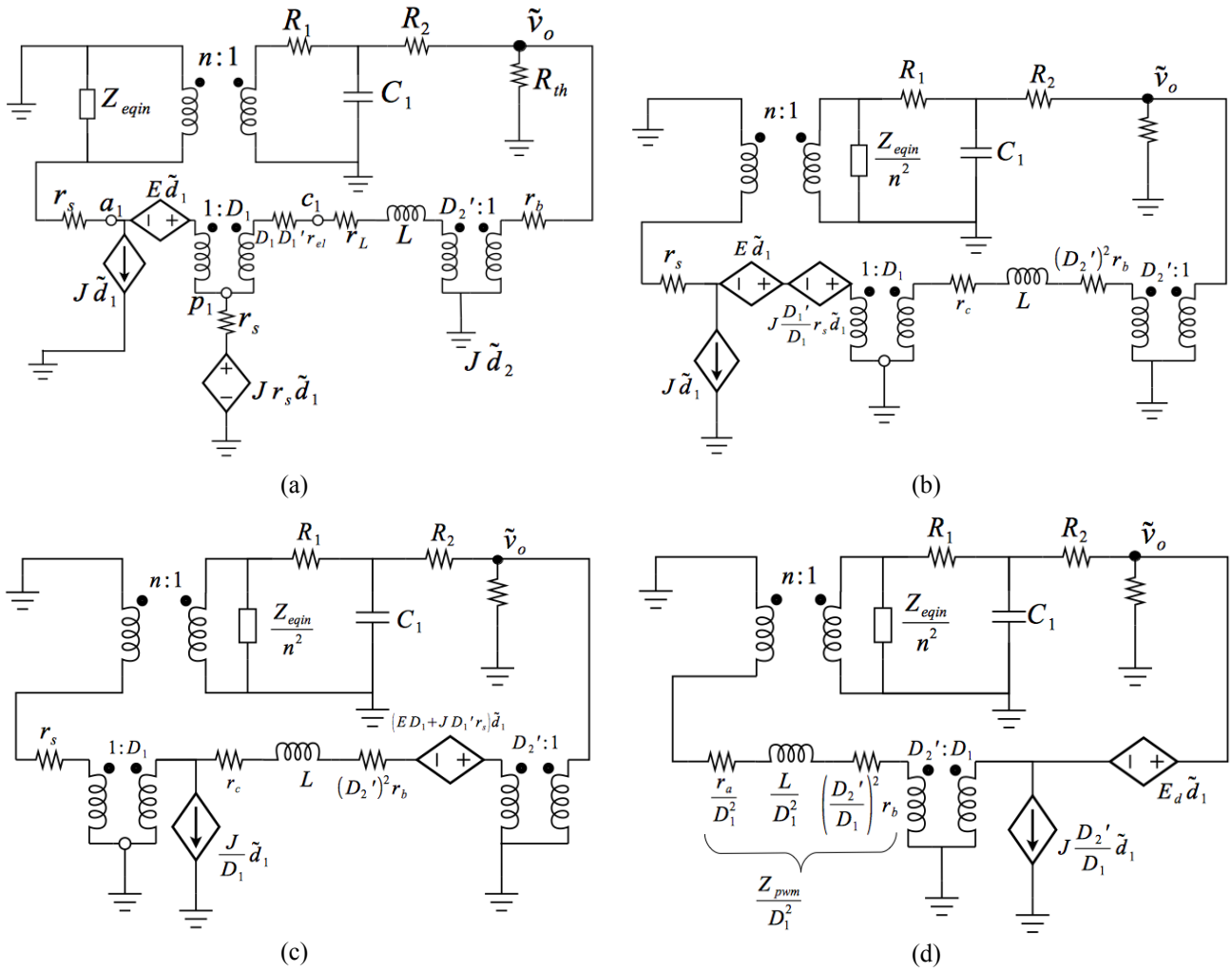
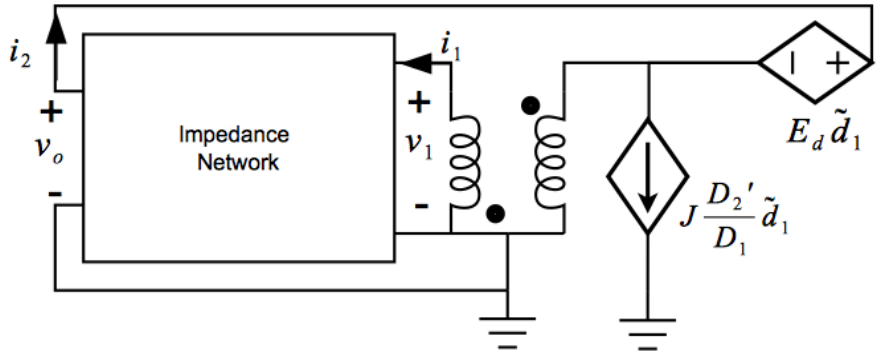
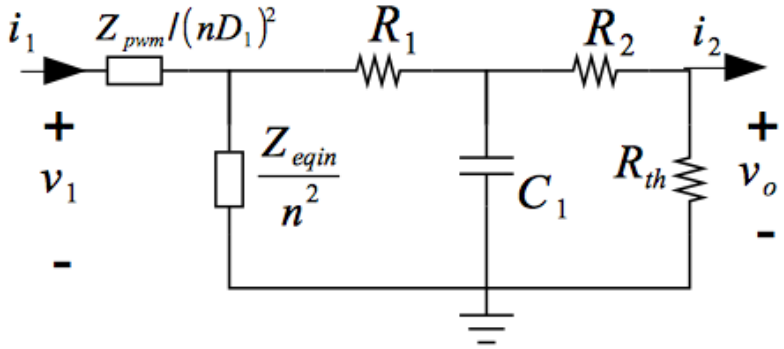


Fig. 4.33. Manipulations of the small-signal circuit model to create a single complex impedance network creating a simplified control-to-output voltage small-signal circuit model.

The impedance Z_{pwm} can then be reflected across the SCC transformer, thereby arranging all of the impedances in a single network shown in Fig. 4.34(b). The impedance network can now be modeled as a two port model described by ABCD parameters. The transformer from the SCC can then be combined with the transformers representing the switches in the H-bridge resulting in a simple circuit model representing the control D1 to output voltage small-signal behavior of the QPRSCC depicted in Fig. 4.34(a).



(a) Simplified small-signal circuit model with two port impedance network



(b) complex impedance network

Fig. 4.34. The control-D_1-to-output voltage small-signal circuit model can be modeled with (a) two port impedance network replacing the (b) complex impedance network.

Analyzing the circuit in Fig. 4.34(a) gives the governing equations (4.76) through (4.78).

$$E_d \tilde{d}_2 = v_o + \frac{n D_1}{D_2'} v_1 \tag{4.91}$$

$$J \frac{D_2'}{D_1} \tilde{d}_2 = i_2 + \frac{D_2'}{n D_1} i_1 \tag{4.92}$$

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \mathbf{ABCD} \begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.93}$$

Equations (4.76) and (4.77) can be written as a system of linear equations (4.79). Substituting (4.78) into the system of equations (4.79) gives (4.80).

$$\begin{bmatrix} E_d \\ J \frac{D_2'}{D_1} \end{bmatrix} \tilde{d}_2 = \begin{bmatrix} \frac{n D_1}{D_2'} & 0 \\ 0 & \frac{D_2'}{n D_1} \end{bmatrix} \begin{bmatrix} v_1 \\ i_1 \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.94}$$

$$\begin{bmatrix} E_d \\ J\dfrac{D_2'}{D_1} \end{bmatrix} \tilde{d}_2 = \left(\begin{bmatrix} \dfrac{n D_1}{D_2'} & 0 \\ 0 & \dfrac{D_2'}{n D_1} \end{bmatrix} \mathbf{ABCD} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \right) \begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.95}$$

Equation (4.80) can be expressed in the form of **C Y** = **A X** as in (4.81). Premultiplying both sides by the inverse of **A** gives (4.82), the multiplication of $\mathbf{A}^{-1}$ **C** will give a 2x1 matrix whose first row is the desired control-to-output voltage relation.

$$C_{2x1}\tilde{d}_2 = A_{2x2}\begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.96}$$

$$A_{2x2}^{-1} C_{2x1}\tilde{d}_2 = \begin{bmatrix} v_o \\ i_2 \end{bmatrix} \tag{4.97}$$

$$\begin{bmatrix} v_o \\ i_2 \end{bmatrix} = A_{2x2}^{-1} C_{2x1}\tilde{d}_2 \tag{4.98}$$

D. Analysis of Control D_1 to Output Voltage Transfer Function

The QPRSCC control D_1 to output voltage transfer function will be compared to the control transfer function of the H-Bridge, analyzed at different operating points of the QPRSCC input voltage range, analyzed at various loads, and finally with different input capacitances. It has been established that the quasi-parallel configuration natural feedback puts a zero into the transfer functions leading to an approximately first order behavior of the system. There is resonant frequency where the phase reaches minimum of -150 degrees and the magnitude decreases at -40dB/decade until reaching the zero from the quasi-parallel configuration. These properties are expected to be seen again in the duty ratio D_1 to output voltage transfer function.

The frequency response of the H-Bridge control D_1 to output voltage transfer function is compared to the QPRSCC transfer function in Fig. 4.35. The H-Bridge is operated with an equivalent input voltage and load as the QPRSCC operating with 48V input voltage and the MMSCC in 3:1 operation for 50% load (60W). The quasi-parallel configuration as expected attenuates the DC gain of the H-Bridge control-to-output transfer function and the addition of the zero from the quasi-parallel configuration makes the frequency response more like a first order system, suggesting a control strategy implemented for the H-Bridge will be able to control the QPRSCC.

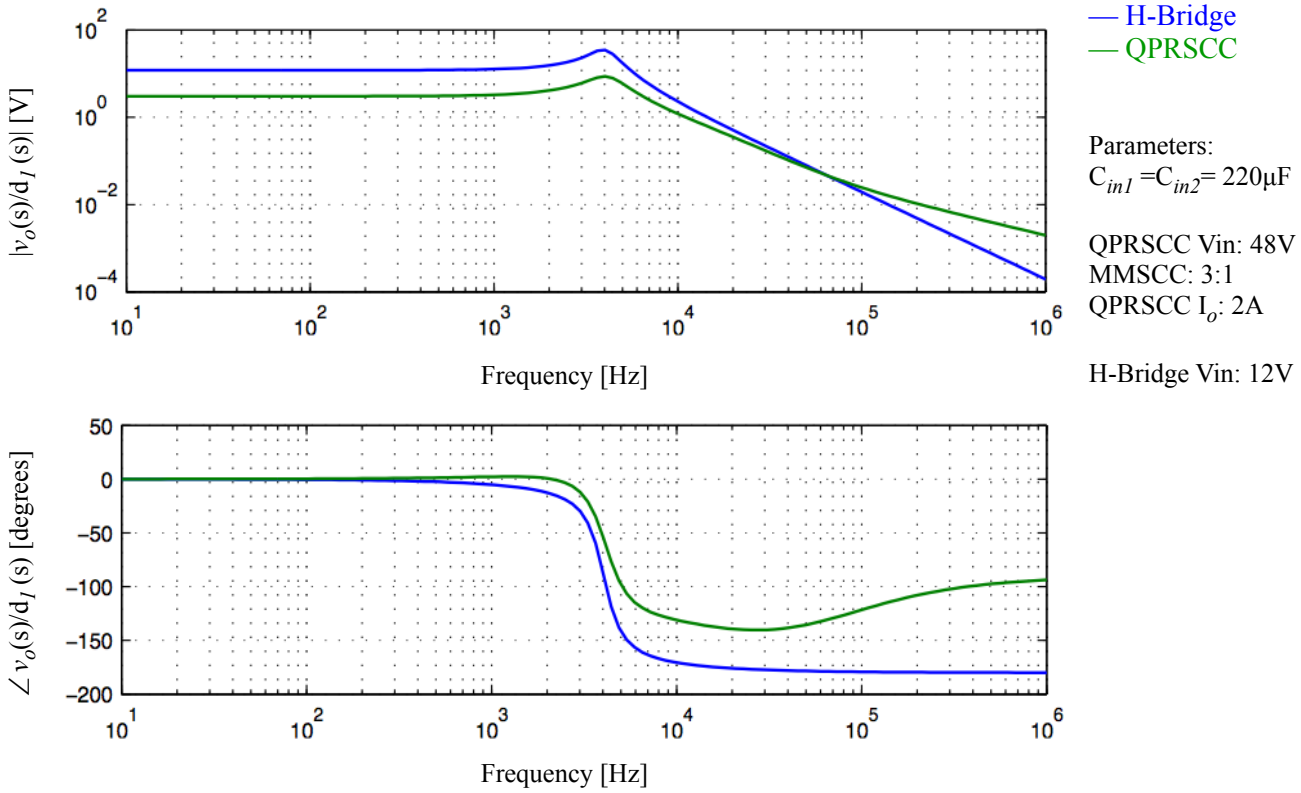


Fig. 4.35. Comparison of the frequency response of the QPRSCC and H-Bridge control-D_1-to-output voltage transfer function shows that the quasi-parallel configuration attenuates DC gain and adds a zero

The frequency response at key QPRSCC input voltages are plotted in Fig. 4.36 revealing no potential issues in terms of control design. The behavior of the QPRSCC control-to-output transfer function is as expected in the design of the H-Bridge converter or a buck converter. The largest effect on the magnitude of the frequency response is due to changes in the conversion ratios of the MMSCC. In 3:1 and 4:1 operation of the MMSCC decreases the resonant frequency and the associated magnitude at the peak. The most significant change is seen in the phase of the frequency response with the 2nd order effects most prominent with an input voltage of 8V for the H-bridge.

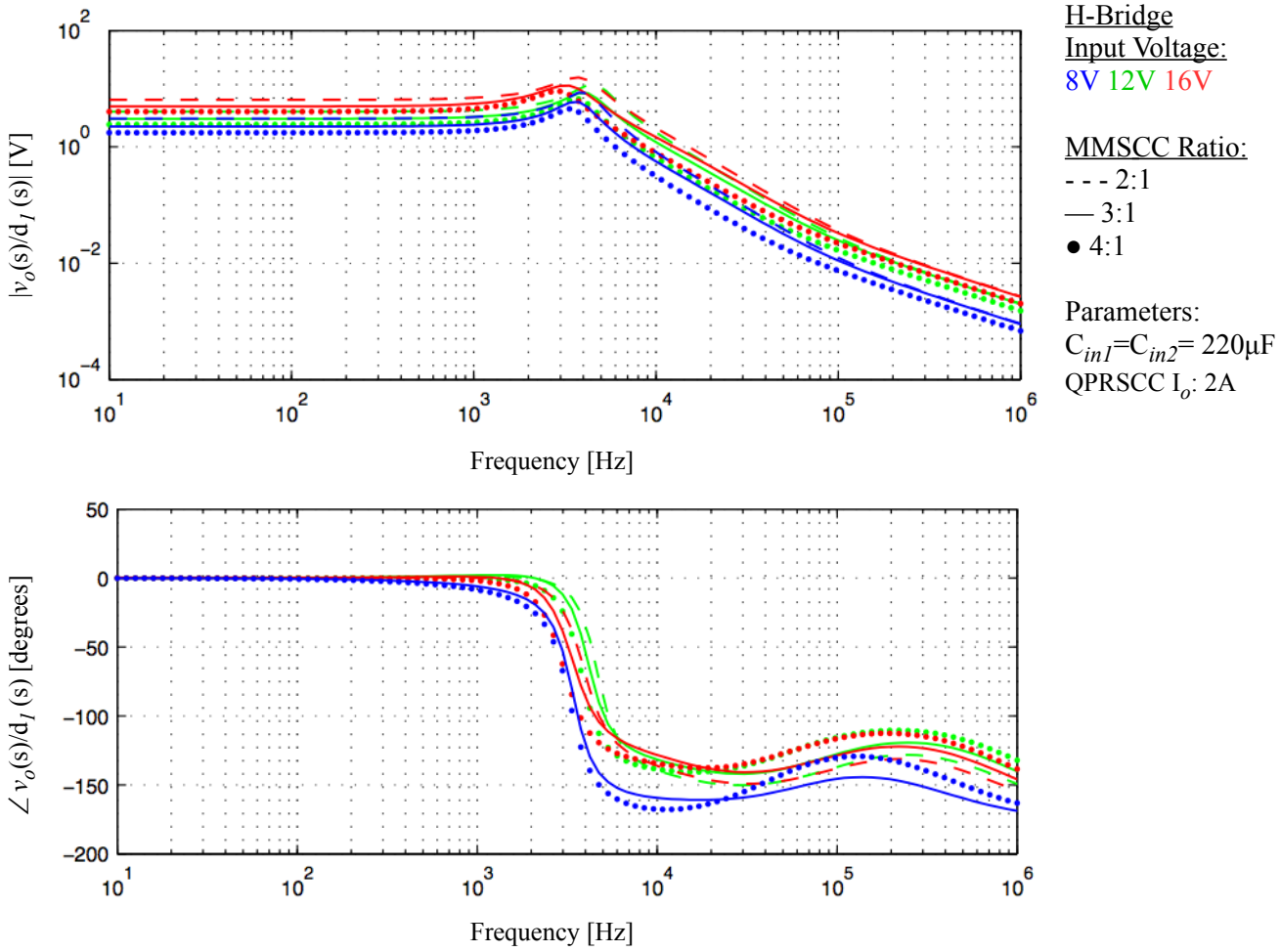


Fig. 4.36. The frequency response of the QPRSCC control-D_1-to-output voltage transfer function does not vary significantly across the QPRSCC input voltage range.

The QPRSCC control D_1-to-output voltage transfer function frequency response is evaluated at different load conditions. The QPRSCC is set at an operating point of 48V putting the H-Bridge in buck-boost mode with a conversion ratio of 1:2 and the MMSCC in 3:1. The load is varied from 1A to 10A in Fig. 4.37 showing no significant change to the frequency response.

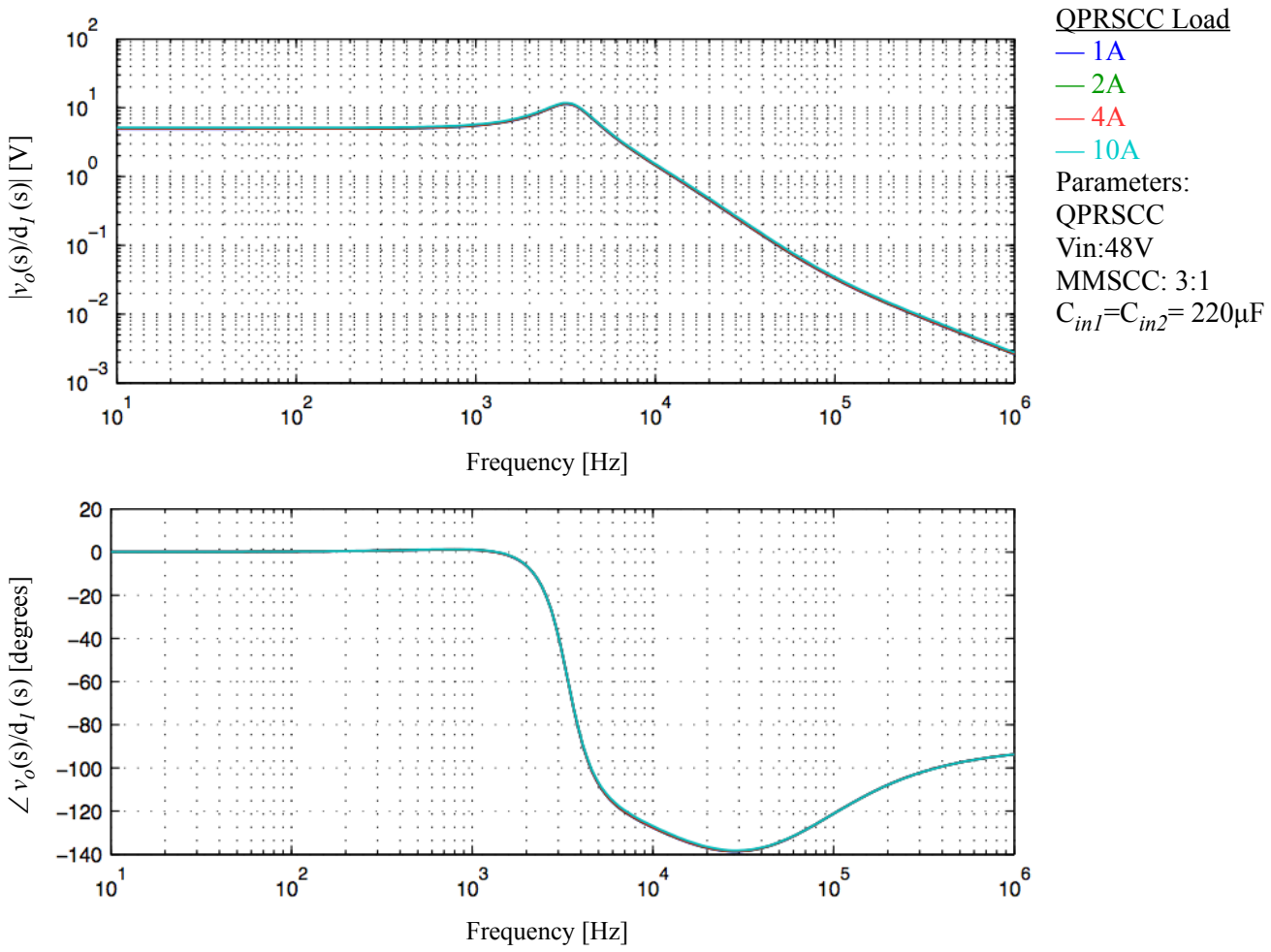


Fig. 4.37. The frequency response of the QPRSCC control-D_1-to-output voltage transfer function is not affected by different loads.

Lastly the effects of the input capacitors on the frequency response of QPRSCC control D_2 to output voltage transfer function are investigated. Inspection of the impedance network, Fig. 4.34(a), shows the individual capacitors C_{in1} and C_{in2} are combined so that the total input capacitance will affect the frequency response and not the ratio of the input capacitances. The QPRSCC frequency response of the buck control-to-output voltage transfer function is shown in Fig. 4.38. As the input capacitance increases, the resonant frequency seen in the QPRSCC frequency response decreases and is dampened. The QPRSCC control-to-output voltage frequency response behaves more like a first order system with larger input capacitance. As with the control duty ratio D_2 it requires a significant amount of capacitance and achieving more first order behavior is not necessary in terms of control.

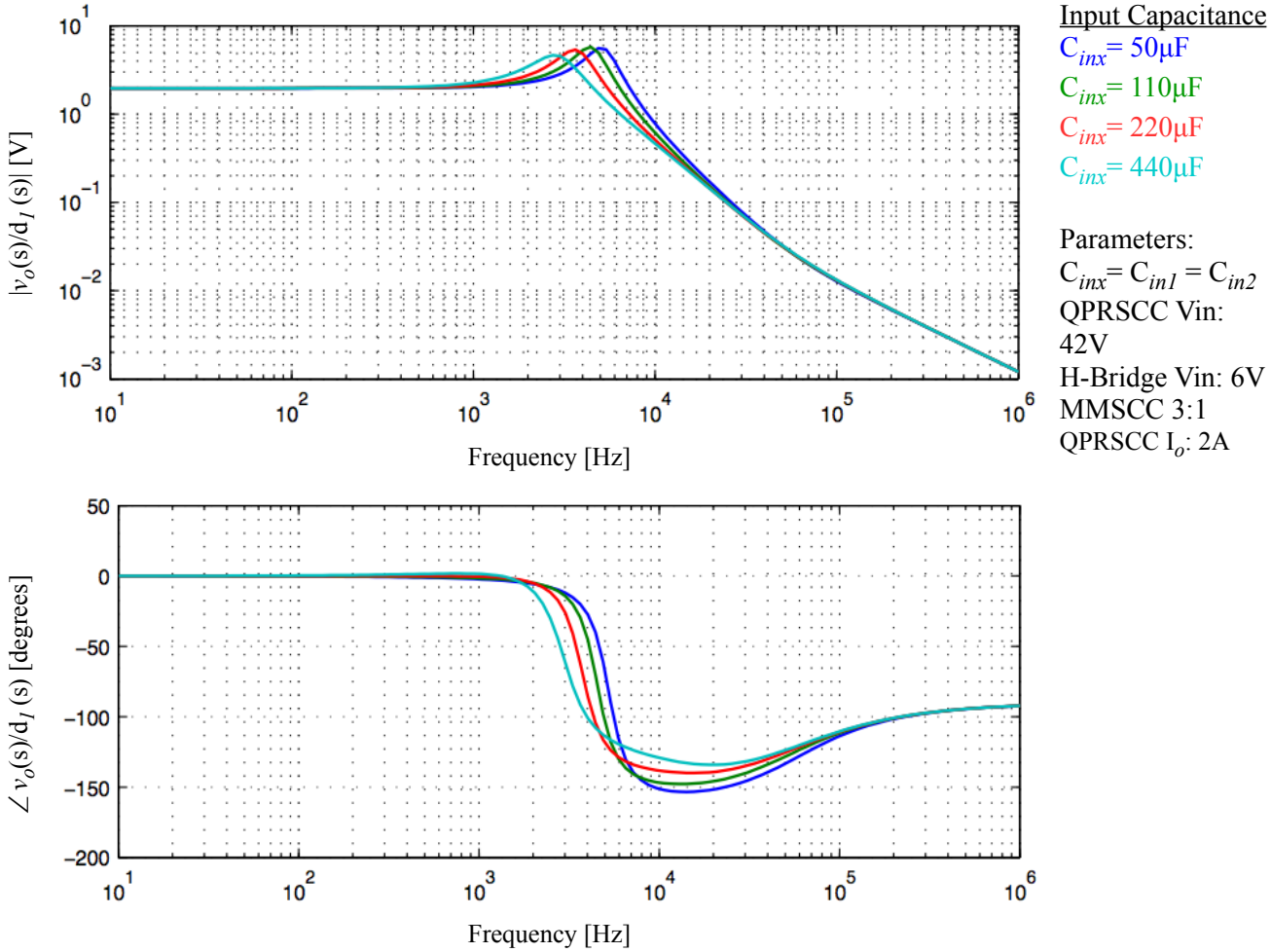


Fig. 4.38. QPRSCC control-D_1-to-output voltage frequency response as the total input capacitance is varied.

4.2.5 Conclusions of Small-Signal Analysis

The quasi-parallel configuration provides feedback within the power path adding a zero to the dynamic behavior of the QPRSCC. In each case, the QPRSCC exhibited some 2nd order behavior at a resonant frequency. The selection of input capacitance can provide damping causing the QPRSCC characteristics become more like that of a first order system. For the line-to-output voltage transfer function the QPRSCC can be approximated by a first order system with a high frequency phase of -90 degrees. At the resonant frequency it does reach a minimum of -150 degrees.

In terms of control of the QPRSCC, it is seen that with the quasi-parallel configuration the natural feedback attenuates the DC gain but also gives desirable approximate first order behavior. Again, 2nd order effects occur in the form of complex poles but the effects are generally mitigated by neighboring complex zeros. For the control duty ratio D_2 the RHP zero is still present but it now pushes the phase to

-180 degrees for the QPRSCC compared to -270 degrees for the H-Bridge. All analysis indicates that a control strategy implemented for the H-Bridge can be used to control the QPRSCC. This allows for commercial IC regulators to be used to control the QPRSCC.

4.3 Simulation of QPRSCC

The last section of this chapter will provide simulations of the designed QPRSCC in LTSpice. LTSpice enables simulation with an IC regulator (LT8705) which will be used in the hardware prototype. The input capacitors are set as C_{in1} = 120µF C_{in2} = 50µF for simulations based off the previous analysis and by normal input ripple requirements. Simulations will be performed to show that the LT8705 and the designed QPRSCC can achieve a regulated steady state voltage in section 4.4.1. Following steady-state evaluation both load and line transients tests will be simulated and covered in section 4.4.2 demonstrating the excellent load dynamic properties of the QPRSCC.

4.3.1 Steady State Simulation of the QPRSCC

A SPICE circuit model is developed in LTSpice (the schematic can be seen in Appendix C). The MMSCC MOSFETs are represented with switch elements with an on resistance corresponding to the R_{dson} of the MOSFETs with a 40°C temperature rise. The H-Bridge is simulated with the LT8705, an inductor, and MOSFET SPICE models taken from the manufacturer's websites. A SPICE block is created that will turn on and off the MMSCC modules depending on the input voltage such for an increasing voltage the MMSCC will operate from 2:1 to 3:1 and from 3:1 to 4:1 at 40V and 52V. The same voltages are used to turn off modules with decreasing input voltages.

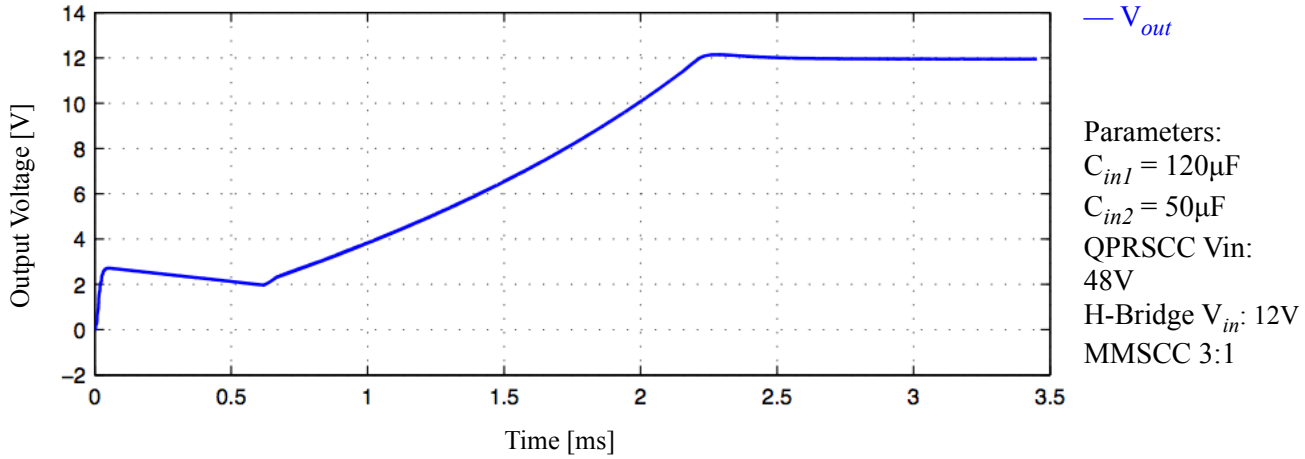


Fig. 4.39. Start-up of the QPRSCC using the LT8705 soft-start feature.

The start up of the QPRSCC with a input voltage of 48V is shown in Fig. 4.39, demonstrating the LT8705 can provide steady state regulation for the QPRSCC. It highlights the soft start feature offered by the LT8705, shown to start just past 0.5ms. The soft start prevents high currents flowing through the inductor and promotes a well-behaved start up. Simulations with input voltages of 36V, 48V, and 72V also achieve the steady state output voltage of 12.1V as shown in Fig. 4.40. As noted in section 3.3 for the design of the H-Bridge, the chosen feedback resistors would result in regulated output voltage of 12.1V, which is accurate enough for most 12V applications.

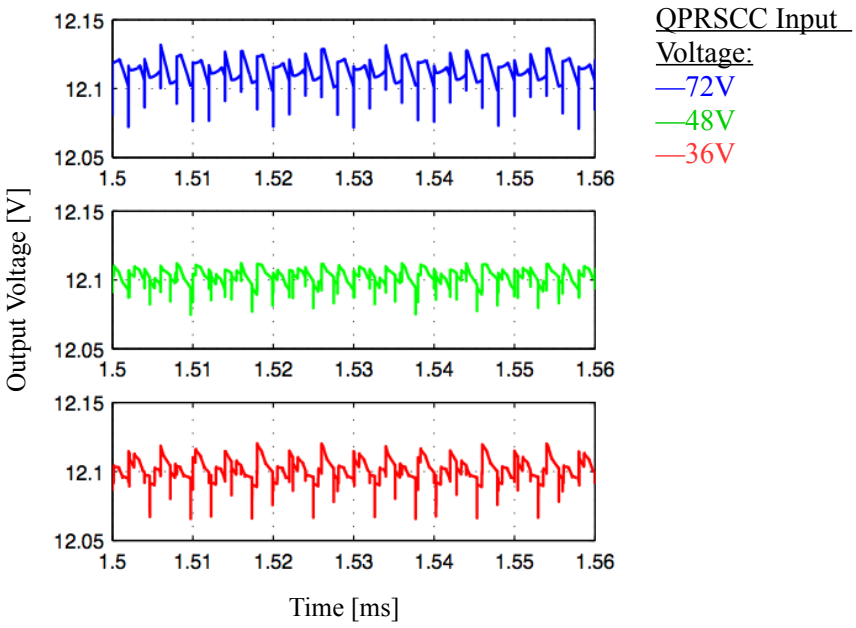


Fig. 4.40. QPRSCC reaches steady-state output voltage for different input voltages.

The input voltage of the H-Bridge is plotted in Fig. 4.41 showing a constant voltage at the expected voltages of 12V, 12V, and 24V for the QPRSCC input voltages of 36V, 48V, and 72V. The percentage of power processed by the H-Bridge is equivalent to the ratio of the H-Bridge input voltage to QPRSCC input voltage. For the QPRSCC input voltages of 36V, 48V, and 72V the H-Bridge should handle 1/3, 1/4, and 1/3 respectively of the total power. The inductor currents should then be approximately 1.6A, 1.25A, and 1.6A for a 5A load for the QPRSCC. The plotted inductor currents (Fig. 4.41) confirm that the H-Bridge is converting only a portion of the total power.

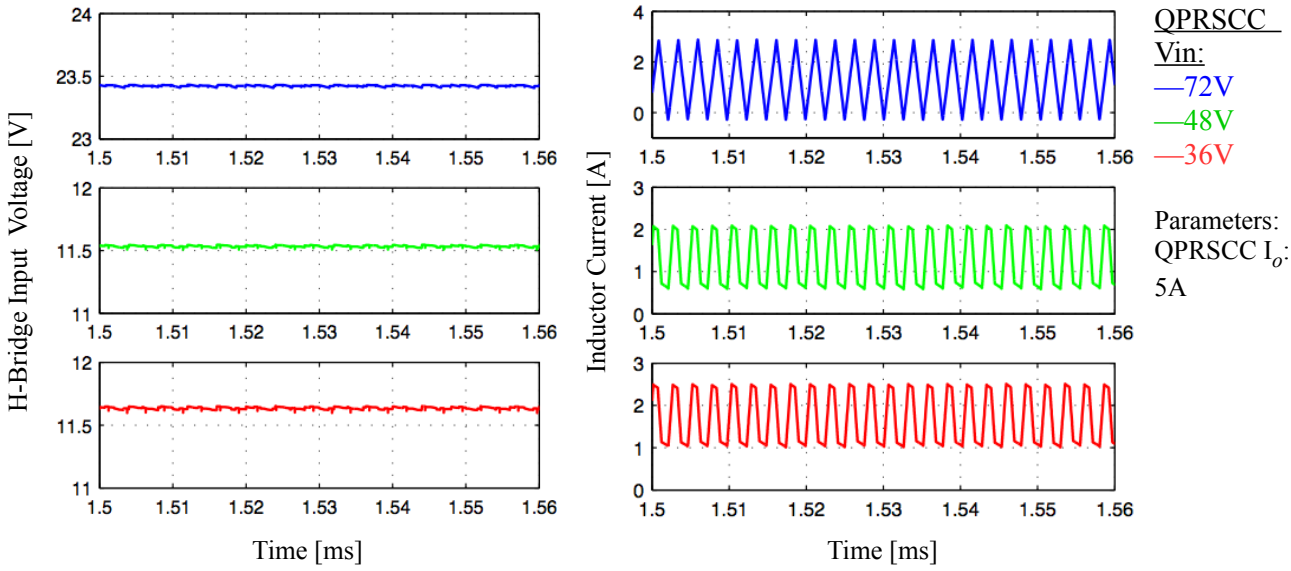


Fig. 4.41. The steady-state H-bridge input voltage and corresponding inductor current for different QPRSCC input voltages confirms partial power properties.

Simulations confirm that the LT8705, subsequently control of the H-Bridge, can provide regulation for the QPRSCC and reach the desired steady state operation.

4.3.2 Transient Simulations

The response of the regulated QPRSCC to load and line transients were also simulated. Analysis of the QPRSCC, indicates that it will have excellent and well behaved behavior in response to load transients. It is expected that the MMSCC, with a lower output impedance, will provide the majority of the current during the transient. Ideally the H-Bridge inductor current ideally will have a first order response rising to the needed steady state current. In terms of line transients, the choice of input capacitance will affect the QPRSCC response. The lower capacitance will provide higher bandwidth but increased 2nd order oscillatory behavior. The regulation provided by the LT8705 should eliminate the oscillatory behavior and will benefit from the higher bandwidth provided by lower input capacitance. The input capacitors are selected as C_{in1} = 120µF C_{in2} = 50µF for the following transient tests.

The QPRSCC is operated with an input voltage of 48V and given a load step from 10% to 100% and then back down. The voltage response is excellent staying within ±150mV of the regulated 12.1V as seen in Fig. 4.42. Inspection of the inductor current shows limited overshoot of the steady state current. Tuning of the LT8705 compensation network may further reduce the overshoot, but it is not a major concern.

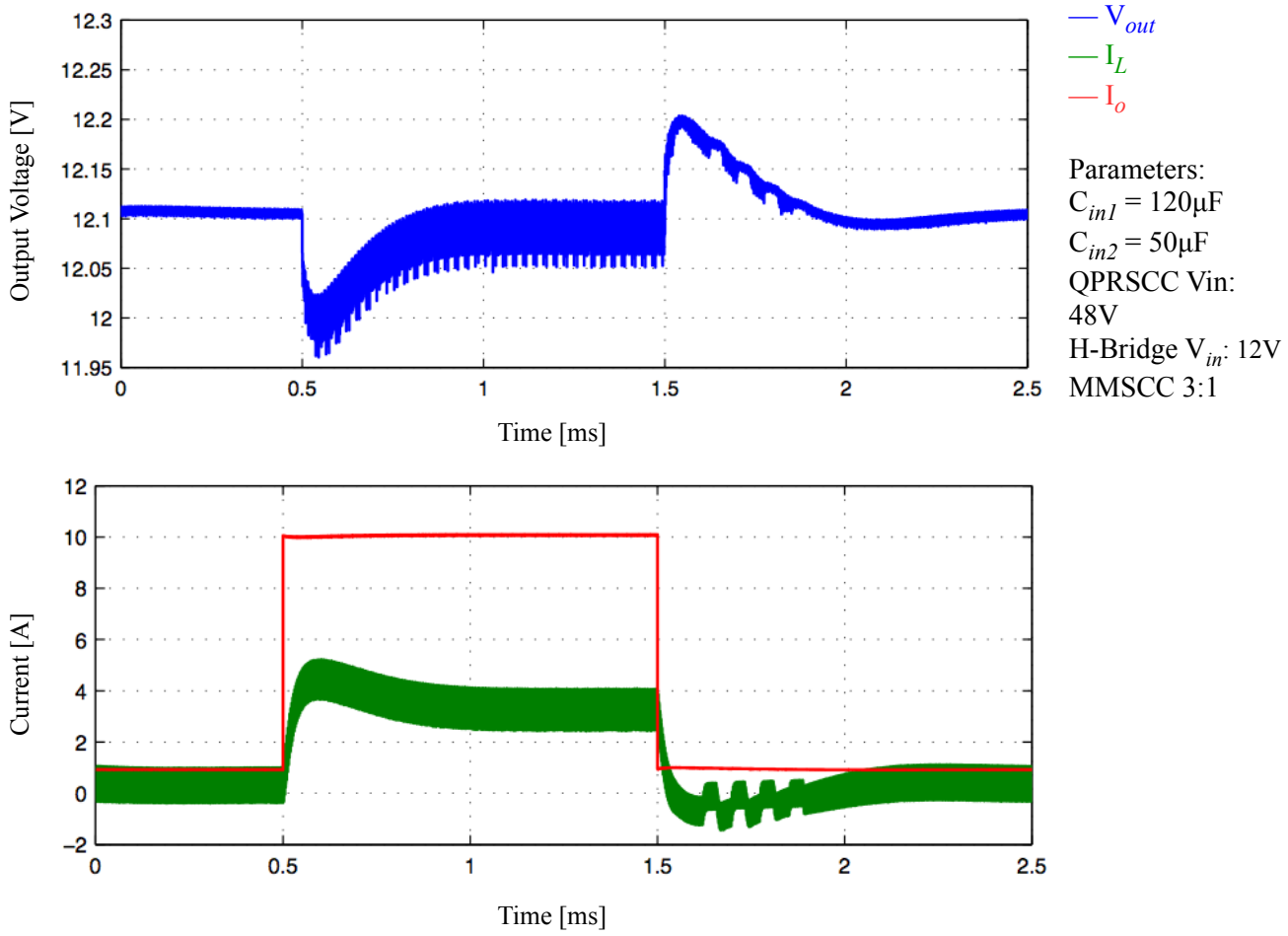


Fig. 4.42. QPRSCC load is stepped from 10% to 100% and vice versa showing excellent transient response.

The input voltage of the QPRSCC is stepped and ramped from 42V to 52V keeping the MMSCC in 3:1 operation. The transient response for the line step and line ramp are shown in Fig. 4.43 and Fig. 4.44 respectively. The output voltage stays within 10% of the 12V but larger input voltage steps may prove to be problematic, however input voltages rarely change in a step fashion but and ramp changes are more commonly seen in terms of transients on line voltages. Given an input voltage ramp, the QPRSCC transient behavior is excellent, varying less than 80mV as seen in Fig. 4.44. The major changes in the output voltage response is due to the H-Bridge changing from boost to buck-boost and finally to buck mode of operation.

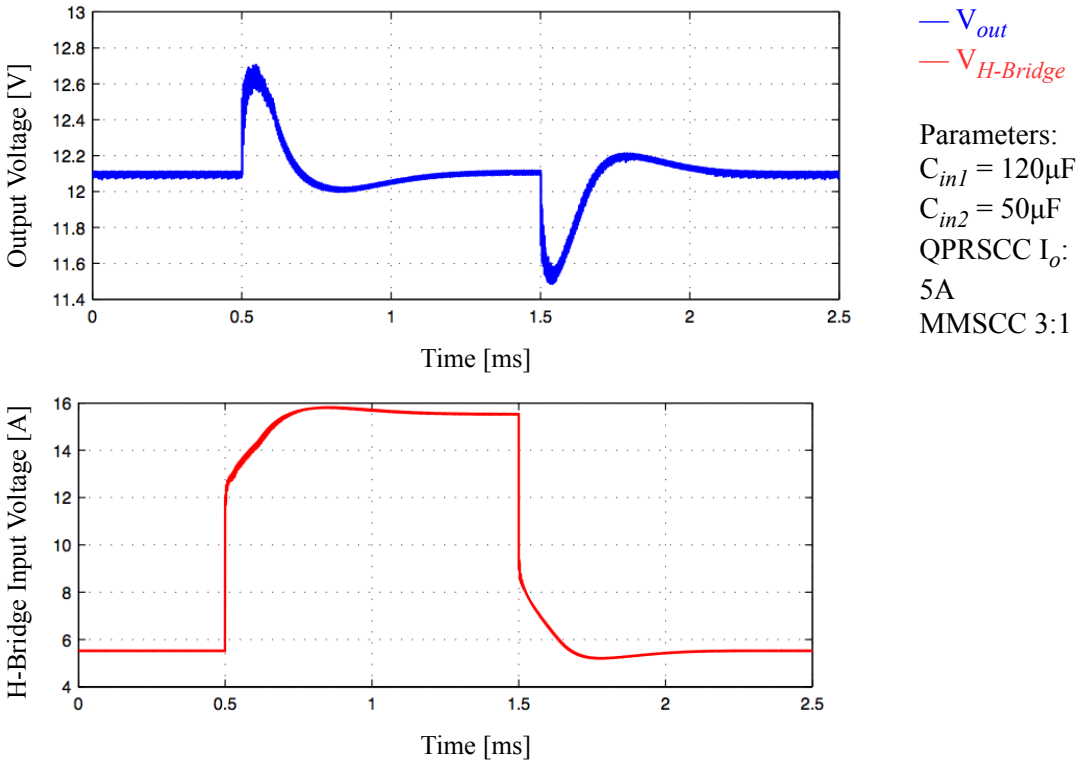


Fig. 4.43. QPRSCC output voltage response to line voltage step from 42V to 52V.

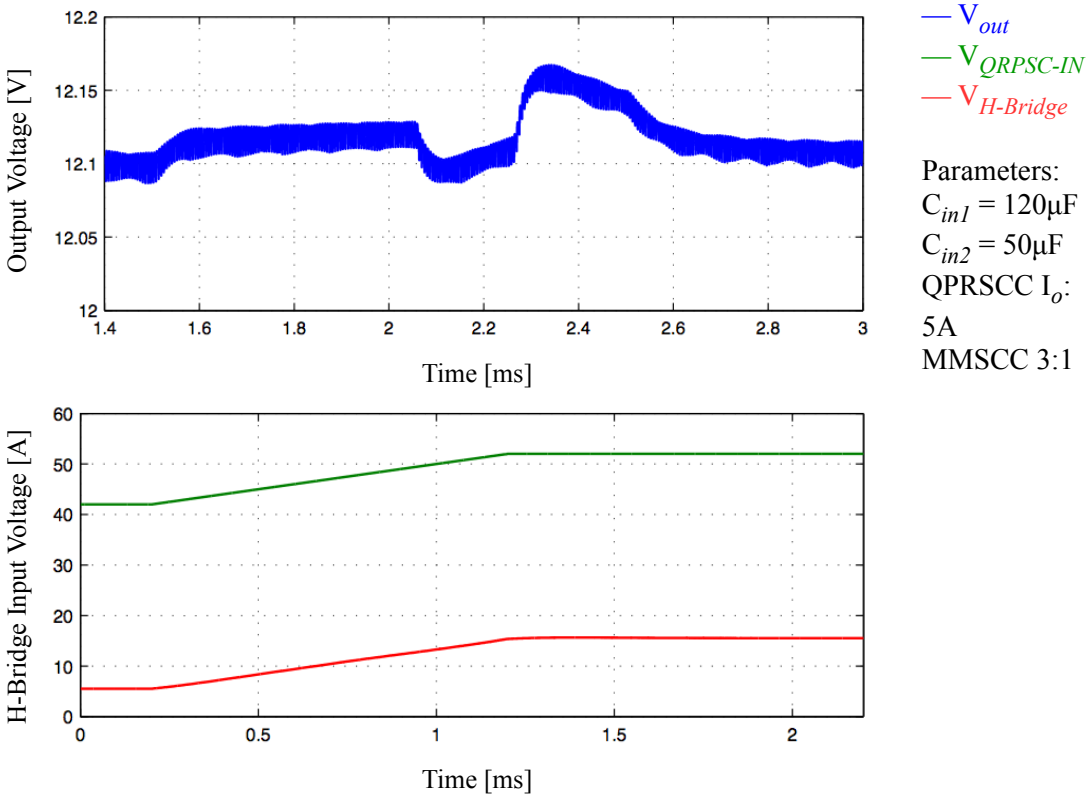


Fig. 4.44. QPRSCC output voltage transient response to line voltage ramp from 42V to 52V.

4.4 Calculated Efficiency

The losses of the QPRSCC can be divided into losses due to the MMSCC and the losses due to the H-Bridge. The losses will be evaluated separately and then combined to look at the total efficiency of the QPRSCC. Again, the estimated efficiency does not take into account parasitic impedances due to the PCB board.

4.4.1 Switched-Capacitor Converter Losses

For the MMSCC, there are conduction losses, switching losses, and power lost due to the gate drivers and control circuitry. The gate drive and control circuitry should be fairly efficient and add negligible losses in comparison to the power losses. This assumption will appear as minor errors in estimation at light loads.

The conduction losses are estimated using the approximate output impedance found in section 3.2. This output impedance includes capacitive and resistive losses of the MMSCC. The output current of the MMSCC is dependent on the ratio of the input voltage of the MMSCC to the QPRSCC. The conduction losses of the MMSCC for N:1 conversion ratio is estimated as (4.83).

$$P_{cond}^{N:1} = \left(\frac{V_{\text{MMSCC-IN}}}{V_{\text{QPRSC-IN}}} I_o \right)^2 R_O^{N:1} \tag{4.99}$$

The switching losses of a SCC, as discussed earlier, include output capacitance losses, resistive turn on losses, and gate capacitance losses. The turn-on of the MOSFET, sans significant parasitic inductance, is resistive in nature due the absence of inductors. The MOSFET output capacitance and gate charge losses are approximately fixed and depend on the device parameters. The turn-on loss depends on the output capacitance and the current waveform. The design of the MMSCC put it near the fast switching limit, which means it should have partial charging or no charging current waveforms. An example of these wave forms are depicted in Fig. 4.45. In the fast switching limit, the capacitor's voltage varied little and capacitors experience no charging (NC) giving square waveforms for the current. The design of the MMSCC puts it on the cusp of the FSL and the capacitors experience partial charging (PC).

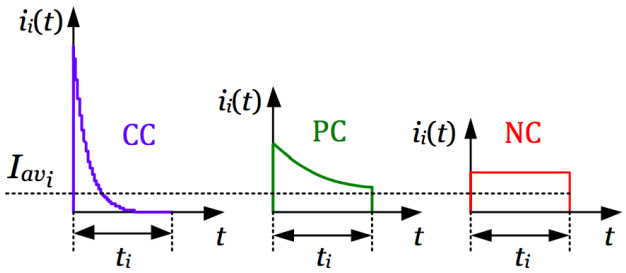


Fig. 4.45. Current waveforms for charging capacitors in the complete charging (CC), partial charging (PC), and no charging (NC) modes [11].

For the SCC with PC, the peak current can be calculated using the techniques in [11]. Using these techniques, the turn-on losses can be approximated for different output currents. The turn-on loss is dependent on the blocking voltage and the peak current is estimated by (4.84).

$$P_{turn-on} = \frac{t_{on}}{6} V_{DS-OFF} I_{pk} f_{sw} \tag{4.100}$$

The gate charge losses associated with the MOSFETs, AON6280 and the PSMN3R9, chosen for the MMSCC are given in (4.85) and (4.86) respectively. The gate drive and control circuitry will be estimated to consume roughly 0.25W.

$$P_{g-AON} = V_{drive} Q_G f_{sw} = 12\text{V}(60\text{nC}) f_{sw} \tag{4.101}$$

$$P_{g-PSMN} = V_{drive} Q_G f_{sw} = 12\text{V}(21.5\text{nC}) f_{sw} \tag{4.102}$$

Lastly the output capacitance losses of the AON6280 and the PSMN3R9 are calculated as (4.87) and (4.88) respectively.

$$P_{Coss-AON} = \frac{1}{2} C_{oss} V_{DS-OFF} = ¿ \tag{4.103}$$

$$P_{Coss-PSMN} = \frac{1}{2} C_{oss} V_{DS-OFF} = ¿ \tag{4.104}.$$

The total gate charge losses and output capacitance losses associated with the switching MOSFET will depend on the MMSCC conversion ratio. With different conversion ratios, there is a different number of MOSETs switching. The total switching losses can be calculated by (4.89) where n is the conversion ratio for n:1.

$$P_{SW} = (1+3n) P_{turn-on} + \begin{cases} 6 & \text{for } 4:1 \\ 5 & \text{for } 3:1 \\ 4 & \text{for } 2:1 \end{cases} (P_{g-AON} + P_{Coss-AON}) + \begin{cases} 7 & \text{for } 4:1 \\ 4 & \text{for } 3:1 \\ 2 & \text{for } 2:1 \end{cases} (P_{g-PSMN} + P_{Coss-PSMN}) \tag{4.105}$$

The calculated efficiencies of the MMSCC plotted for different output currents in Fig. 4.46 show poor efficiencies at loads less than 2A. As the output current increases so does the MMSCC efficiency. Each

conversion ratio of the MMSCC achieves 95% past 5A (50% load). Unlike typical converters with inductors the conduction losses are fixed for a SCC and the switching losses are greatly reduced due to the resistive loads (not inductive). This leads to overall high efficiencies that do not necessarily decrease with higher output currents.

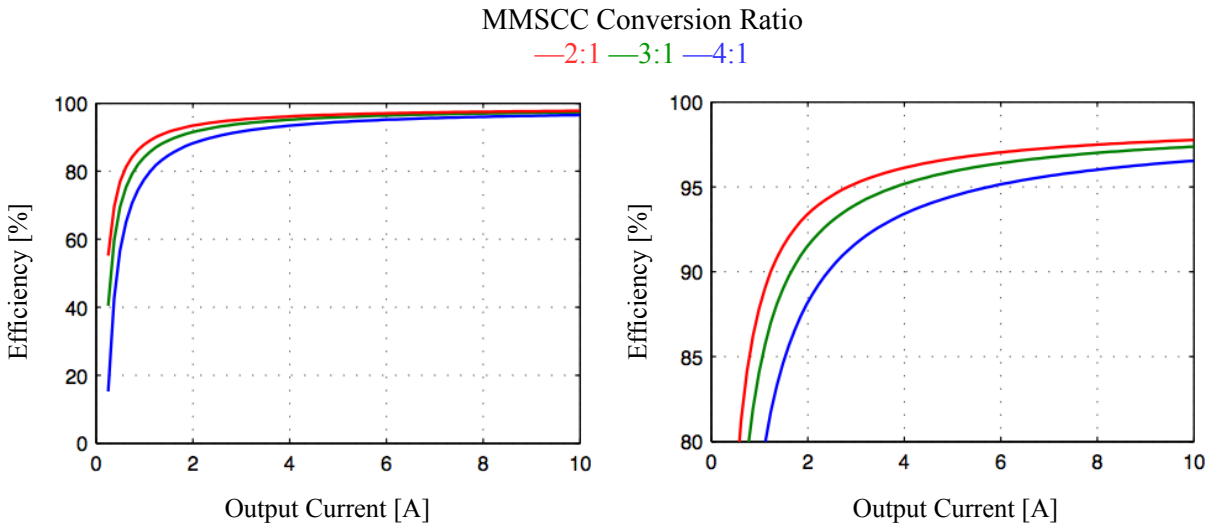


Fig. 4.46. Calculated efficiency of the MMSCC as a function of output current

4.4.2 H-Bridge Losses

The H-Bridge will have losses from conduction, switching, and the losses associated with the control chip LT8705. The sources of conduction losses are due to the MOSFET $R_{ds\text{-}on}$ and the inductor DC resistance. The RMS current can be calculated from the inductor current, duty ratios, and inductance. The inductor current can be calculated with (4.90). The duty ratio is taken from the steady state operation of the H-Bridge in LTSpice at 36V, 48V, and 72V and the inductance is derated from its designed value of 4.7µH by 70% to calculate the ripple current in the H-Bridge.

$$I_c = \frac{M}{R_{th} D_1} V_o = \frac{1}{R_{th}} \left(\frac{V_o}{n D_1 + D_2'} \right) \tag{4.106}$$

The switching losses for the H-Bridge are discussed briefly in the LT8705 application notes but are similar to losses in typical buck and boost converters. The turn on and turn off losses are inductive and typically the one of the pair of switches (on the buck or boost side) operates with soft switching due to the body diode. The drawback is the body diode adds diode reverse recovery losses. The gate charge and output capacitance losses are calculated as in the MMSCC. The switching losses are assumed to be a linear inductive turn-on and calculated with (4.91). The reverse recover loss is calculated with

(4.92).

$$P_{sw} = \frac{(t_{on} + t_{off})}{2} V_{DS-OFF} I_{pk} f_{sw} \tag{4.107}$$

$$P_{QRR} = Q_{RR} V_{DS-OFF} f_{sw} \tag{4.108}$$

The efficiency of the H-Bridge for QPRSCC input voltages of 36V, 48V, and 72V are plotted in Fig. 4.47. At light loads the H-Bridge has an efficiency less than 80%. At higher loads, the efficiency increases past 90% and settling around 95%. This efficiency is more than acceptable as the efficiency of the QPRSCC will depend more on the MMSCC than the H-Bridge. This efficiency is nominally what the LT8705 datasheet states. More than likely light load efficiencies can be increased by not forcing continuous conduction mode and utilizing Linear Technologies "Burst Mode".

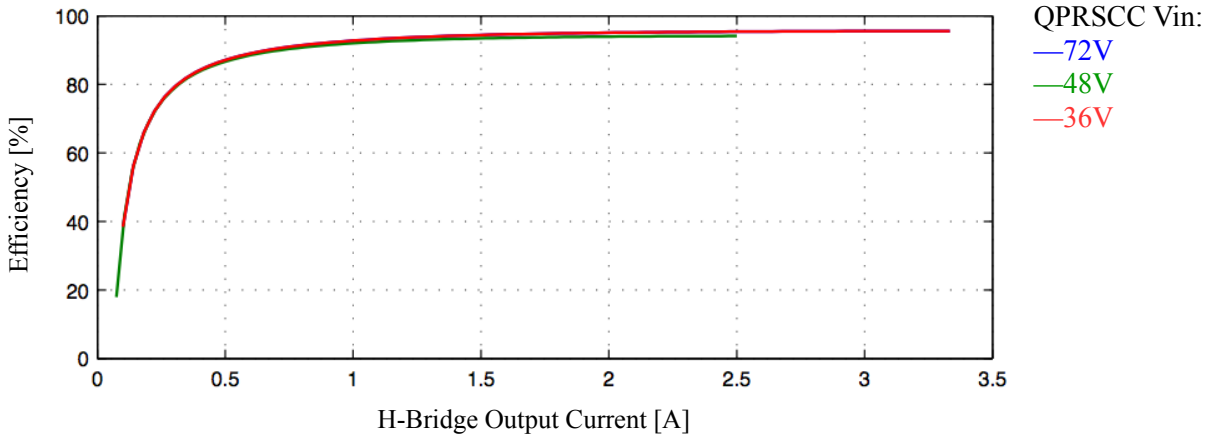


Fig. 4.47. Calculated Efficiency of the H-Bridge

4.4.3 Calculated Total Efficiency

The losses of the H-Bridge and MMSCC are combined to find the calculated net efficiency of the QPRSCC. The calculated efficiency is plotted up to the prototypes full power of 120W in Fig. 4.48. At loads less than 2A the QPRSCC has efficiencies under 80%, being heavily affected by the switching losses associated with the SCC. At 3A the QPRSCC efficiency is above 90% regardless of the QPRSCC input voltage. Details in Fig. 4.49 reveal that the QPRSCC should achieve efficiencies of 93% to 95%.

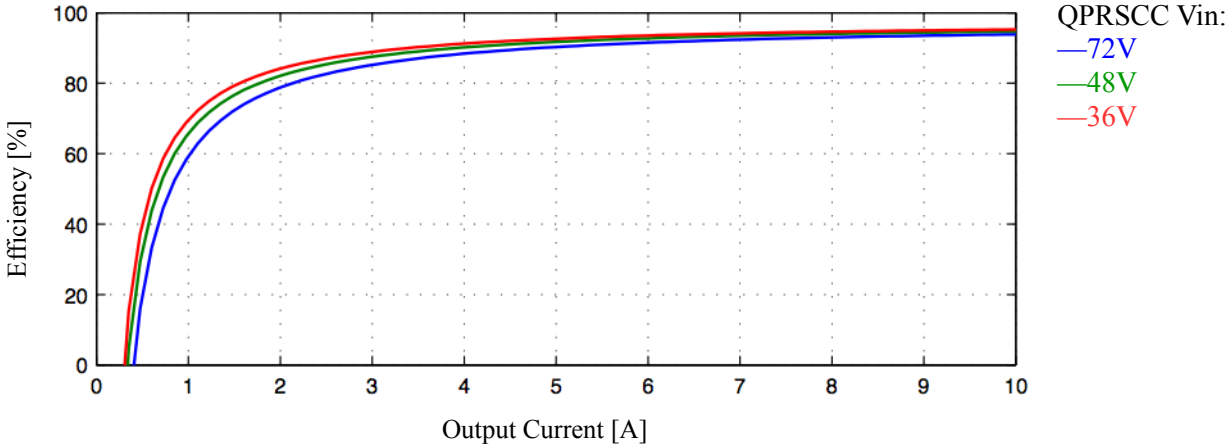


Fig. 4.48. Calculated Efficiency of the QPRSCC

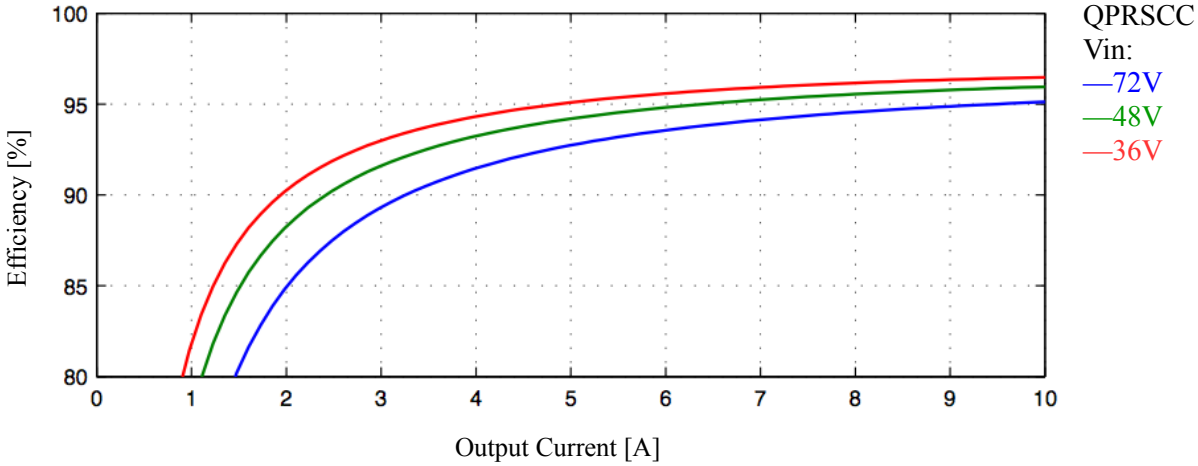


Fig. 4.49. Detailed view of QPRSCC calculated efficiency

Chapter 5 Experimental Results

A 120W half brick sized prototype of the quasi-parallel regulated switched-capacitor converter (QPRSCC) was constructed. The choice of input capacitance and gate drive for the switched-capacitor converter (SCC) will be covered in section 5.1. Design of the 2 layer PCB will be discussed in section 5.2. The PCB is larger than required due to time constraints and the over-design of the SCC. Tthe unregulated operation of the multilevel modular switched-capacitor converter (MMSCC) is presented in section 5.3. The SCC is operated in steady state in 2:1 and 3:1 modes of operation in order to evaluate the load line and converter efficiency. Next the H-Bridge efficiency is evaluated in section 5.4. In section 5.5 the performance of the QPRSCC operating in 2:1 and 3:1 modes will be evaluated in terms of efficiency, load transients, and line transients.

5.1 Input Capacitor Selection, SCC Gate Drive, and Microcontroller

In sections 3.2 and 3.3, both the MMSCC and H-Bridge were designed and their respective power components selected (i.e. the inductor, the MOSFETs, the switching capacitors, and the output capacitance). The output capacitance of the QPRSCC was designed to meet the requirements of the SCC which exceed the requirements of the H-Bridge. This leaves the input capacitance, the SCC gate drive, and the microcontroller to control the SCC to be selected.

The input capacitors C_{in1} and C_{in2} must be large enough to keep the voltage for the MMSCC or H-bridge relatively stable over a switching period. Analysis in Chapter 4 indicated that low capacitance would lead to higher bandwidth in the frequency response of the control-to-output transfer functions. The analysis of the line-to-output voltage transfer function indicated that having a smaller C_{in2} compared to C_{in1} would passively reduce the effect of higher frequency (past 5kHz) changes in the input voltage on the output voltage. Given this, selected capacitances were C_{in1} = 120µF and C_{in2} = 70µF. Simulations in section 4.3 demonstrated that these choices would be adequate.

One of the biggest challenges in using a SCC is driving numerous MOSFETs. The MMSCC was selected over other SCC topologies since 8 of the MOSFETs can be driven by a typical synchronous PWM driver as shown in Fig. 5.1. An unregulated MMSCC operates with each phase having a 50% duty cycle. A single PWM input gate driver can be used to drive a pair of MOSFETs (circled in Fig.

5.1) synchronously from a single signal decreasing the number of signals to be routed on the PCB. Also these MOSFETs (indicated in Fig. 5.1) can be driven with typical boot strap methods utilized in typical buck converters. This leaves the five floating MOSFETs, S_1, S_2, S_5, S_8, and S_{11}, that require isolated gate drivers and a voltage source to provide the driving voltage.

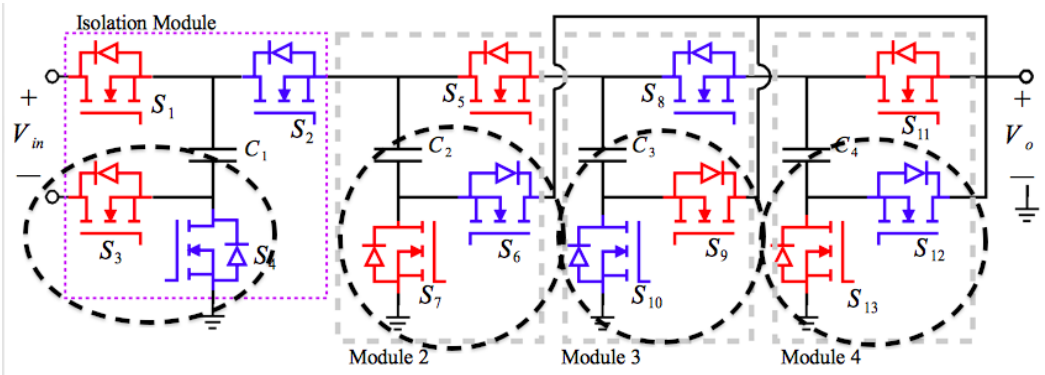


Fig. 5.1. The MOSFETs circled here can be driven by single high-side/low-side synchronous gate driver

Our first approach was to identify if any of the voltages present within the MMSCC are suitable to provide the necessary driving voltage for the floating MOSFETs. It was decided that this approach would be to complex. In the end, the floating MOSFETs driving voltage was generated by using a Texas Instruments unregulated isolated 12V IC's, DCP021212DP, which was combined with a bootstrap method to generate driving voltages for various switches as shown in Fig. 5.2.

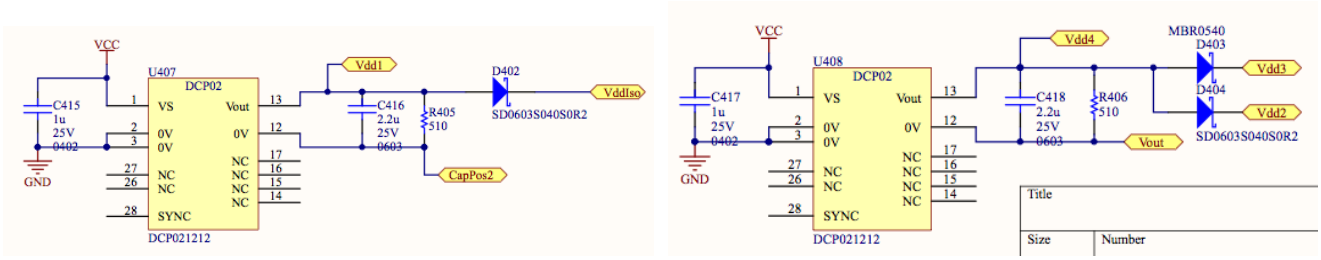
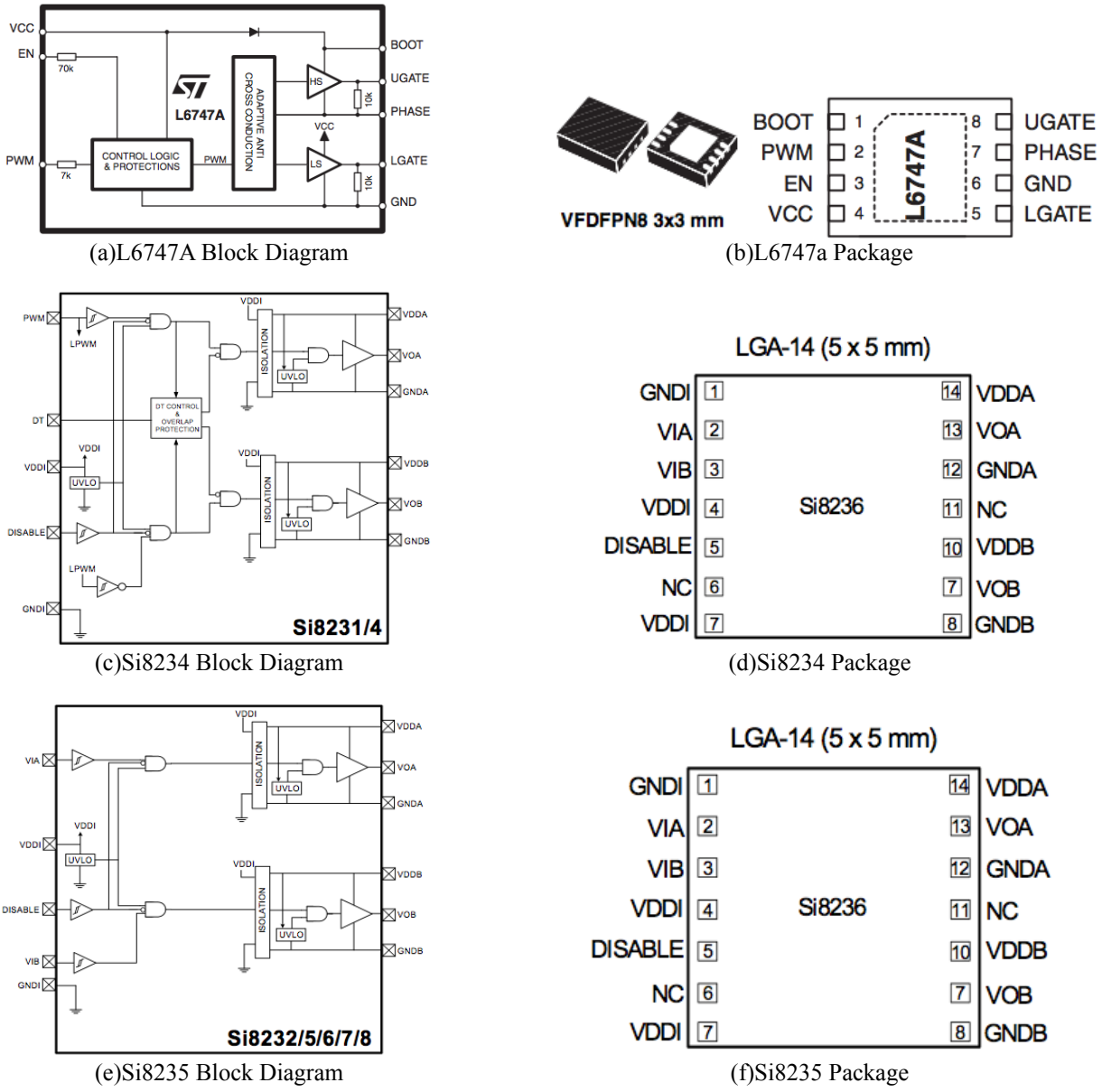


Fig. 5.2. Power sources for the floating MOSFETs driving voltage

The gate drivers selected were chosen for their small package size as well as their ability to drive multiple MOFETs. For the MOSFETs indicated in Fig. 5.1, gate driver L6747a was chosen with a package surface area of 3.3x3.3mm. The L6747a (Fig. 5.3(a)) also offers the ability to send an “enable” signal to turn on and off the gate driver, and the modules used to change the MMSCC conversion ratio. For the floating MOSFETs the gate drivers Si8234 and Si8235 were selected (Fig. 5.3(c)&(e)). The Si8234 is able to drive two MOSFETs from a single PWM input (MOSFETs S_2 and S_5 as labeled in

Fig. 5.1). In order to turn on and off modules the switches S_8 and S_{11} are driven with an Si8235 which has two independent isolated gate drivers in a single package. The gate drivers and the package dimensions are depicted in Fig. 5.3.



(a)L6747A Block Diagram (b)L6747a Package

(c)Si8234 Block Diagram (d)Si8234 Package

(e)Si8235 Block Diagram (f)Si8235 Package

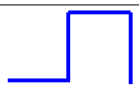
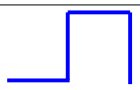
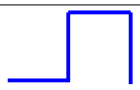
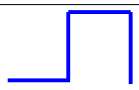
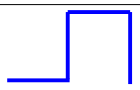
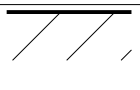
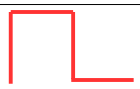
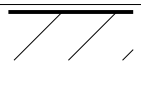
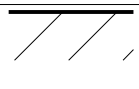
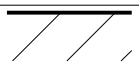
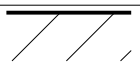
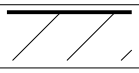
Fig. 5.3. MMSCC Gate Drivers (a,c,e) block diagrams and the (b,d,f) corresponding package dimension

The microcontroller, MSP430f5510 was selected to control the MMSCC because the launchpad and evaluation board were previously purchased in our research group. Our group had experience with this IC, which simplified programming the IC. It met our basic requirements: it could sense the input voltage, could produce multiple signals, and produce high frequency PWM signals.

A total of 6 different signals are necessary to operate the MMSCC for our purposes. Two signals are

needed to produce the 50% duty cycles for Phase 1 and Phase 2 for the MMSCC. Two more signals are needed for the floating MOSFETs S_8 and S_{11}, one will be Phase 1 and the other Phase 2. The modules need to be bypassed in order to alter the conversion ratio from 4:1 to 3:1 to 2:1, so these two signals will need to be set to a constant ON, i.e. 100% duty cycle, instead of the previous 50% duty cycle. The last two signals required will be the ENABLE signals sent to the gate drivers for the bottom MOSFETs pairs S_9 / S_{10} and S_{12} / S_{13} to turn on and off the modules as the conversion ratio changes. A summary of the signals and their necessary signals are shown in Table 5.1. Signals EN MOD3 and EN MOD4 are the enable signals sent to the L6747a that drive module 3 and module 4 respectively as labeled in Fig. 5.1.

TABLE 5.1: SUMMARY OF GATE DRIVE SIGNALS AND ENABLE SIGNALS FROM THE MICROCONTROLLER

Signal Name	Waveform		
	4:1	3:1	2:1
Phase 1			
Phase 2			
S_8			
S_{11}			
EN MOD3			
EN MOD4			

In the PCB design, a resistor divider with a bottom capacitor is included to reduce the input voltage to a voltage that can safely be sampled with the microcontroller's analog to digital converter (ADC). During operation, the microcontroller is programmed to sample the input voltage and once it reaches 40V or 52V to switch the MMSCC the next conversion ratio accordingly.

5.2 Overview of Operation and PCB Design

The Altium software package was used to create schematics and for PCB layout. There were several objectives for the PCB design:

1. Utilize a 2 layer PCB board. The top layer will host the power components while the bottom layer hosts the control components such as the LT8705, gate drive, and

microcontroller.

2. Place the Power Input and Output near each other to minimize the power path. Place them on the same side so the converter could in future reversions be plugged into another board allowing modularity and increased power ratings.
3. Keep the connections between MOSFETs and switching capacitors in the SCC as close as possible to minimize parasitic inductance.
4. Utilize parasitic inductance by increasing PCB track length from the SCC to form a small filter with the input capacitance and the output capacitance to help mitigate the large di/dt from the SCC.
5. Allow for adjustment of input capacitance, output capacitance, and switching capacitance. Due to limited experience with SCC having the ability to increase the capacitance on the SCC will allow for some flexibility.

The schematics are presented so as to separate logical groupings of components, such as gate drive, MMSCC, H-Bridge, microcontroller, and bulk capacitors. The full schematics and each PCB layer can be seen in Appendix D. The PCB design for the top layer is shown in Fig. 5.4 and the bottom layer in Fig. 5.5. In Fig. 5.4, the dimensions of the power converter (all components and active copper) are outlined by the green silkscreen and fit within the half brick dimensions (2.3″x2.4″). The switching capacitors C_1, C_2, C_3, and C_4 are made up of several individual ceramic capacitors. In order to prevent long rows of capacitors and awkward placements of the MOSFET and gate drive, the capacitors are placed in box formation. This box formation has their capacitors tightly packed with their “positive” sides facing out to each side and their “negative” side in the middle of the box. This enabled for the MMSCC to be laid out in a compact fashion with adequate room for the H-Bridge components. Inspection of Fig. 5.4 reveals that the MMSCC takes up about 60% of the space which is reasonable, since it will handle at least 60% of the power.

The power input is on the upper right hand side of the board (Fig. 5.4). The input sees parasitic inductance of a few nanoHenries prior to the input capacitors of the MMSCC. Power flows through the MMSCC, then out to the bottom side, where there are output filter capacitors. Again, the trace length is meant to provide parasitic inductance to smooth out potential di/dt created by the MMSCC. The output of the board is near the input in the upper right hand corner (Fig. 5.4). The H-Bridge is near the inductor and its output is located close to the board power output. The H-Bridge has three of its output

filter capacitors close by to provide local capacitance without parasitic inductance. The MOSFET placement is not obvious in Fig. 5.4, but can be seen easily in Appendix D.

As mentioned earlier there are extra capacitors (or at least the footprint for capacitors) to enable the variation of input capacitance and the switching capacitors. Future revisions can eliminate any excess capacitors and reduce the size of the QPRSCC.

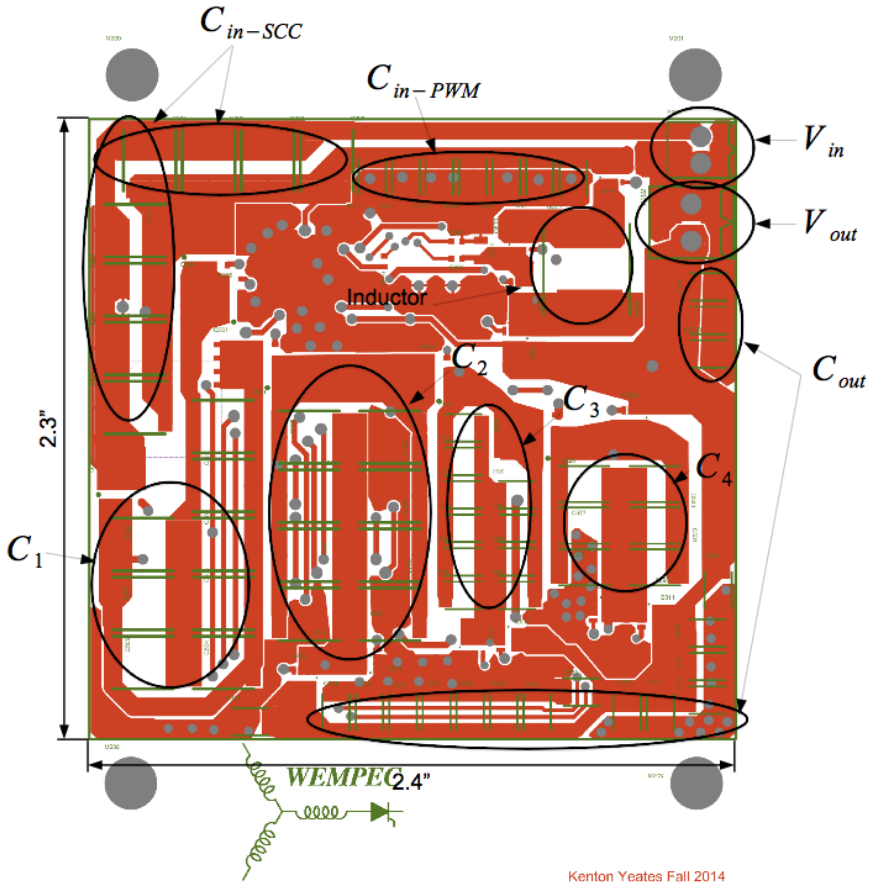


Fig. 5.4. Top Layer of the PCB with the power components and board dimensions annotated.

The bottom layer, depicted in Fig. 5.5, has the gate drive, gate drive power, LT8705, and the microcontroller for the SCC. The largest components on the backside are the DCP021212DP which provides unregulated isolated 12V for the gate drive of the floating MOSFETs in the MMSCC. Although large, they were chosen as they greatly simplified the design thus saving time.

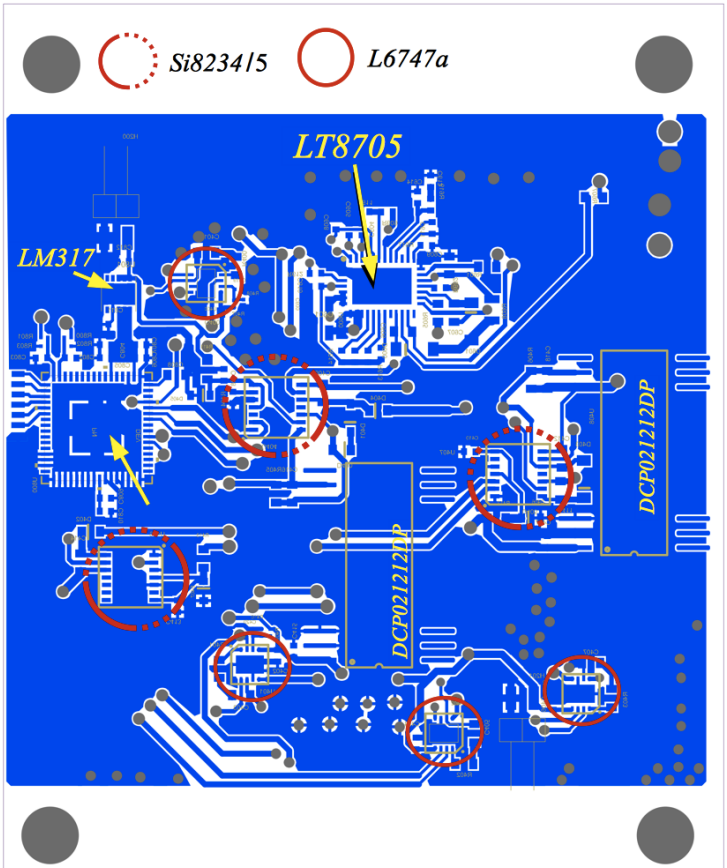
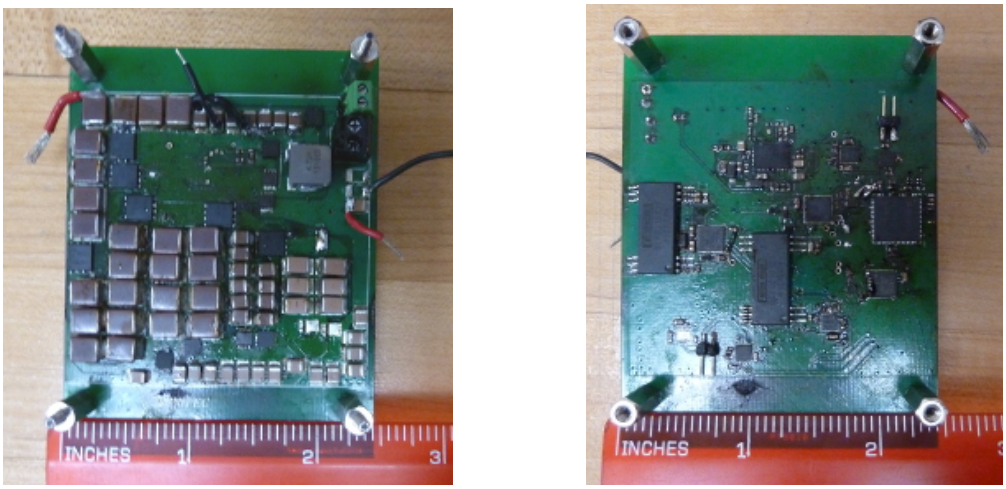


Fig. 5.5. The bottom layer of the 120W QPRSCC Prototype PCB with the gate drive and control chips annotated

The completed QPRSCC 120W prototype PCB board is shown in Fig. 5.6. The board is shown fully populated and with a ruler showing the achieved “half-brick” size.



(a) (b)

Fig. 5.6. The QPRSCC 120W Prototype (a) top layer and (b) bottom layer

5.3 Steady State Operation of the SCC

To verify that the MMSCC was operating as intended it is first operated independently of the H-Bridge in both 2:1 and 3:1 modes. The MMSCC was operated at varying steady-state loads with measurements of the input current, input voltage, output current, output voltage used to calculate the MMSCC load-line and output resistance (section 5.3.1). The experimental output resistance is compared to the calculated steady-state output impedances made in section 3.2. In section 5.3.2, the efficiency of the MMSCC is calculated for 2:1 and 3:1 operation. Gate drive circuity loss is discussed in section 5.3.3. A significant percentage of these losses are due to the design and implementation of the gate drive, rather than from the gate drivers and driving the MOSFETs.

5.3.1 Load Line and Estimated Output Resistance of the MMSCC

In order to test only the MMSCC, the H-Bridge components were not placed on the PCB. A short was placed where the H-Bridge's input capacitors would be placed grounding the input capacitors of the MMSCC. Hence, the MMSCC input voltage is the same as the voltage applied to the board, i.e. the QPRSCC input voltage. While in this configuration, the MMSCC was tested at several steady state loads from 0A to 9A in 2:1 and 3:1 operation using a 150W electronic DC load.

Measuring the output voltage at the different loads provided a load line of the MMSCC. The load-line of an unregulated SCC should be linear, fitting a linear line to the data provides an estimate of the output impedance. This estimated output impedance consists of the switching losses and conduction losses of the MMSCC. As discussed earlier, the theoretical output impedance represents conduction

losses with a slow switching limit (SSL) and a fast switching limit (FSL) asymptote. As the switching frequency increases, the output impedance decreases until reaching the FSL. Any additional increases to the switching frequency, no longer decrease the conduction losses and only incurs further switching losses.

The MMSCC was first operated in 3:1 mode at the following switching frequencies: 250kHz, 213kHz, 165kHz, 110kHz, and 53kHz. It was therefor tested at switching frequencies above, below, and near the selected switching frequency of 180kHz (section 3.2). Frequencies higher than 180kHz will produce similar conduction losses but will incur higher switching losses. Frequencies lower than 180kHz will have lower switching losses but the conduction losses will begin to increase as the MMSCC moves from the FSL and capacitive charging losses become significant.

The experimental load lines for the MMSCC in 3:1 operation at various switching frequencies are plotted in Fig. 5.7. The slope of the linear fit line overlays the data, giving an estimate of the output impedance. The estimated output impedances, which include turn on and turn off switching losses, were 84.5mΩ, 72.6mΩ, 62.4mΩ, 60.9mΩ, and 88.1mΩ for the switching frequencies 250kHz, 213kHz, 165kHz, 110kHz, and 53kHz respectively. This confirms the expected pattern of decreasing output impedance to a minimum value and then increasing upon entering the SSL as the switching frequency decreases. The experimental results revealed two derivations from the expected results. First, the most efficient operating switching frequency was expected to be around 180kHz. However, the ideal switching frequency was around 110kHz since it provided the smallest estimated output impedance. Secondly, all of the estimated output impedances were much larger than the expected 23mΩ. Similar results are obtained from the experimental results for the 2:1 MMSCC steady-state tests.

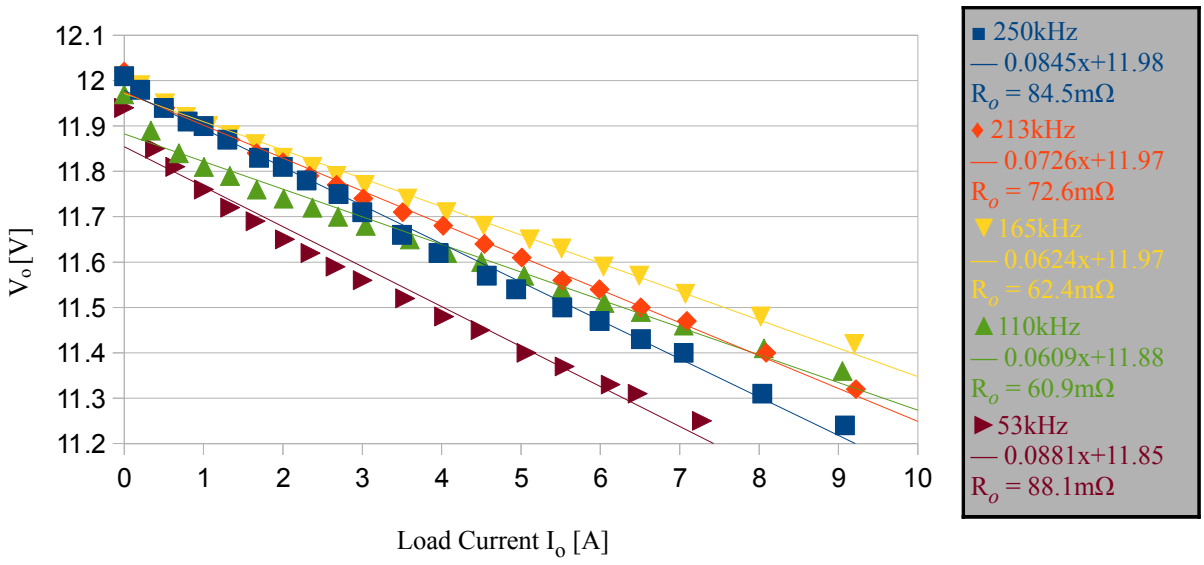


Fig. 5.7. Experimental load-line of the 3:1 MMSCC at selected switching frequencies with the linear fit lines overlaid to estimate the output impedance

The experimental load lines for the MMSCC in 2:1 operation at various switching frequencies are plotted in Fig. 5.8. The MMSCC in 2:1 operation was tested at 213kHz, 141kHz, and 110kHz.The slope of the linear fit line is overlaid the data gives an estimate of the output impedance. The estimated output impedances, which include turn on and turn off switching losses, are 109mΩ, 104mΩ, and 92.4mΩ for the switching frequencies 213kHz, 141kHz, and 110kHz respectively. As in 3:1 mode, the MMSCC estimated output impedances indicate that 110kHz is an optimal switching frequency while the magnitudes of the impedances are larger than expected. For 2:1 operation, the MMSCC expected output impedance was a nominal 38mΩ.

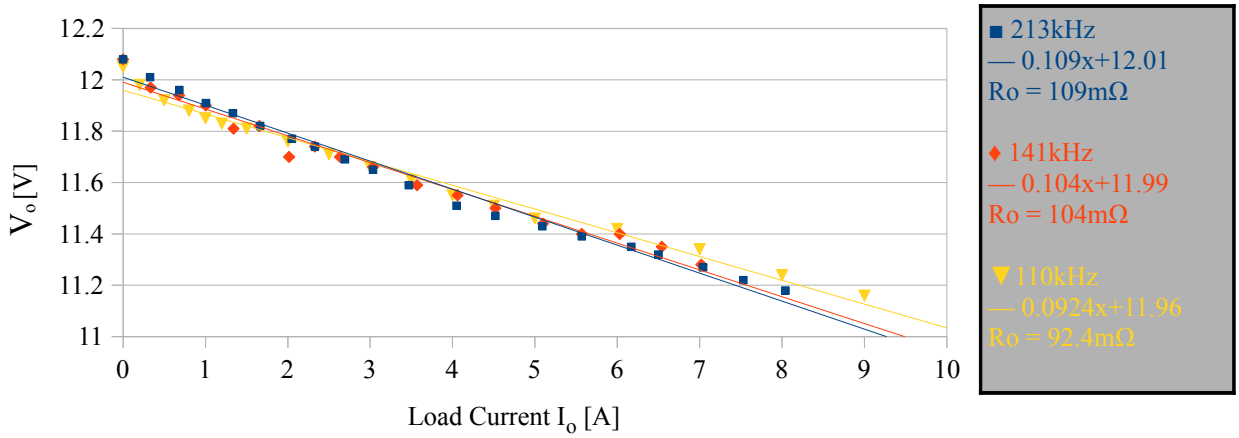


Fig. 5.8. Experimental load-line of the 2:1 MMSCC at selected switching frequencies with the linear fit lines overlaid to estimate the output impedance

When considering the difference between the measured output impedance and the modeled output

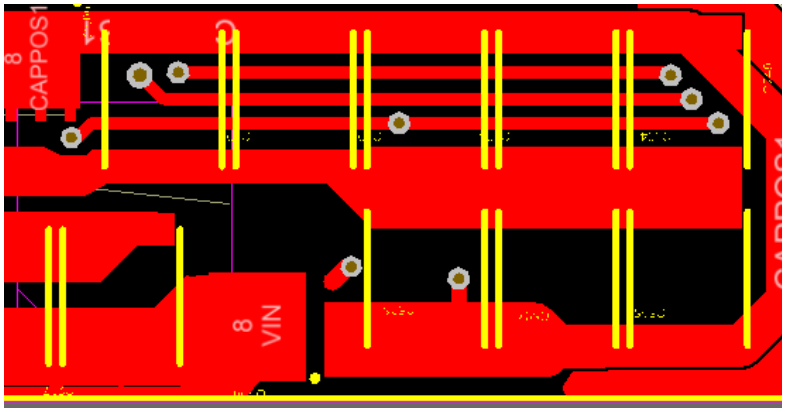
impedance, there are two possible explanations. The first is that the ceramic capacitors did not lose as much capacitance as expected due to the DC-Bias voltage. The second is that the PCB trace resistances are much more significant and have increased the fast switching limit output impedance asymptote. Either case would cause the most efficient switching frequency to occur lower than 180kHz. Regardless of the cause, this indicates the MMSCC can be either operated at a slower switching frequency or the switching capacitance can be reduced. Because the capacitor footprints have already increased the PCB board area, it was decided to reduce the switching frequency.

While the capacitance of the switching-capacitors cannot be easily measured while the MMSCC is operating, (the necessary test equipment was not available), the parasitic resistance of the PCB can be estimated. The PCB board is laid with 1oz copper and despite attempts to keep trace resistance low with wide traces, the PCB trace resistance was evidently significant in comparison to the MOSFET on resistances of ~4mΩ@25° C. Estimates of PCB trace inductance and resistances can be made using equations (5.1) and (5.2), where w, l, and t are the width, length, and thickness of the traces respectively. Using these equations each switching capacitor can be represented by a network of PCB trace resistances, PCB trace inductances, and the capacitors.

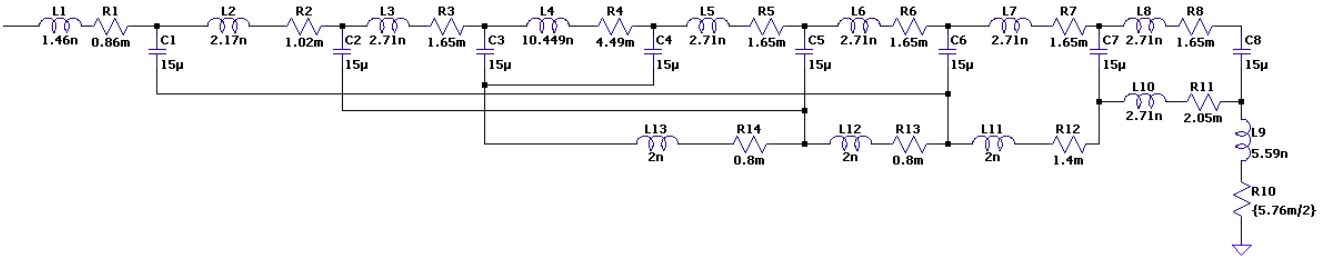
$$L_{PCB}=0.2\,l\left(\ln\left(\frac{2\,l}{(w+t)}\right)+\frac{0.223(w+t)}{l}+0.5\right) \tag{5.1}$$

$$R_{PCB}=\frac{\sigma_{CU}\,l}{w\,t}\quad\text{where}\quad\sigma_{CU}=1.7\left[\frac{\mu\,\Omega}{cm}\right] \tag{5.2}$$

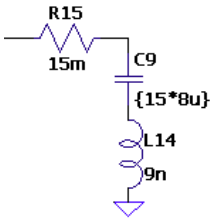
For example, the first switching-capacitor (PCB layout shown in Fig. 5.9(a)), yields a network of resistances and inductances displayed in Fig. 5.9(b). An equivalent single resistance, single capacitance, and single inductor, Fig. 5.9(c), is then made by inspection of the frequency response of the impedances using LTSpice. A comparison of the complex impedance network representing the PCB and equivalent single RLC impedance is shown in Fig. 5.9(d).



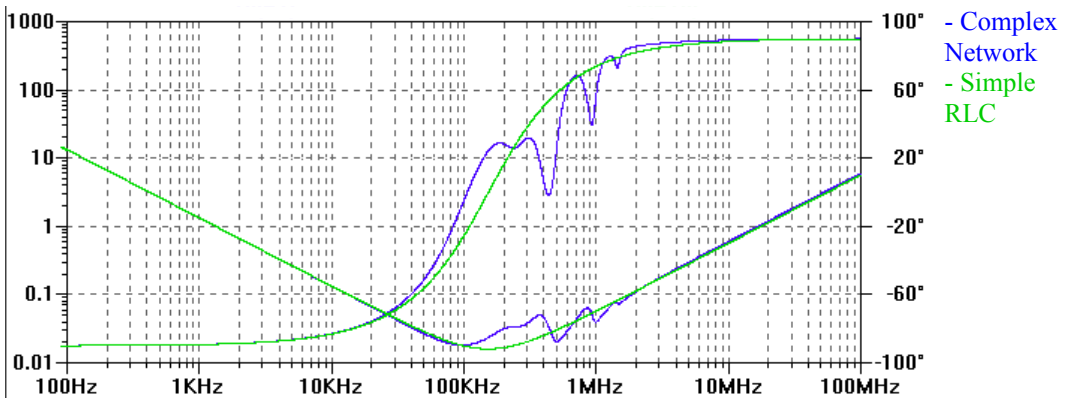
(a) PCB Layout for the first switching capacitor C_1 in the MMSCC.



(b)Spice Model of PCB parasitics



(c)



(d)

Fig. 5.9. The PCB (a) layout creates a (b) complex network of impedances for each switching capacitor. These can be modeled by a (c) simple RLC impedance that matches the (d) frequency response.

The resulting simplified RLC, shown in Fig. 5.9(c), illustrates that the PCB trace resistance contributes a significant resistance of 15mΩ to the first switching capacitor. By modeling the switching capacitor as a simple RLC impedance the PCB trace resistance can be combined with the capacitor's ESR. The same process is applied to the switching capacitors C_2 and C_3 calculating that the respective PCB trace resistance adds 5.5mΩ and 6mΩ to the respective capacitor's effective ESR. With the added resistance, the capacitors ESR will increase the FSL output impedance asymptote, calculated by (5.3).

$$R_{FSL} = 2\,R_{ds-on}\left(\frac{5+2n}{n^2}\right) + 4\frac{1}{n^2}\sum_i R_{ESR,i} \tag{5.3}$$

Besides the PCB trace resistance within the switching-capacitors, there is a significant source of parasitic resistance from the long PCB trace from the MMSCC to the board output. The MMSCC connects to the output from two or three different sources on the board depending on 2:1 or 3:1 operation. The path of the power from the MMSCC to the board output is illustrated in Fig. 5.10. The parasitic resistances associated with these paths can be added to the MOSFETs which are located at these circled sources in the figure.

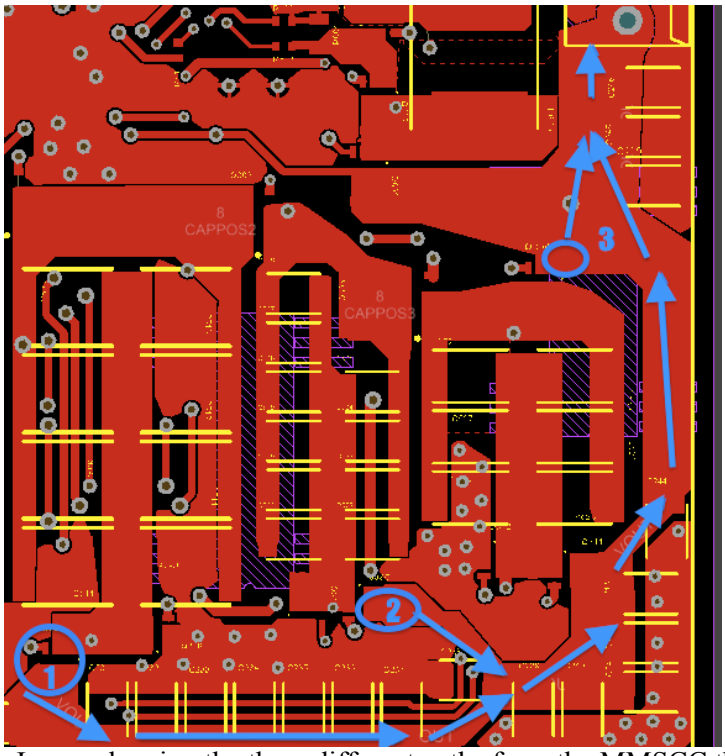


Fig. 5.10. Image showing the three different paths from the MMSCC the output voltage. Two of which see significant parasitic resistance

The source 1 (circled) labeled in Fig. 5.10 adds 18mΩ to one MOSFET that is operated in 2:1, 3:1, and 4:1 operation. The source 3 adds 3mΩ to one MOSFET that is operated in 2:1, 3:1, and 4:1. Source 2 adds 12mΩ to a MOSFET that only operates in 3:1 and 4:1. The The FSL asymptotic output impedance can be recalculated for 2:1 and 3:1 modes of operation, with the PCB parasitic resistances added to the capacitor ESR for selected MOSFETs from (5.4).

$$R_{FSL} = 2\frac{1}{n^2}\sum_j R_{ds-on,j} + 4\frac{1}{n^2}\sum_i R_{ESR,i} \tag{5.4}$$

$$R_{FSL}^{2:1}=\frac{1}{2}\left(9\left(6\text{m}\Omega\right)+\left(18\text{m}\Omega\right)+\left(3\text{m}\Omega\right)\right)+\left(18\text{m}\Omega+8.5\text{m}\Omega\right)=64\text{m}\Omega \tag{5.5}$$

$$R_{FSL}^{3:1}=2\left(6\text{m}\Omega\right)\left(\frac{11}{9}\right)+\frac{4}{9}\left(18\text{m}\Omega+8.5\text{m}\Omega+9\text{m}\Omega\right)=34\text{m}\Omega \tag{5.6}$$

Plotting the output impedance asymptotic limits, SSL and FSL, the increased FSL asymptote has pushed the optimal switching frequency near the 100kHz range as shown in Fig. 5.11. The experimental output impedances are still larger than the theoretical output impedances due to the inclusion of switching losses and parasitic resistances not modeled.

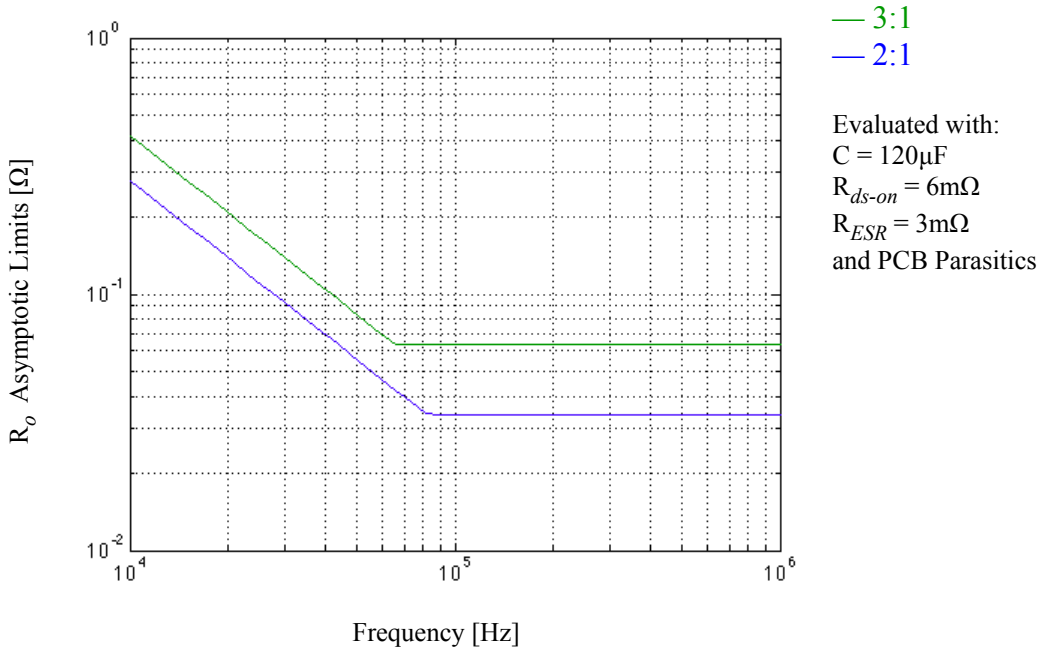


Fig. 5.11. Increases in the FSL asymptotic limit shifts the optimal switching frequency to approximately 100kHz due to PCB trace resistances

5.3.2 Efficiency of the MMSCC

Efficiency measurements were taken of the MMSCC in 2:1 and 3:1 operation at various switching frequencies. The power path efficiency in 3:1 operation and 2:1 operation is shown in Fig. 5.12 and Fig. 5.13 respectively. These do not include the gate drive and control circuitry losses. The measured efficiencies again indicate that 110kHz is the optimal switching frequency. At light loads, where switching losses tend to dominate over conduction losses, the switching frequencies above the 110kHz have decreased efficiencies. At higher loads (above 5A) when conductions losses begin to dominate, the switching frequencies at and above 110kHz display similar efficiencies. This indicates that switching frequencies at and above 110kHz are in the FSL have the highest efficiency in the power

path. The lowest switching frequency, 50kHz, has the worst efficiency as expected as it operates the MMSCC in the SSL, leading to an increased output impedance and higher conduction losses.

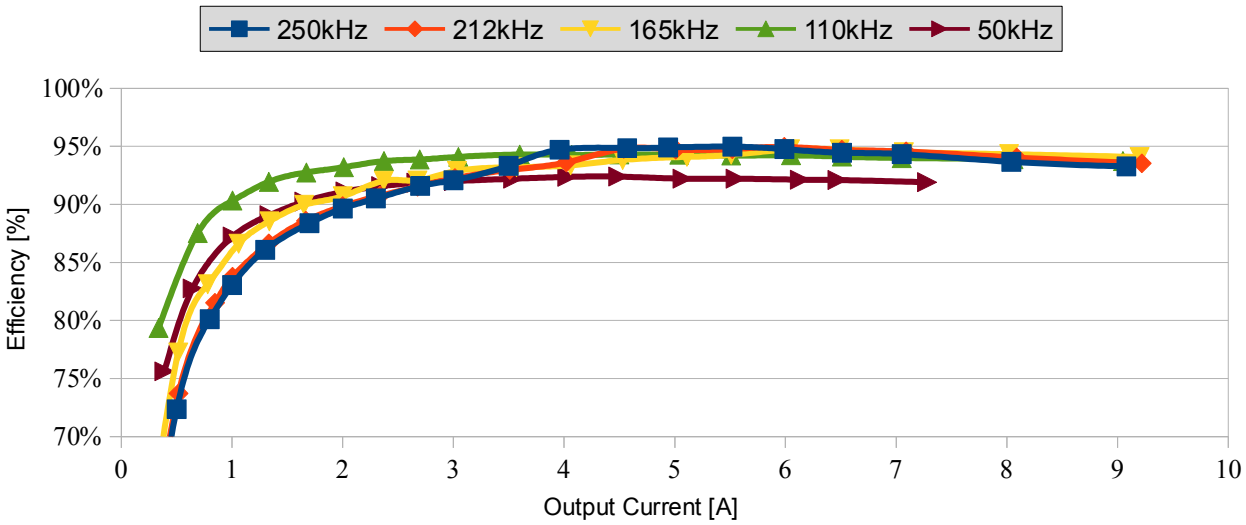


Fig. 5.12. Efficiency of the power path of the 3:1 MMSCC (not including losses in gate drive circuitry)

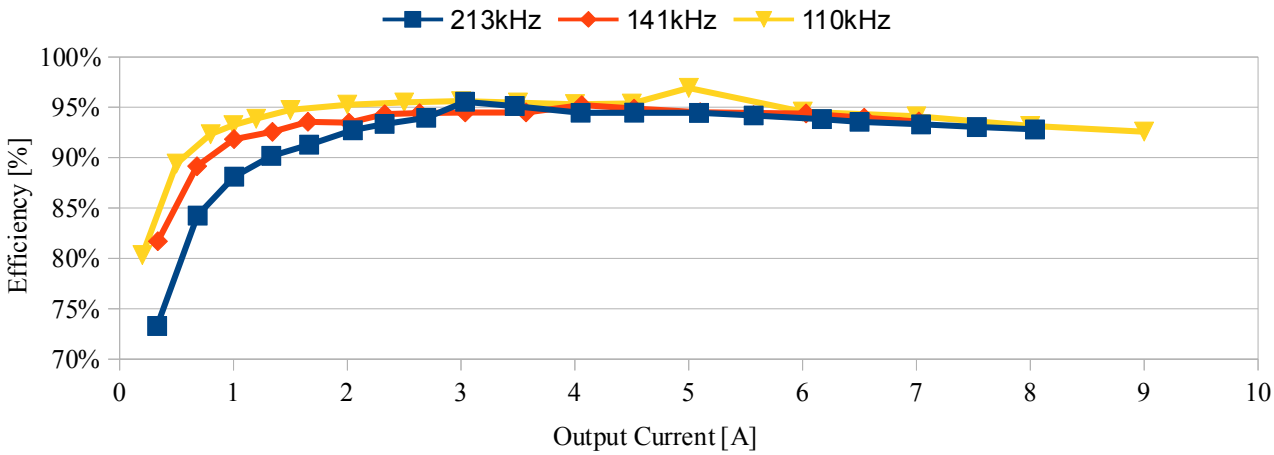


Fig. 5.13. Efficiency of the power path of the 2:1 MMSCC (not including losses in gate drive circuitry)

For light loads the MMSCC has relatively low efficiencies regardless of switching frequency, implies significant switching losses. Investigation revealed “shoot-through” is occurring in the switches below the capacitors circled in Fig. 5.14. A thermal image of the QPRSCC, Fig. 5.15, operating at no load, shows a MOSFET with significant temperature rise while the other MOSFETs are at or near room temperature. These MOSFETs are driven synchronously by the gate driver L6747A. The L6747A accepts a PWM signal that drives each MOSFET and should prevent shoot-through. Future work should investigate different gate drivers to eliminate shoot-through. Since the gate signals could not be adjusted, the MOSFETs were replaced with those with a higher gate charge increasing switching losses

but reducing shoot-through.

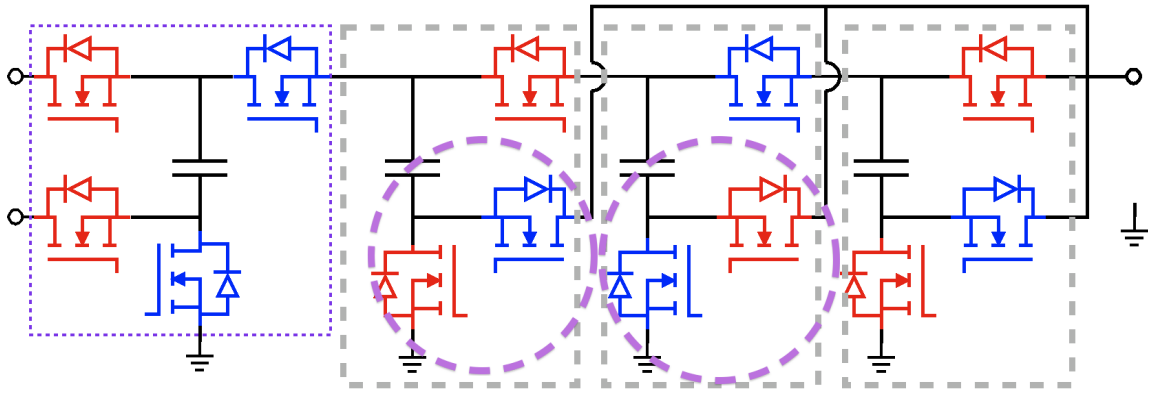


Fig. 5.14. Shoot-through at the MOSFETs (circled in purple), decreases the efficiency of the MMSCC

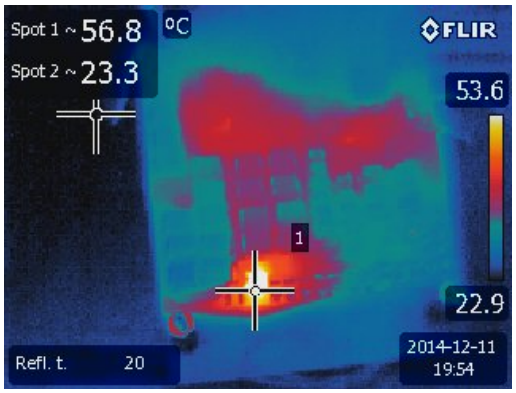


Fig. 5.15. At no load (for the MMSCC) shoot-through causes significant power loss in the MOSFET connected to the output

The experimental efficiencies shown in Fig. 5.13 indicate the MMSCC should be operated at or near 110kHz for highest efficiencies and increased light load efficiency. Thus a switching frequency of 110kHz was used for all additional tests. Inclusion of gate drive and control circuitry power consumption the efficiency of the MMSCC drops a few percentage points as seen in Fig. 5.16. In 2:1 mode the MMSCC achieves approximately 93% efficiency at loads above 3A. In 3:1 operation the MMSCC reaches 92% at loads of 5A or higher. By replacing the MOSFETs, the shoot-through effect is greatly reduced in 3:1 mode leading to a increase of 2 percentage points in efficiency as shown by the yellow triangle (▼) in Fig. 5.16.

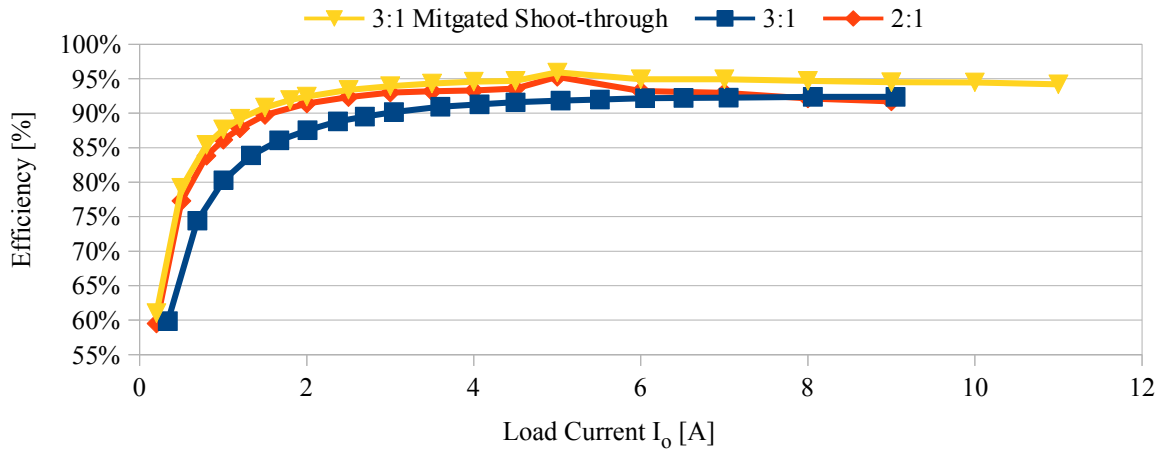


Fig. 5.16. Total efficiency of the MMSCC as a function of load currents at selected conversion ratios and showing the efficiency gain by mitigating the shoot-through issue.

5.3.3 Gate Drive Circuitry Losses

During the steady-state testing of the MMSCC the power for the gate drive circuitry and the microcontroller are supplied from a separate power supply. Depending on the switching frequency and the number of active gate drivers and MOSFETs, the gate drive losses ranged from 2.4W to 3W. A third of the power due is lost due to design inefficiency. This design inefficiency arises from limiting the complexity of the gate drive and reducing design time. The power losses are discussed in subsections A and B. In subsection C a portion of the dissipated power is shown to be through unnecessary losses. The measured gate drive and control losses will be compared to the expected design losses.

A. Unregulated Isolated 12V Power Converter

The first source of lost power is from using the DCP021212DP for the isolated 12V to drive the floating MOSFETs in the MMSCC. As long as there is a significant load on the output of the DCP021212DP the driving voltage will be roughly 12V. Without a load the output voltage can reach 24V. To prevent this and safeguard the MOSFETs and gate drivers, a resistor was placed in parallel to the output to provide a minimum load on the unregulated 12V output as shown in Fig. 5.17. As calculated in (5.7) the loss in the resistor assuming 12V output is 0.282W. There are two DCP021212DP and two of these resistors for a total of 0.564W.

$$P_{loss}=\frac{V^2}{R}=\frac{12^2}{510}=0.282\text{W} \tag{5.7}$$

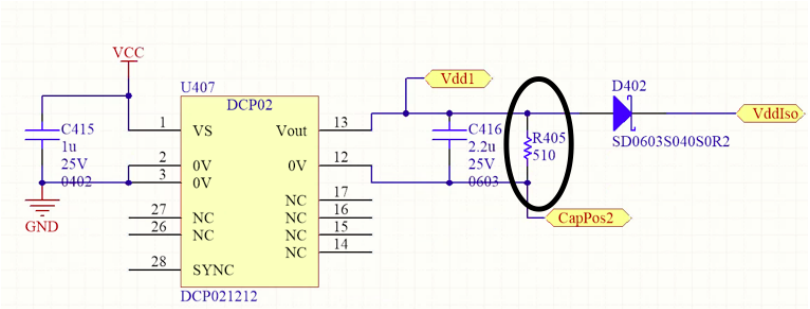


Fig. 5.17. Roughly 0.282W are lost in the resistor (circled) keeping a minimum load on the unregulated 12V

B. Zener Regulated Voltages

Another source of power loss is in the decision to only provide a 12V Vcc despite some of the gate drive ICs having a maximum input voltage of 5V. To save space, the 12V Vcc is regulated to 5.1V by a zener diode as shown in Fig. 5.18. This results in power loss through the zener diode and the resistor. Assuming a nominal breakdown voltage of 5.1V, the power loss in the resistor is calculated to be 0.136W in (5.6). The current through the diode will be, at steady state, roughly the current through resistor minus the current drawn by the Si234/5 gate driver. According to their datasheets both the Si8234 and the Si8235 will draw 2.5mA while operating. Thus the power loss in the zener diode is calculated as in (5.5) and found to be 0.088W. There are three of these zener regulated voltages for a total of 0.672W.

$$P_{res} = \frac{V^2}{R} = \frac{(12-5.1)^2}{350} = 0.136\text{W} \tag{5.8}$$

$$P_{zener} = I\,V = \left(\frac{(12-5.1)}{350} - 2.5\text{mA}\right) 5.1\text{V} = 0.088\text{W} \tag{5.9}$$

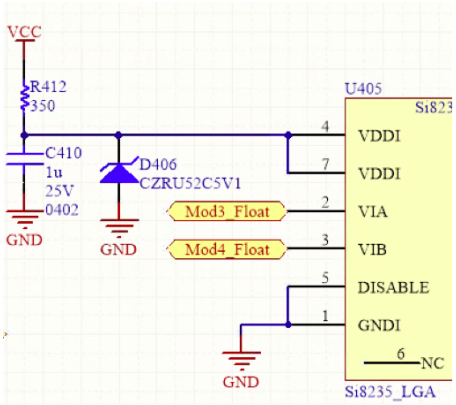


Fig. 5.18. The 5V needed for the Si8234/5 Gate Drivers is supplied by a shunt zener diode and a resistor to limit input current from 12V Vcc.

C. Evaluation of Gate Drive Circuitry Loss and Comparison to Calculated Losses

It can be verified through thermal imaging that when operating with no load, the hottest components on the back of the PCB are the resistors and zener diodes mentioned in the previous subsections. The thermal image shown in Fig. 5.19 shows that the zener diodes and resistors, circled in orange, are the hottest parts on the prototype. The large warm devices (circled in purple) are the DCP021212DP, and the unmarked warm devices are gate drivers.

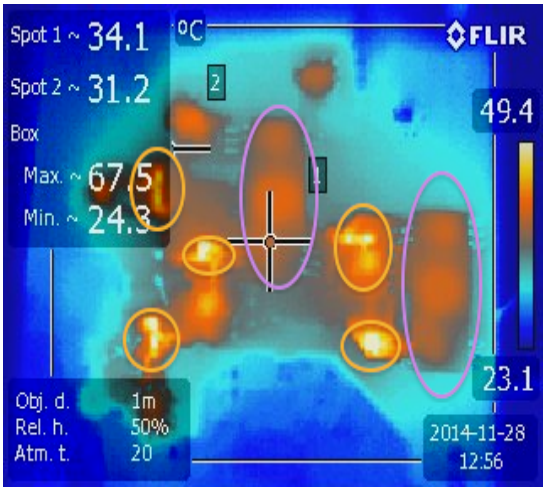


Fig. 5.19. Thermal image depicting the gate drive losses due to design inefficiencies

Future revisions of this prototype should eliminate the resistors and zener diodes through better design of the gate-drive circuitry. This will eliminate unnecessary power loss and heat generation. The other gate drive and control losses come from driving the MOSFETs, the gate driver chips, the microcontroller, and the LDO that provides the 3.3V for the microcontroller. It is assumed that only the charging of the MOSFET gate will vary significantly with switching frequency, the rest are considered constant.

Summing the previously discussed losses gives a total of 1.236W. At light loads this is a significant amount of wasted power, and should be reduced in a future design. The experimental efficiencies presented in this paper have had the 1.236W subtracted from the total input power. Thus the presented experimental efficiencies only account for losses in the power path (i.e. conduction and switching losses) and losses in the gate drive ICs and microcontroller.

5.4 Regulated Voltage and Efficiency of the H-Bridge

The H-Bridge was tested at steady-state at various input voltages with up to 4A of DC load. This is

done by disconnecting the output of the MMSCC from the rest of the circuit to prevent power from flowing back into the MMSCC through the body diodes of the MOSFETs. The input voltage is then directly applied across the input capacitors of the H-Bridge.

The H-Bridge was tested with input voltages of 4V, 6V, 12V, 16V, and 24V, forcing the H-Bridge to operate in boost, buck-boost, and buck modes. For each input voltage the H-Bridge was tested up to the maximum current it would see while operating within the QPRSCC. As shown in Fig. 5.20, the H-Bridge provides a regulated output voltage of approximately 12.1V for each input voltage and load currents. The total efficiencies of the H-Bridge are shown in Fig. 5.21, this includes gate drive and control circuitry for operation of the H-Bridge. At light loads the H-Bridge is relatively inefficient with efficiencies below 90%. Future versions of the prototype can allow the H-Bridge to operate with Linear Technologies "Burst Mode" which provides higher efficiencies at light loads. Overall, the H-Bridge achieves acceptable efficiencies of 92%, 94% and 95% for 6V, 12V and 24V, and 16V input voltages respectively. At 4V the H-Bridge peaks around 90% efficiency which is acceptable for boost mode and providing 1 to 3 conversion ratio.

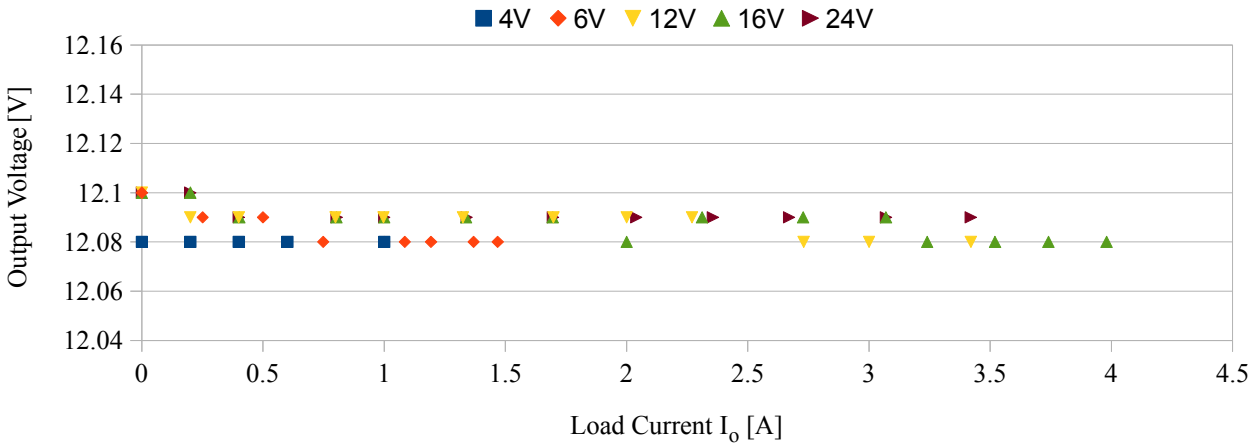


Fig. 5.20. H-Bridge achieves a regulated voltage of ~12.1V for input voltages of 4V, 6V, 12V, 16V, and 24V.

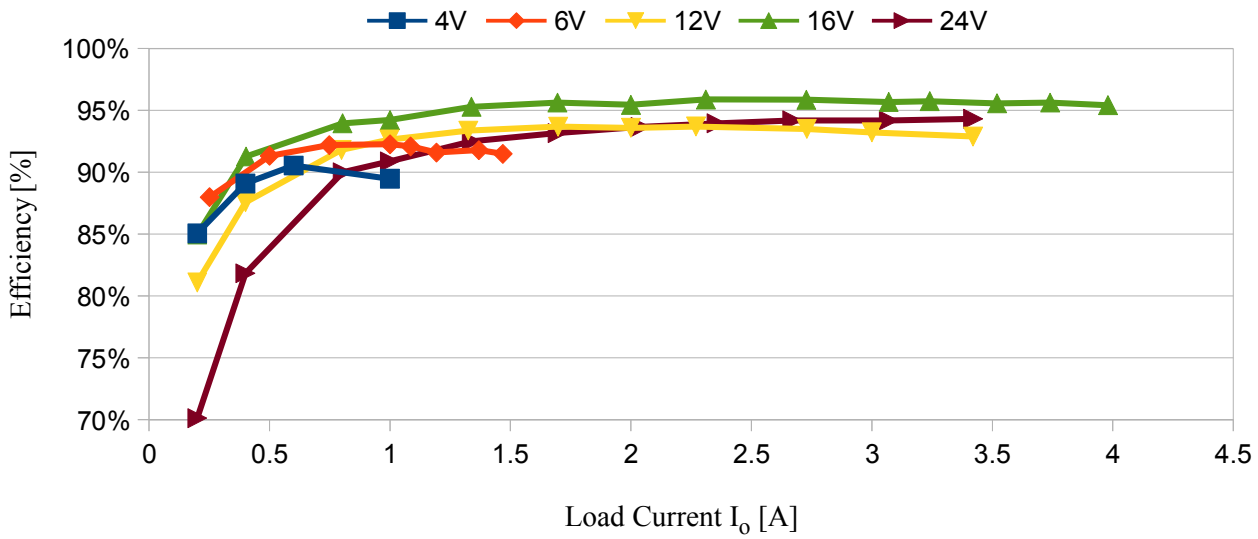


Fig. 5.21. H-Bridge efficiencies for input voltages of 4V, 6V, 12V, 16V, and 24V.

5.5 Experimental Results of the QPRSCC

The 120W prototype QPRSCC was tested at steady state to examine voltage regulation at several voltages and to measure overall efficiency. Next in section 5.5.2 the experimental results of load transient tests are shown, demonstrating the QPRSCC dynamic response and ability to handle load transients from 50% to 100%. Finally experiments showing the ability to provide line regulation of the QPRSCC will be shown in section 5.5.3.

5.5.1 Steady State Operation and Efficiency

To show that the QPRSCC provided the desired regulation, it was tested at various input voltages for output currents of 0A to 10A (full load). The QPRSCC load line plotted in Fig. 5.22 shows the QPRSCC achieves a regulated voltage of approximately 12.1V. This is the desired regulated voltage based off the design of the H-Bridge circuit utilizing the LT8705. The output voltage is seen to vary with the input voltage of the H-bridge and the MMSCC conversion ratio. The variation seen is only ±50mV and is acceptable. A drop in output voltage is seen with increasing output current. In this case, the variation is at most ±20mV and again acceptable. The variations in output voltage could be a result of the output voltage being sensed very close to the H-bridge's output. The distance from the H-Bridge to the board output may be large enough to cause a 20mV difference in measured output when the QPRSCC is at full load (10A). Overall the issue is of little interest as it is not problematic.

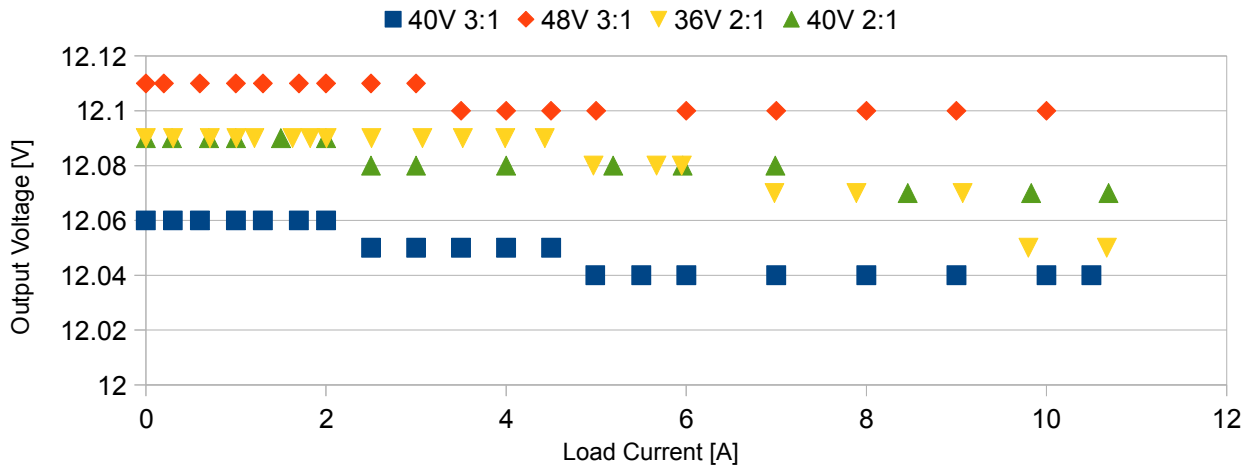


Fig. 5.22. QPRSCC load-line for selected input voltages and MMSCC conversion ratios

The efficiency of the QPRSCC was measured for input voltages of 36V, 40V, and 48V with the MMSCC operating in 2:1 and 3:1 modes. The efficiency is calculated by looking at the input current, input voltage, output current, and output voltage at the board power connections. The gate drive current and voltage is also measured, but the power losses due to design inefficiencies (as discussed 5.3.3) have been subtracted from the gate drive power.

The QPRSCC achieves efficiencies of 93% or 94% for 50% to 100% load as shown in Fig. 5.23. At light load the QPRSCC remains fairly efficient until loads below 1A. Thermal imaging has shown that for a 48V input voltage and MMSCC operating in 3:1 mode, there may be shoot-through loses due to unusual heating of a pair of synchronous MOSFETs. However, the results indicate that the QPRSCC does provide steady-state regulation with a partial power H-Bridge with achievable efficiencies of 94%.

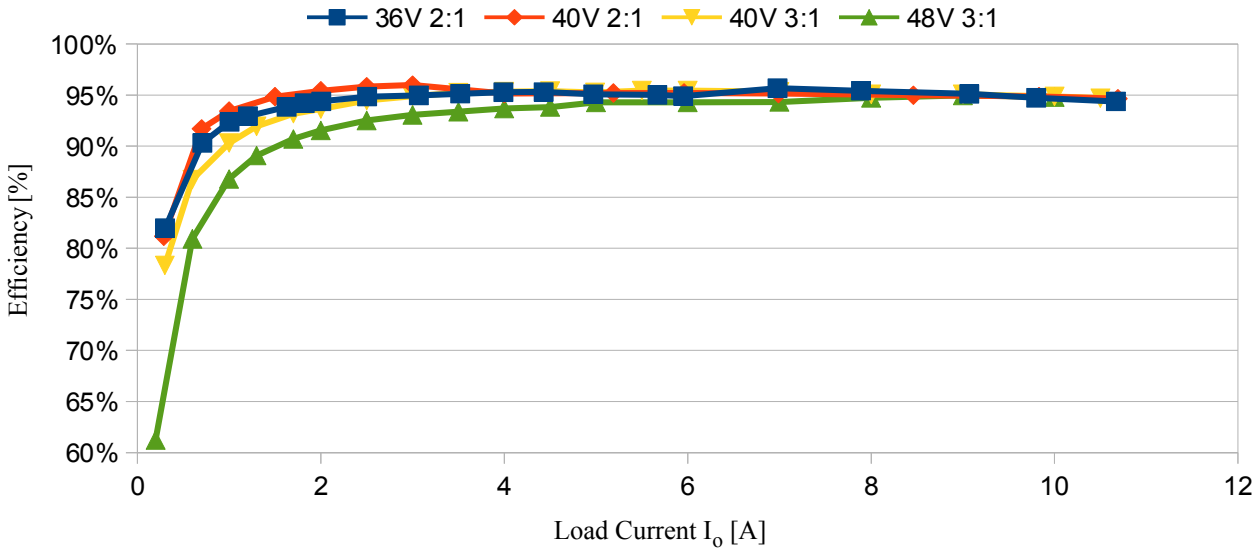


Fig. 5.23. QPRSCC efficiencies for input voltages of 36V, 40V, and 48V showing high efficiencies attained at 50% to 100% load

5.5.2 Load Transients

To test the QPRSCC's dynamic response a resistor bank was connected with an emergency stop switch (the red button in Fig. 5.24) to the output of the QPRSCC. The emergency stop switch is used as it is able to connect/disconnect the resistor bank within 10µs, providing an adequate approximation of a load step. The constructed resistive load is shown in Fig. 5.24. The resistor bank has a measured resistance of 2.18Ω providing a load step of 5.58A. The 150W DC electronic load is attached in parallel with the resistive bank to provide a constant DC load. By setting the DC electronic load to 5A and using the emergency stop switch to connect/disconnect the resistor bank load transients of 50% to 100% and 100% to 50% were applied to the QPRSCC.

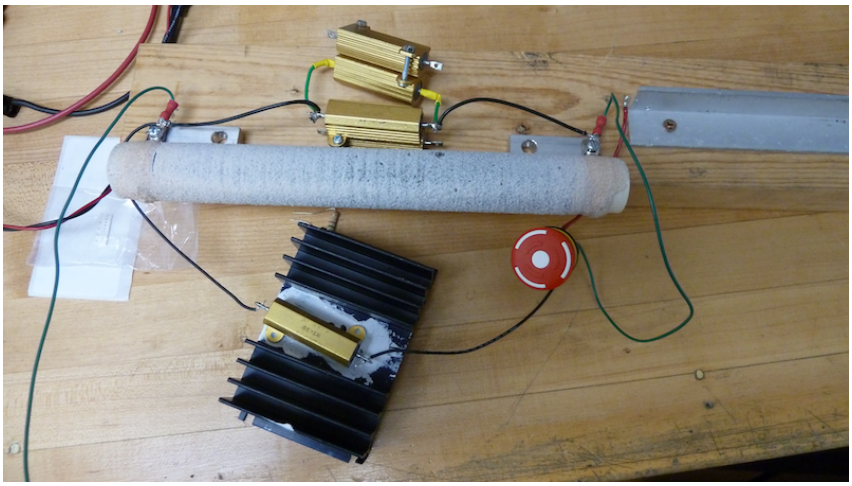
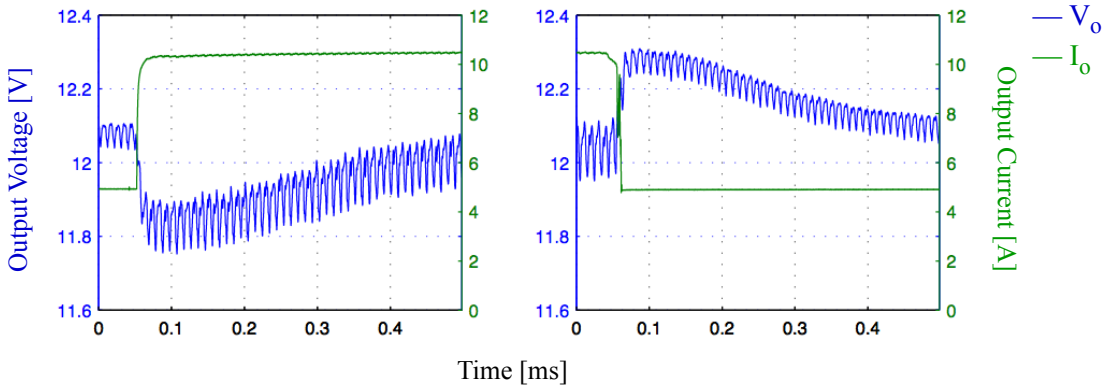
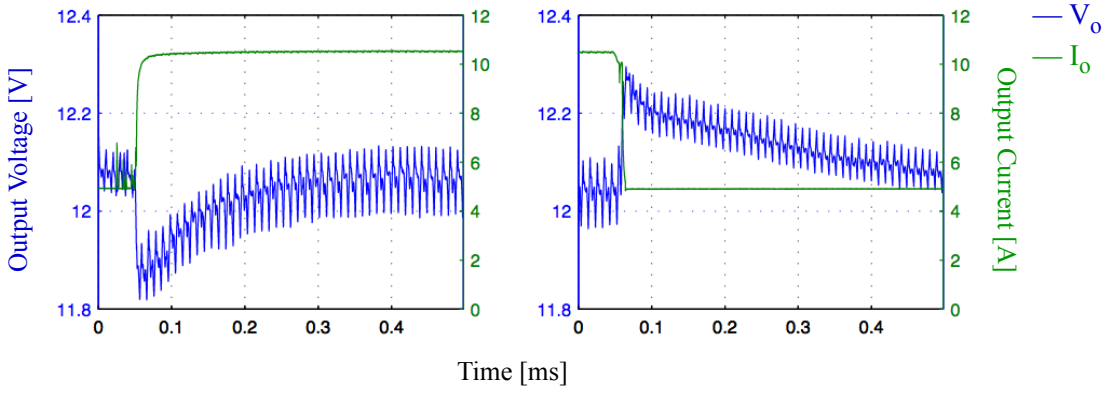


Fig. 5.24. Resistor bank used for load transients
connected/disconnected by emergency stop switch (button)

The QPRSCC load is stepped from 50% to 100% and vice versa with input voltages of 36V and 48V. The QPRSCC exhibits a well behaved output voltage transient response, that stays within 3% of the regulated voltage as shown in Fig. 5.25. Although not completely evident from Fig. 5.25, the QPRSCC does reach steady state. The QPRSCC regulates to a different steady state voltage depending on the load as shown in Fig. 5.22. The difference in steady-state output voltage is 40mV (for 50% to 100% load and vice versa) and explains the difference in the initial and final steady state voltage during the load step.



(a) 36V QPRSCC (MMSCC 2:1)



(b) 48V QPRSCC (MMSCC 3:1)

Fig. 5.25. QPRSCC output voltage response to a load step of 50% to 100% and vice versa

5.5.3 Line Variation

The QPRSCC also provides a regulated output voltage in the event of line transients. A SCC by itself has limited ability to provide regulation, especially for changes in the input voltage. The ability of the QPRSCC to deal with line transients was experimentally proven by applying a ramp transient to the input voltage.

Due to a limitation of equipment, the input voltage of the QPRSCC could only be adjusted by hand. A line disturbance is simulated by altering the voltage from the power supply to the QPRSCC, limiting the (achievable) slew rate. The input voltage is ramped from 40V to 52V over a span of ~50ms and also decreased from 52V to 40V in 100ms with the MMSCC having a conversion ratio of 3:1. The only observable effect on the output voltage is the change of steady state values due to the H-Bridge shifting from boost to buck-boost to buck mode of operation in Fig. 5.26. As shown in Fig. 5.22, the regulated output voltage depends on the H-Bridge mode of operation with 12.06V for boost mode and 12.1V for

buck-boost and buck mode. At 40V, the output voltage sits at 12.06V, then with the line ramp to 52V the output voltage rises in a well behaved fashion to 12.1V in Fig. 5.26. A reverse response is seen as the input voltage decreases from 52V to 40V.

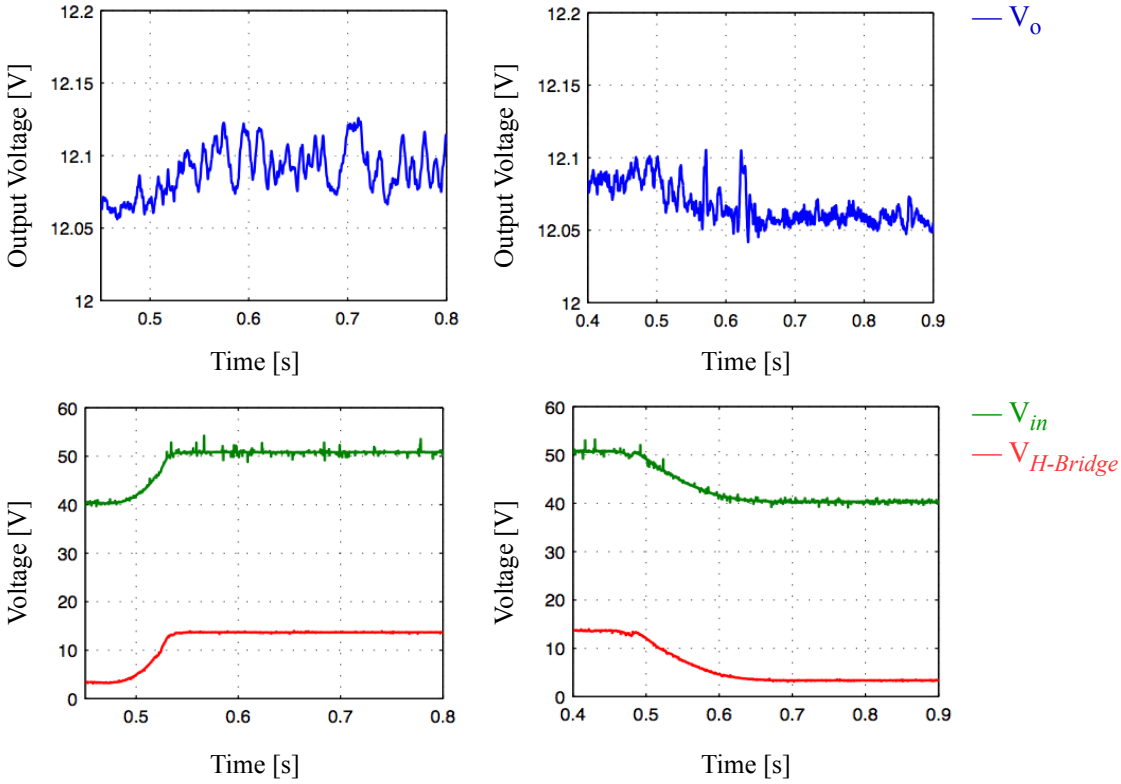


Fig. 5.26. QPRSCC provides a regulated output voltage for input voltage ramps

Chapter 6 Conclusions and Future Work

A regulation strategy for a DC-DC switched-capacitor converter utilizing a regulating DC-DC H-Bridge converter in quasi-parallel configuration has been proposed. Its design has been analyzed and a 120W experimental prototype was built and tested. The prototype was built within a “half-brick” size, however, other commercial converters of this size can produce four times more power. Our tests of the prototype indicate that more power can be realized through the MMSCC converter but the limiting factor in the prototype's design was the H-Bridge.

The quasi-parallel regulated switched-capacitor converter (QPRSCC) as designed achieved load regulation. However, due to time and testing limitations line regulation within 40V to 52V was confirmed. The proposed multilevel modular switched-capacitor converter while able to operate in 2:1, 3:1, and 4:1 modes, has been experimentally shown to function in the QPRSCC in 2:1 and 3:1 modes of operation. The QPRSCC achieved efficiencies above 90% and reaches a peak of 94%, demonstrating the promise of higher efficiencies.

The QPRSCC was shown to have excellent load transient properties, as one would expect for a quasi-parallel configuration. The low output impedance and fast dynamical response of the MMSCC allowed the QPRSCC to respond quickly to changes in the load. As desired, the MMSCC handled the majority of the transient load, keeping the current through the H-Bridge at a low and approximate steady-state value. This protects the inductor from large current transients that could lead to magnetic saturation and loss of regulation.

The prototype demonstrates that a control strategy designed for the regulating converter can provide regulation and excellent transient response for the QPRSCC without added complexity. This allows the QPRSCC to be controlled by commercially available Power IC regulators such as the LT8705, validating the analysis done in Chapter 4, illustrating that the quasi-parallel configuration simplifies the control transfer functions.

The 120W prototype confirms that this approach is a viable method for regulating a SCC while also benefitting from the high efficiencies and high conversion ratios of a SCC. The regulating converter does utilize magnetics but the converter is partial power and can operate at higher frequencies allowing for smaller magnetics when compared to cascaded approaches. Although the QPRSCC is designed to operate at input voltages of 72V and operate with the MMSCC in 4:1 mode this has not been

experimentally proven viable. Time limitations and issues with sensing the input voltage prevented this from being tested.

An additional design change was operating with a switching frequency of 110kHz for the MMSCC instead of the calculated 180kHz. This was caused by the PCB trace resistances increasing the fast switching limit output impedance. This lead to a lower optimal switching frequency of 110kHz. Future revisions of the QPRSCC can utilize less capacitance and further decrease its size. In completed tests the maximum power provided from the MMSCC was restricted to 120W. Future modifications should be able to achieve higher power ratings with the same, if not smaller, board sizes.

The other aspect that requires improvement is the efficiency of the QPRSCC at light loads. This can be improved by increasing the MMSCC light load efficiency, a major cause of the poor efficiency. The unexpected shoot-through issues seen on some of the MOSFETs, was hard to resolve since the gate drivers for these synchronous MOSFETs were driven by a single PWM signal. By providing independent gate drivers in a single package (e.g. Si8235) there would be more control of the MMSCC MOSFETs. Another source of significant loss at light loads were the switching losses of the MMSCC. Here, improvements can be made by decreasing the switching frequency for light loads, thereby decreasing the switching losses. While this increases the equivalent output impedance, the decrease in switching losses will more than compensate for the minor increase in conduction losses due to the higher output impedance at light loads.

An additional source of power loss, is the design of the gate drive circuitry. As detailed in Chapter 5, over 1W of power is lost just enabling and providing adequate voltage levels for the gate drive circuitry. A better design of the gate drive and control circuitry would eliminate these power losses.

Other possible paths for improvements are to consider the use of different SCC. While the MMSCC was chosen for its ability to easily change its conversion ratio, and the low number of floating MOSFETs, other SCC can be designed for multiple conversion ratios. For example the Ladder SCC can be augmented to provide 2:1, 3:1, and 4:1 modes, by tapping different nodes of its topology. Changes in its conversion ratio may not be as problematic, as the switching-capacitors do not need to be discharged or charged when altering the conversion ratio. One drawback (the reason it was not initially chosen) is the number of floating MOSFETs which requires more complex gate drive circuitry. However, the Ladder SCC, with isolated gate drivers, may be well suited for bootstrapped powered gate drive.

The 120W prototype QPRSCC demonstrated the high efficiency and high conversion ratio benefits of

the SCC but the cost of a partial power regulating converter containing magnetics. The regulating converter (the H-Bridge) had low input and output voltages and a lower power rating compared to the MMSCC allowing for higher switching frequencies and smaller passive components in the H-Bridge. The overall efficiency of the QPRSCC is higher than the cascaded approaches as well. Finally, the quasi-parallel configuration does not require special control strategies and can be implemented with commercially available IC power regulators.

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Appendix A Matrices for DSSA of MMSCC

Matrices E,F,and G for Dynamic Analysis of the Isolated MMSCC in 4:1 and 2:1 mode

4:1 Mode

Phase 1

$$\mathbf{E}_1^{4:1}=\begin{bmatrix} -(2r_s+r_e) & 0 & 0 & 0 & 0 \\ 0 & 0 & (3r_s+2r_e) & 0 & r_{co} \\ 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & -(2r_s+r_e) & r_{co} \\ 0 & 0 & R_{th} & -R_{th} & -(R_{th}+r_{co}) \end{bmatrix} \quad \mathbf{F}_1^{4:1}=\begin{bmatrix} -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & -1 \end{bmatrix}$$

$$\mathbf{G}_1^{4:1}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & R_{th} \end{bmatrix}$$

Phase 2

$$\mathbf{E}_2^{4:1}=\begin{bmatrix} 0 & (3r_s+2r_e) & 0 & 0 & r_{co} \\ 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & (3r_s+2r_e) & r_{co} \\ 0 & 0 & 1 & 1 & 0 \\ 0 & R_{th} & 0 & R_{th} & -(R_{th}+r_{co}) \end{bmatrix} \quad \mathbf{F}_2^{4:1}=\begin{bmatrix} -1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 \end{bmatrix} \quad \mathbf{G}_1^{4:1}=\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & R_{th} \end{bmatrix}$$

Deadtime

$$\mathbf{E}_{dt}^{4:1}=(R_{th}+R_{co}) \qquad \mathbf{F}_{dt}^{4:1}=1 \qquad \mathbf{G}_{dt}^{4:1}=\begin{bmatrix} 0 & -1 & \dfrac{R_{co}}{R_{th}+R_{co}} \end{bmatrix}$$

2:1 Mode

Phase 1

$$\mathbf{E}_1^{2:1}=\begin{bmatrix} -(2r_s+r_e) & 0 & 0 \\ 0 & -(4r_s+r_e) & r_{co} \\ 0 & -R_{th} & -(R_{th}+r_{co}) \end{bmatrix} \quad \mathbf{F}_1^{2:1}=\begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 1 \\ 0 & 0 & -1 \end{bmatrix} \quad \mathbf{G}_1^{2:1}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & R_{th} \end{bmatrix}$$

Phase 2

$$\mathbf{E}_2^{3:1}=\begin{bmatrix} 0 & (3r_s+2r_e) & r_{co} \\ 1 & 1 & 0 \\ 0 & R_{th} & -(R_{th}+r_{co}) \end{bmatrix} \quad \mathbf{F}_2^{3:1}=\begin{bmatrix} -1 & 1 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & -1 \end{bmatrix} \quad \mathbf{G}_2^{3:1}=\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & R_{th} \end{bmatrix}$$

Deadtime

$$\mathbf{E}_{dt}^{2:1}=(R_{th}+R_{co}) \qquad \mathbf{F}_{dt}^{2:1}=1 \qquad \mathbf{G}_{dt}^{2:1}=\begin{bmatrix} 0 & -1 & \dfrac{R_{co}}{R_{th}+R_{co}} \end{bmatrix}$$

P and Q Matrices

4:1 Mode

$$g = 3r_s + 2r_e \quad f = 2r_s + r_e$$

$$r_{tot} = \frac{1}{\left(1 + \frac{r_{co}}{g} + \frac{r_{co}}{f} + \frac{r_{co}}{R_{th}}\right)}$$

$$\mathbf{P^{4:1}} = \begin{bmatrix} \frac{-D_1}{(2r_s + r_e)} & 0 & 0 & 0 & 0 \\ 0 & \frac{r_{tot} r_o}{g} & \frac{-r_{tot} r_o}{g} & \frac{r_{tot} r_o}{f} & r_{tot} \end{bmatrix}$$

$$\mathbf{Q^{4:1}} = \begin{bmatrix} \frac{D_1}{(2r_s + r_e)} & 0 & 0 \\ 0 & \frac{r_{tot} r_o}{R_{th}} & r_{tot} r_{co} \end{bmatrix}$$

3:1 Mode

$$g = 3r_s + 2r_e$$

$$r_{tot} = \frac{1}{\left(1 + \frac{r_{co}}{g} + \frac{r_{co}}{R_{th}}\right)}$$

$$\mathbf{P^{3:1}} = \begin{bmatrix} \frac{-D_1}{(2r_s + r_e)} & 0 & 0 & 0 \\ 0 & \frac{r_{tot} r_o}{g} & \frac{-r_{tot} r_o}{g} & r_{tot} \end{bmatrix}$$

$$\mathbf{Q^{3:1}} = \begin{bmatrix} \frac{D_1}{(2r_s + r_e)} & 0 & 0 \\ 0 & \frac{r_{tot} r_o}{R_{th}} & r_{tot} r_{co} \end{bmatrix}$$

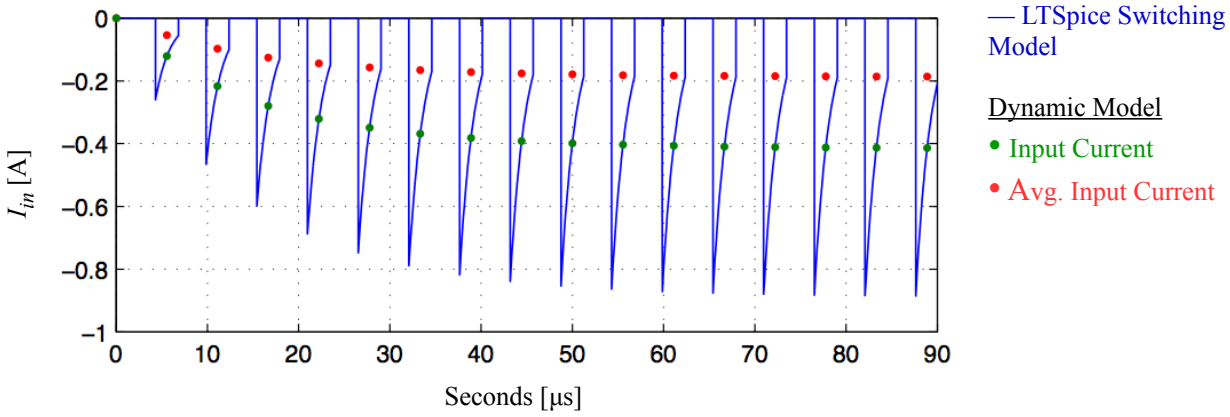
2:1 Mode

$$g = 4r_s + r_e$$

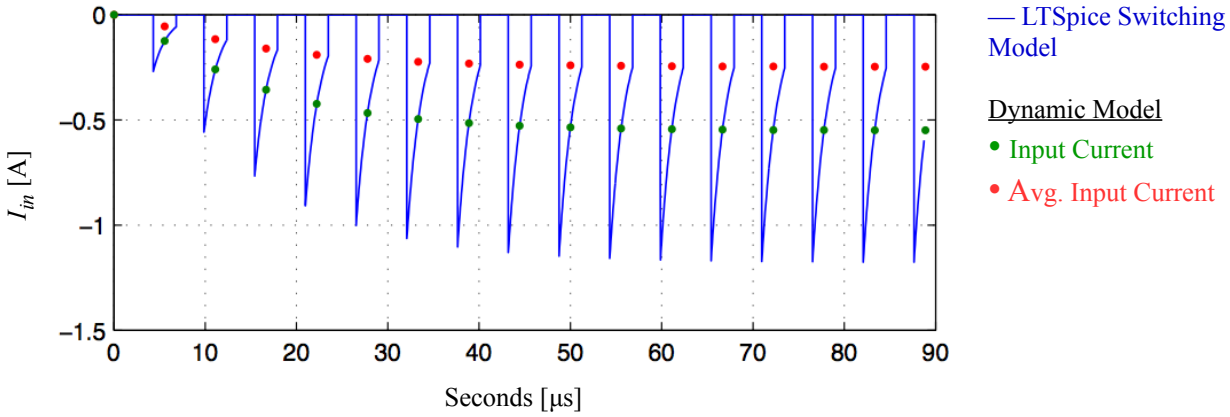
$$r_{tot} = \frac{1}{\left(1 + \frac{r_{co}}{g} + \frac{r_{co}}{R_{th}}\right)}$$

$$\mathbf{P^{2:1}} = \begin{bmatrix} \frac{-D_1}{(2r_s + r_e)} & 0 & 0 \\ 0 & \frac{r_{tot} r_o}{g} & r_{tot} \end{bmatrix} \qquad \mathbf{Q^{2:1}} = \begin{bmatrix} \frac{D_1}{(2r_s + r_e)} & 0 & 0 \\ 0 & \frac{r_{tot} r_o}{R_{th}} & r_{tot} r_{co} \end{bmatrix}$$

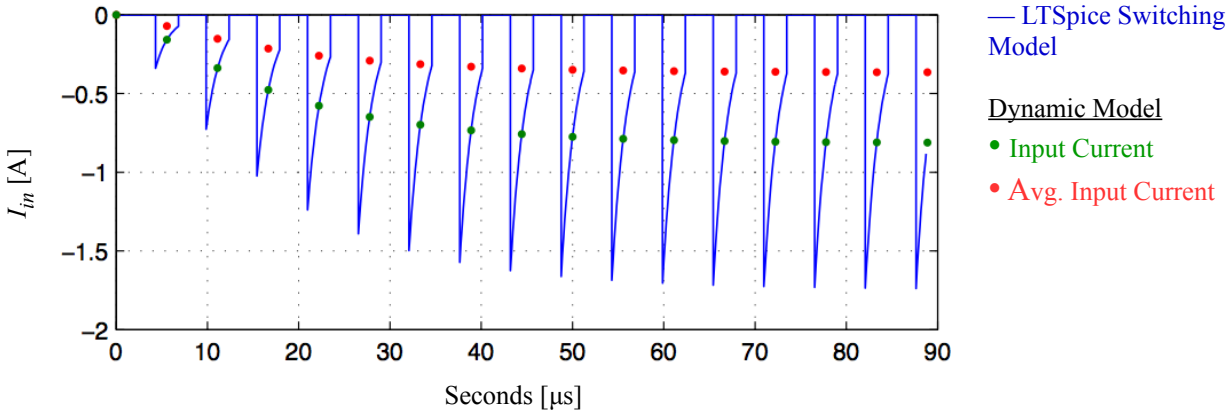
Appendix B Comparison of DSSA Model and LTSpice



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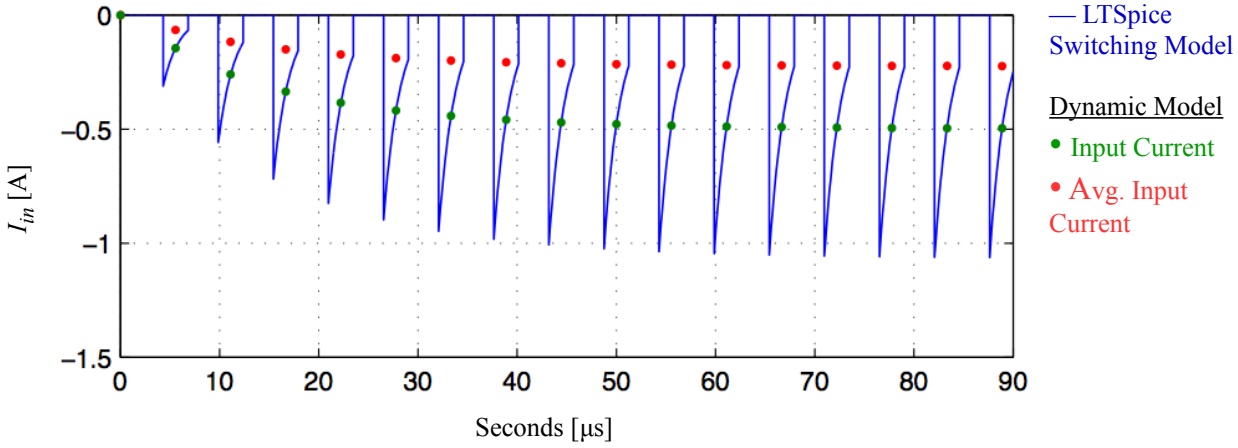


(b) 3:1

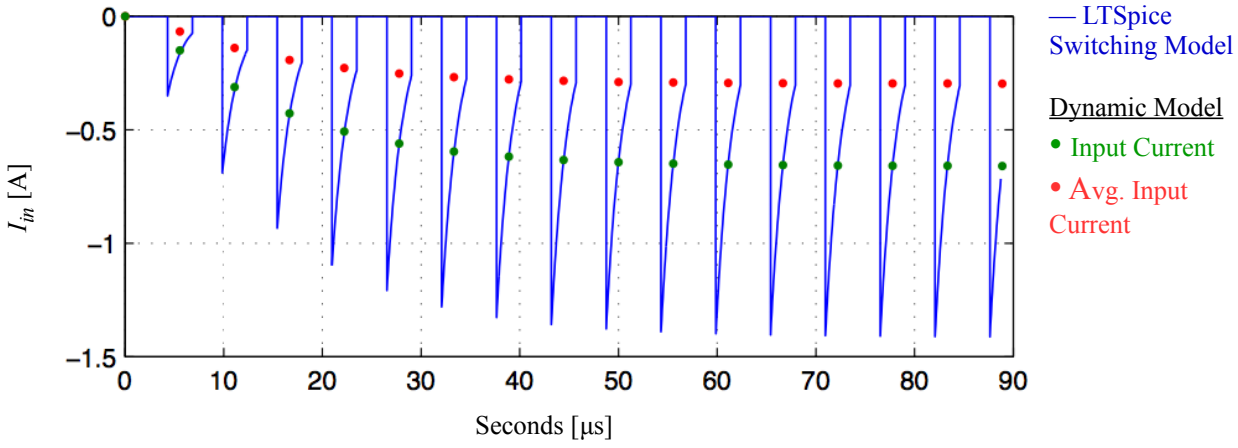


(c) 2:1

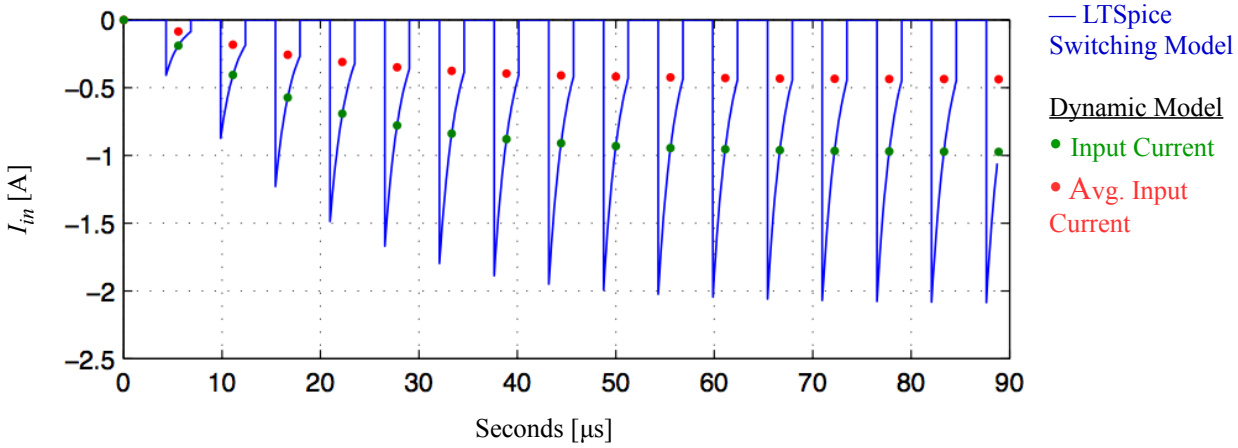
Fig. B.2. Comparison of the input current step response of the DSSA Dynamic Model and the LTSpice simulation of the MMSCC in each operating mode to a step in the v_{th}.



(a) 4:1



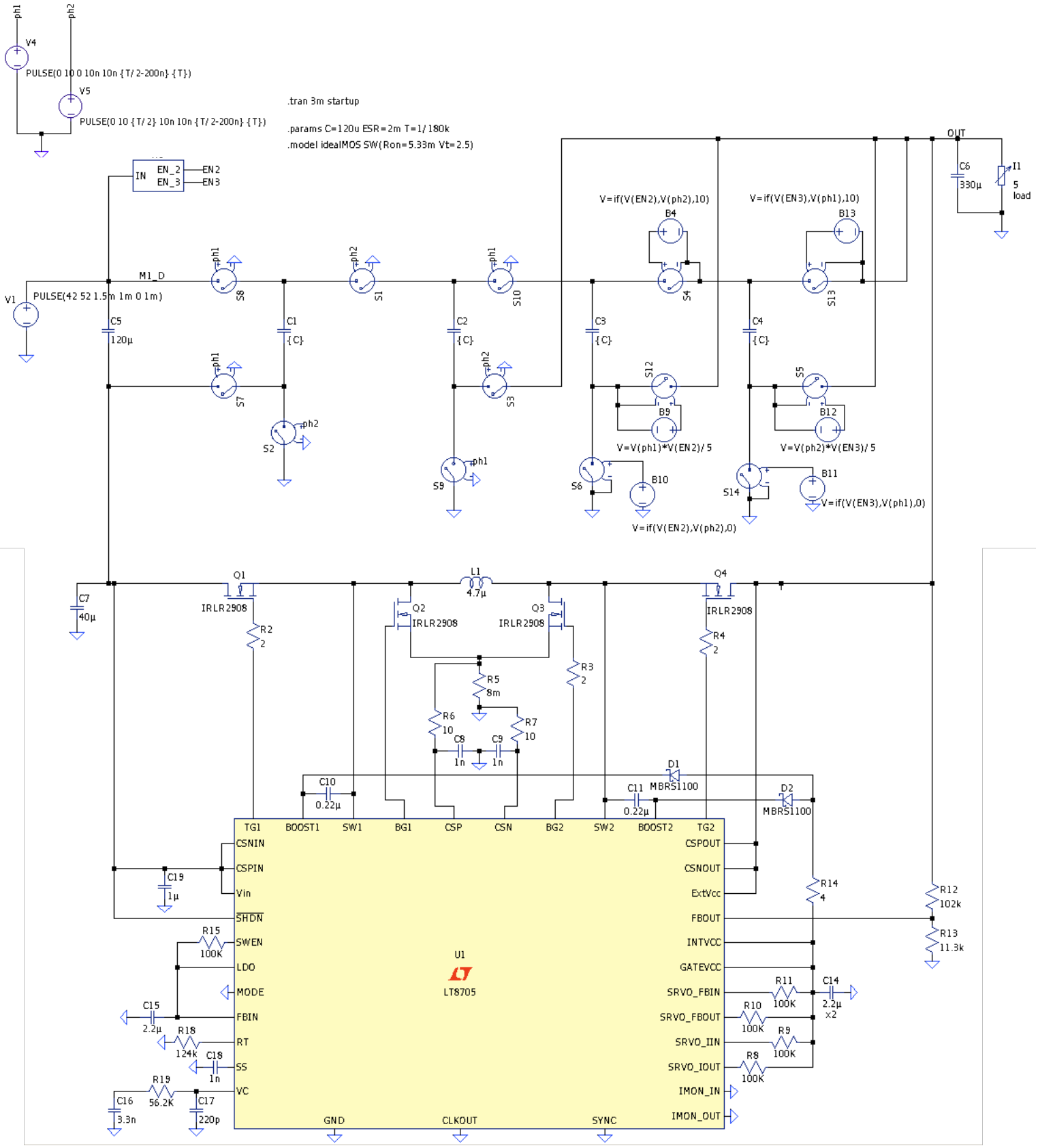
(b) 3:1



(c) 2:1

Fig. B.2. Comparison of the input current step response of the DSSA Dynamic Model and the LTSpice simulation of the MMSCC in each operating mode to a step in the I_{PWM}.

Appendix C LTSpice Circuit for QPRSCC Simulation



Appendix D QPRSCC Prototype Schematics and PCB

Table of Contents

Pg.1 – TOC

Pg.2 – Power Connections & Bulk Capacitance

Pg.3 – Isolated MMSCC

Pg.4 – MMSCC Gate Drive

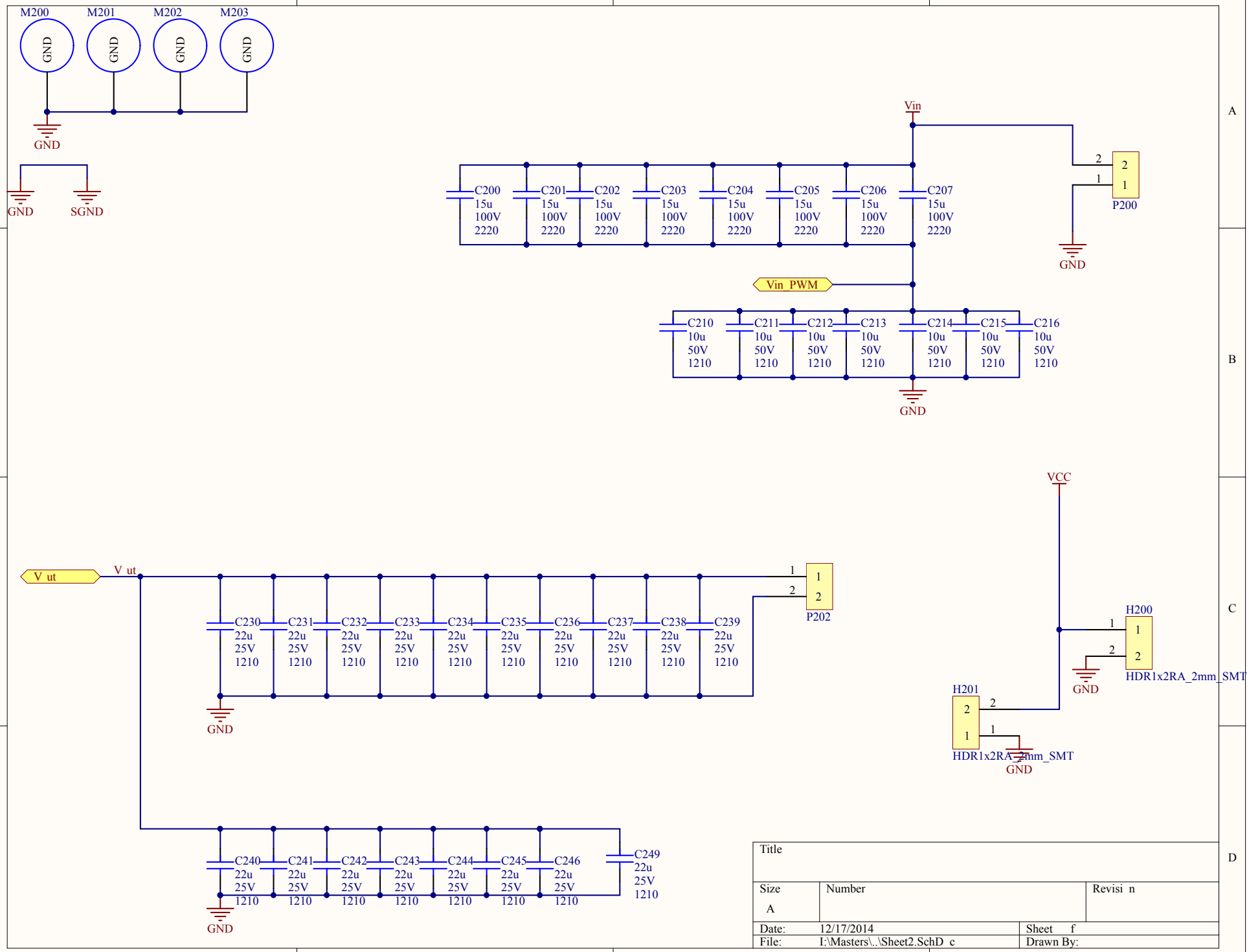
Pg.5 – Switched-Capacitor Capacitance Banks

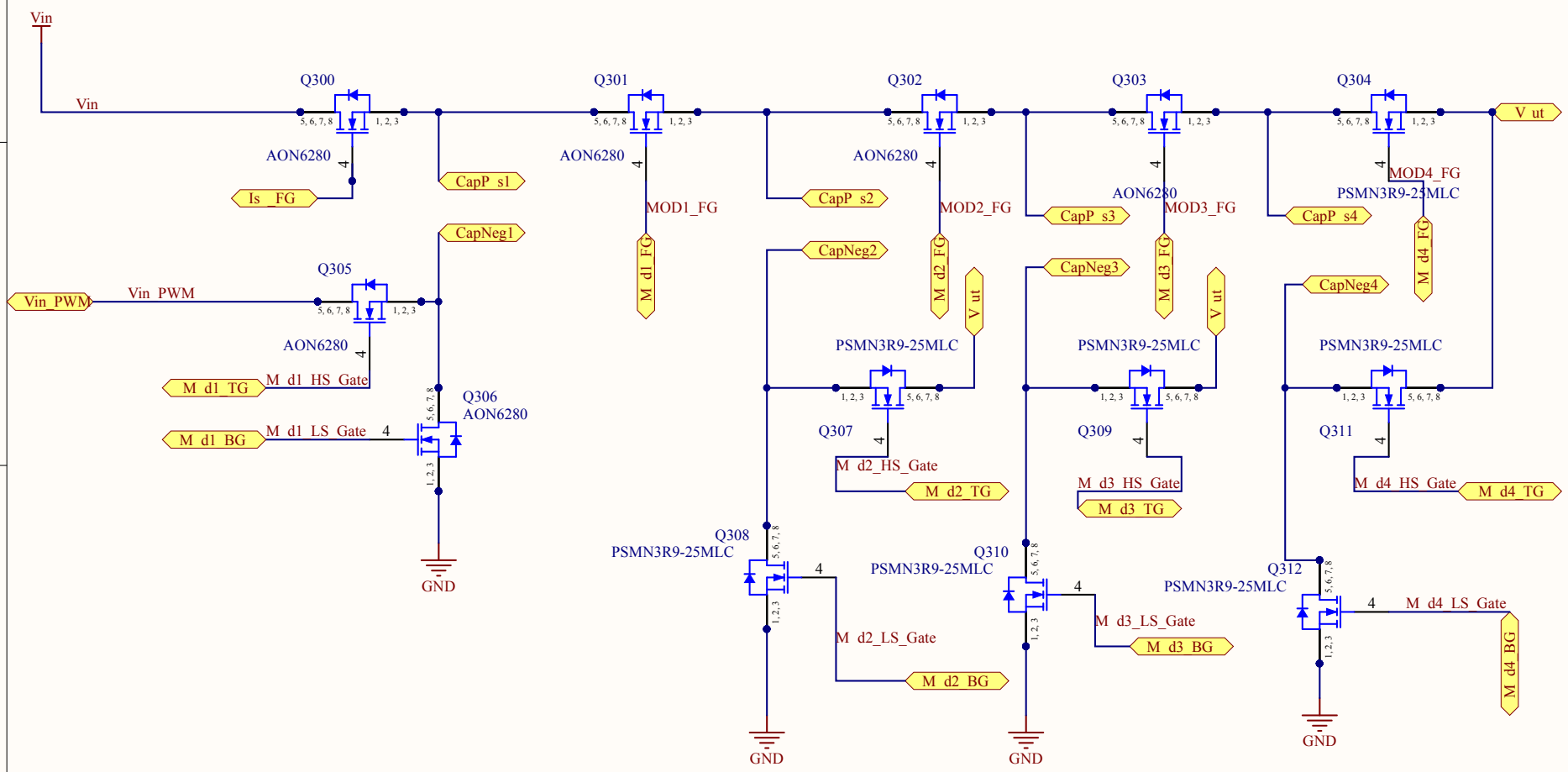
Pg.6 – H-Bridge

Pg.7 – Gate Drive Power

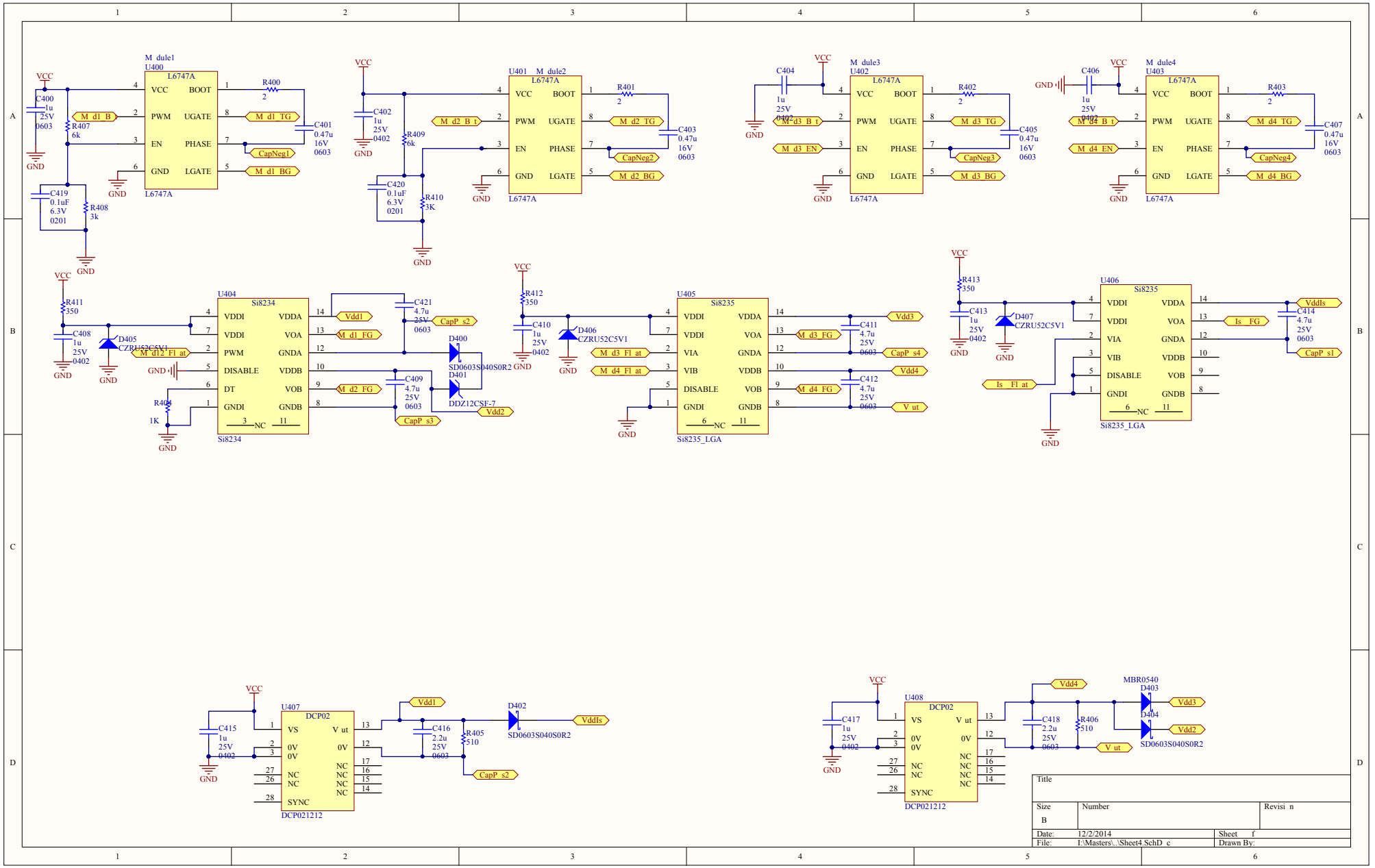
Pg.8 – Microcontroller

Pg.9+ - PCB Layers

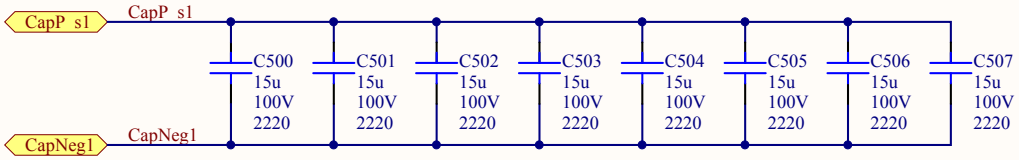

M200
M201
M202
M203
GND
GND
GND
GND
GND
GND
SGND
Vin
C200 15u 100V 2220
C201 15u 100V 2220
C202 15u 100V 2220
C203 15u 100V 2220
C204 15u 100V 2220
C205 15u 100V 2220
C206 15u 100V 2220
C207 15u 100V 2220
2
1
P200
GND
Vin_PWM
C210 10u 50V 1210
C211 10u 50V 1210
C212 10u 50V 1210
C213 10u 50V 1210
C214 10u 50V 1210
C215 10u 50V 1210
C216 10u 50V 1210
GND
VCC
H200
1
2
HDR1x2RA_2mm_SMT
GND
H201
HDR1x2RA_2mm_SMT
GND
V ut
V ut
C230 22u 25V 1210
C231 22u 25V 1210
C232 22u 25V 1210
C233 22u 25V 1210
C234 22u 25V 1210
C235 22u 25V 1210
C236 22u 25V 1210
C237 22u 25V 1210
C238 22u 25V 1210
C239 22u 25V 1210
1
2
P202
GND
C240 22u 25V 1210
C241 22u 25V 1210
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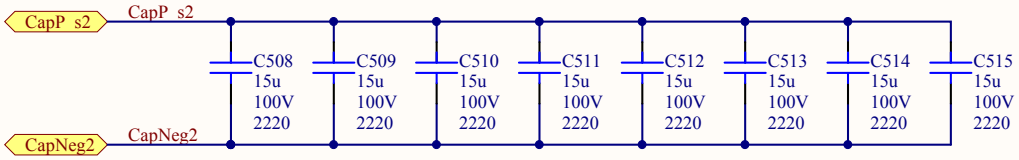
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EN
PHASE
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LGATE
R400
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M_d1_BG
M_d1_B
CapNeg1
C400
1u
25V
0603
R407
6k
C401
0.47u
16V
0603
C419
0.1uF
6.3V
0201
R408
3k
U401 M_dule2
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0402
R409
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C420
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0201
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M_d2_BG
M_d2_B_t
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16V
0603
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C404
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25V
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M_d3_TG
M_d3_BG
M_d3_B_t
M_d3_EN
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0603
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C406
1u
25V
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0603
U404
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VDDI
VDDA
VOA
PWM
GNDA
DISABLE
VDDB
DT
VOB
GNDI
GNDB
NC
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350
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1u
25V
0402
D405
CZRU52C5V1
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4.7u
25V
0603
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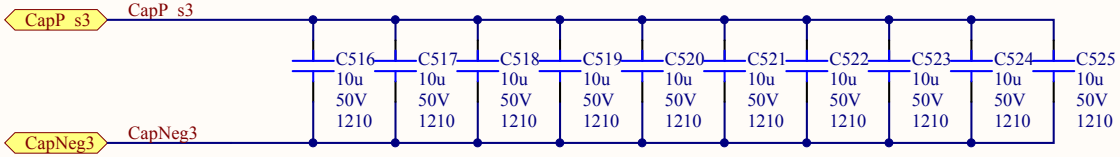
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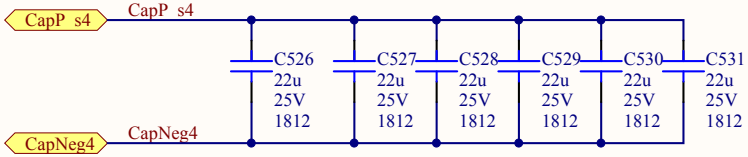
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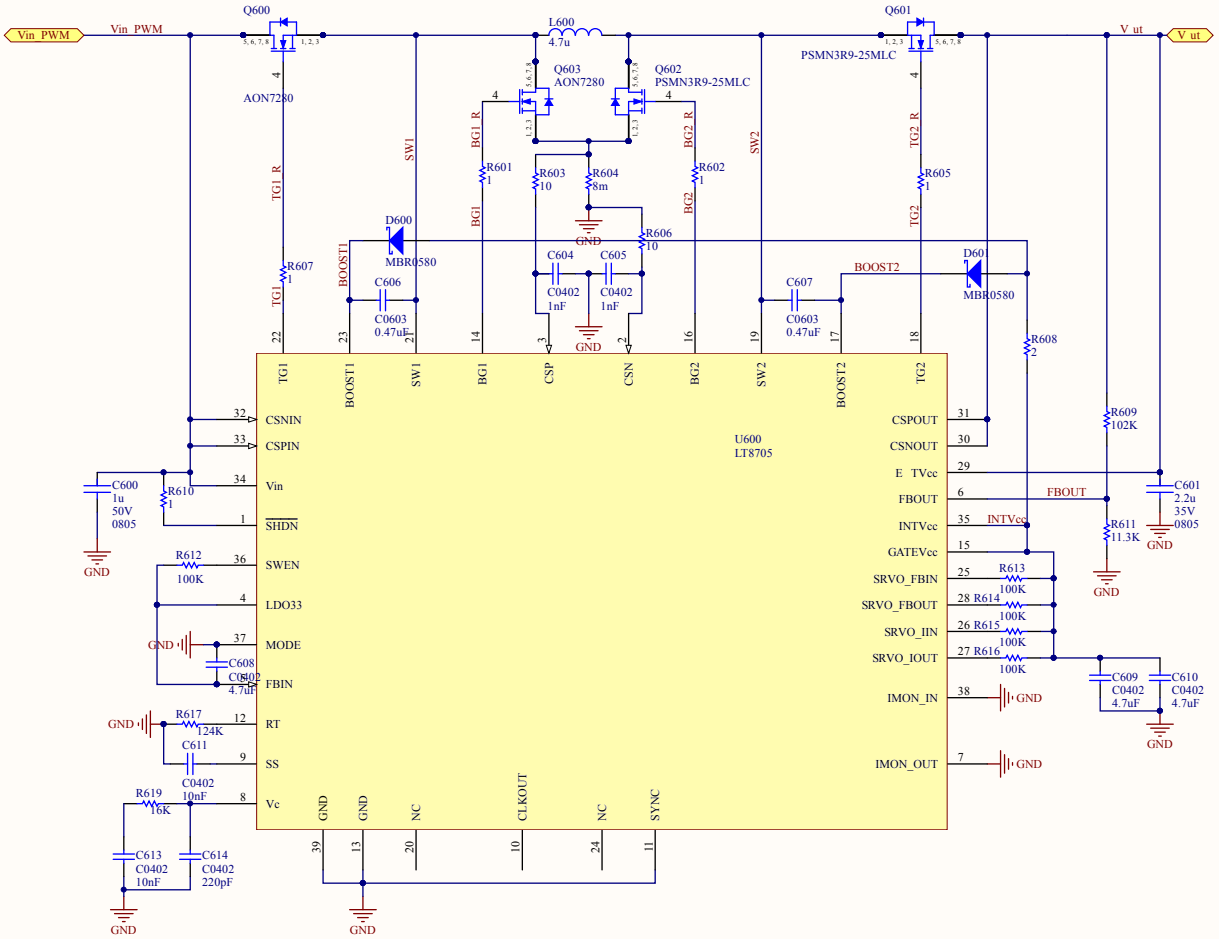
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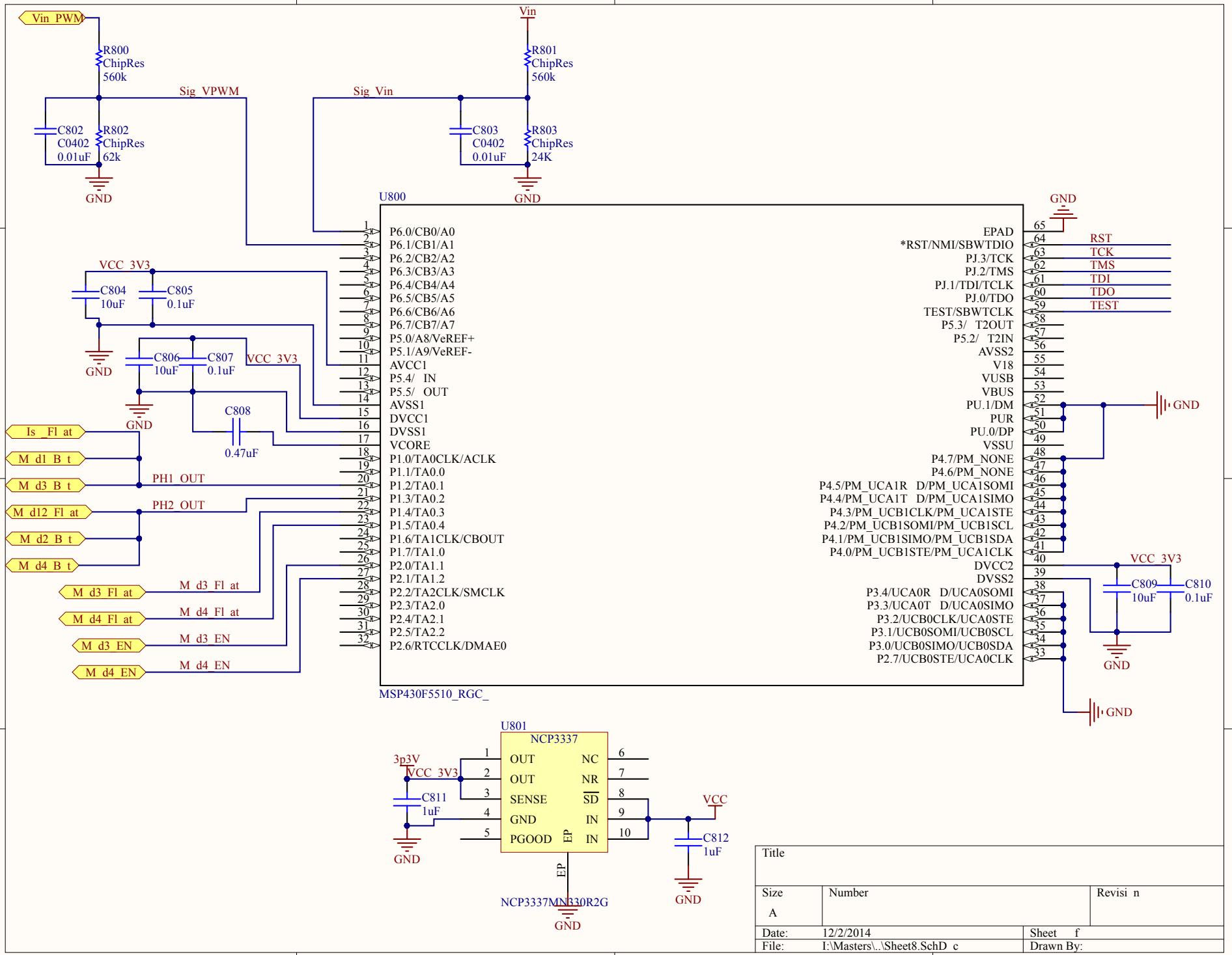
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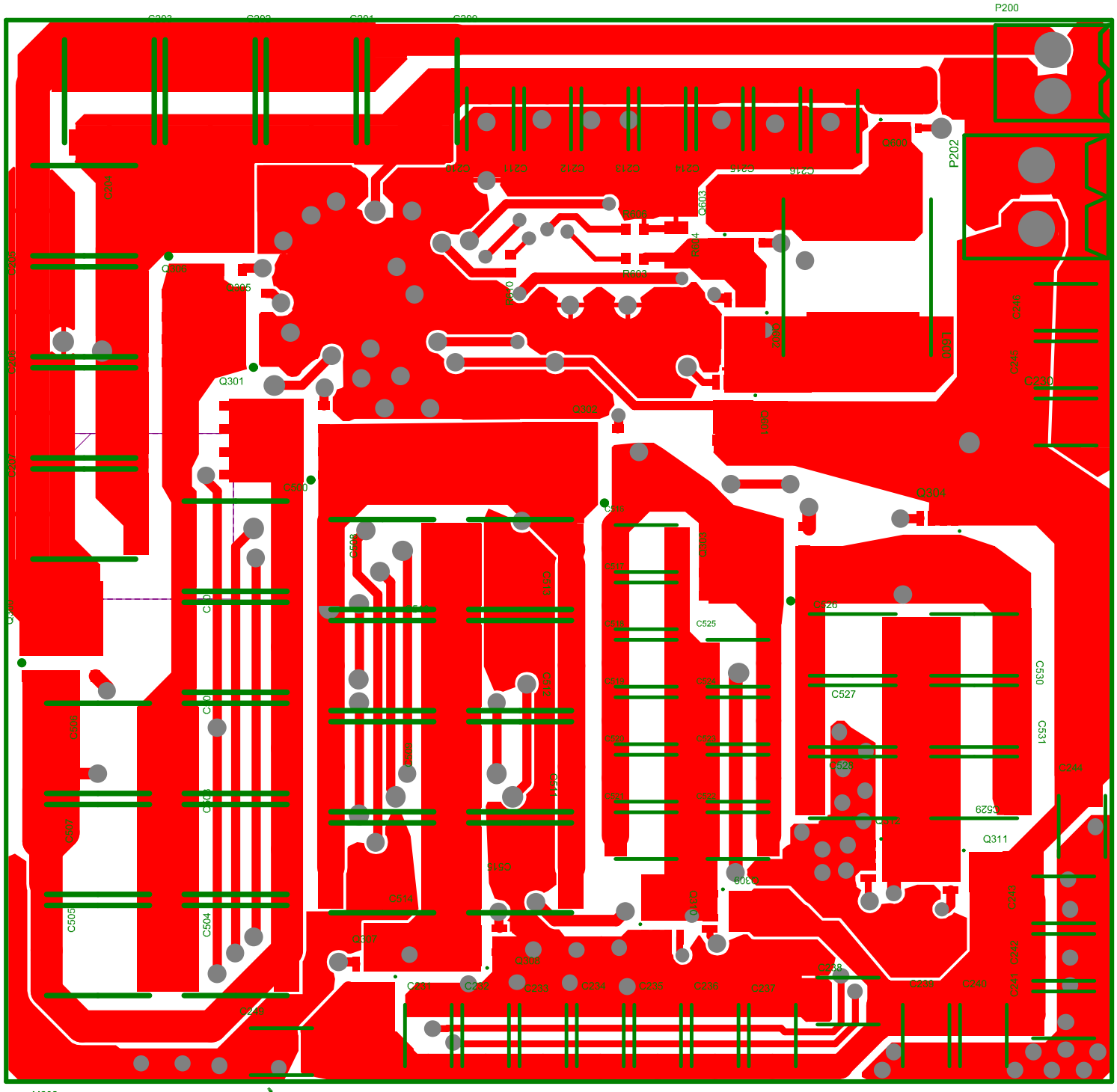


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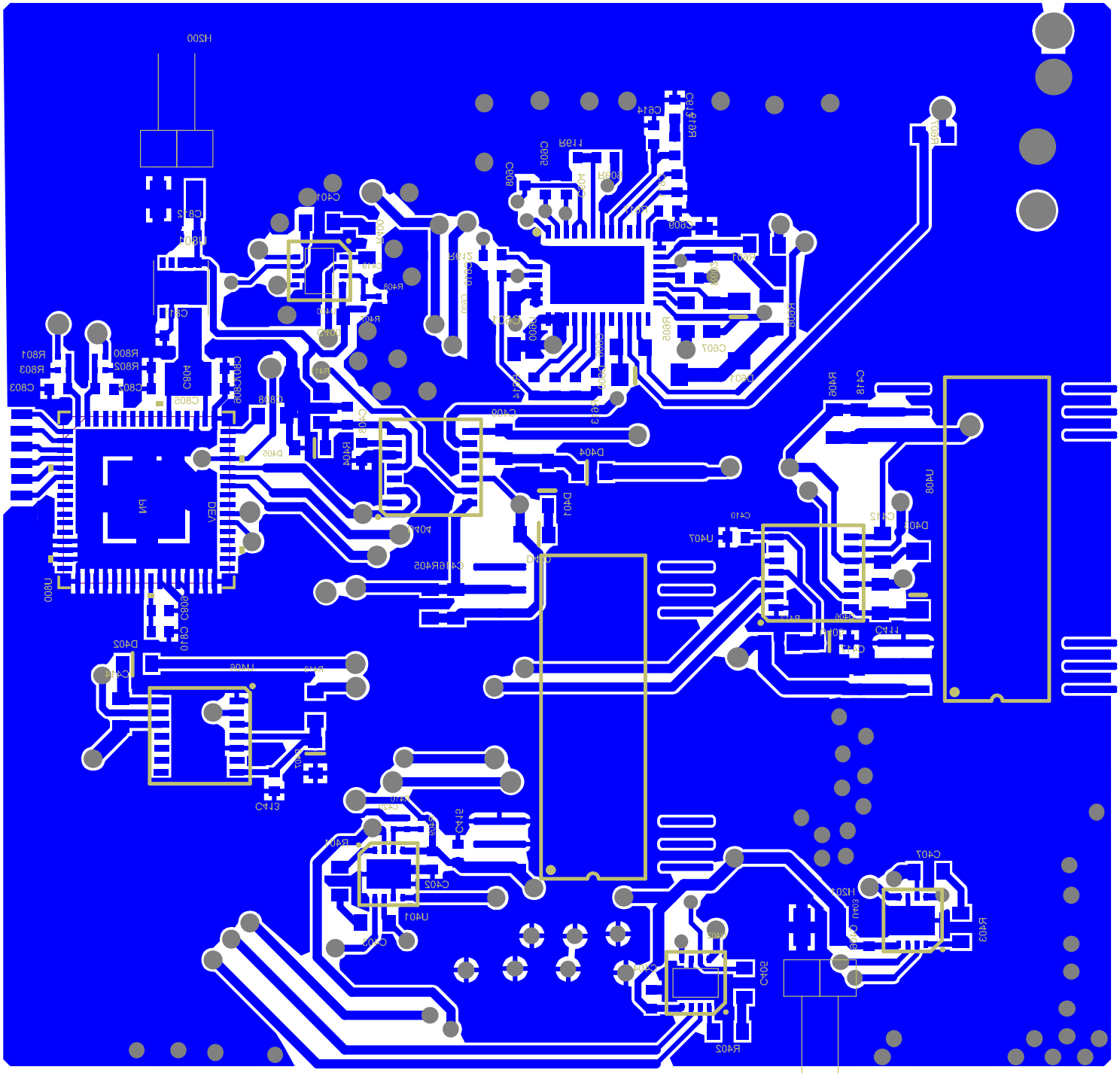
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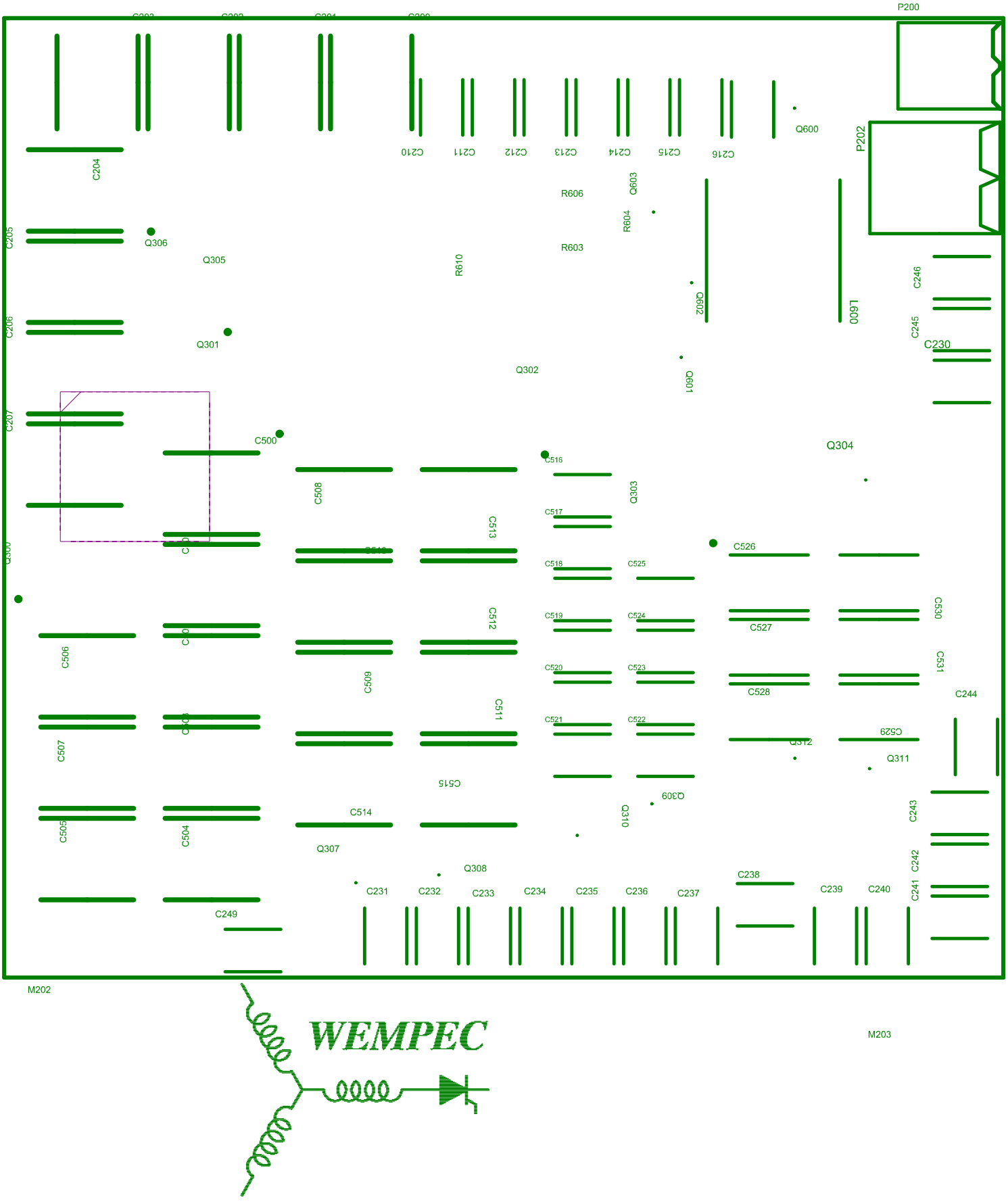
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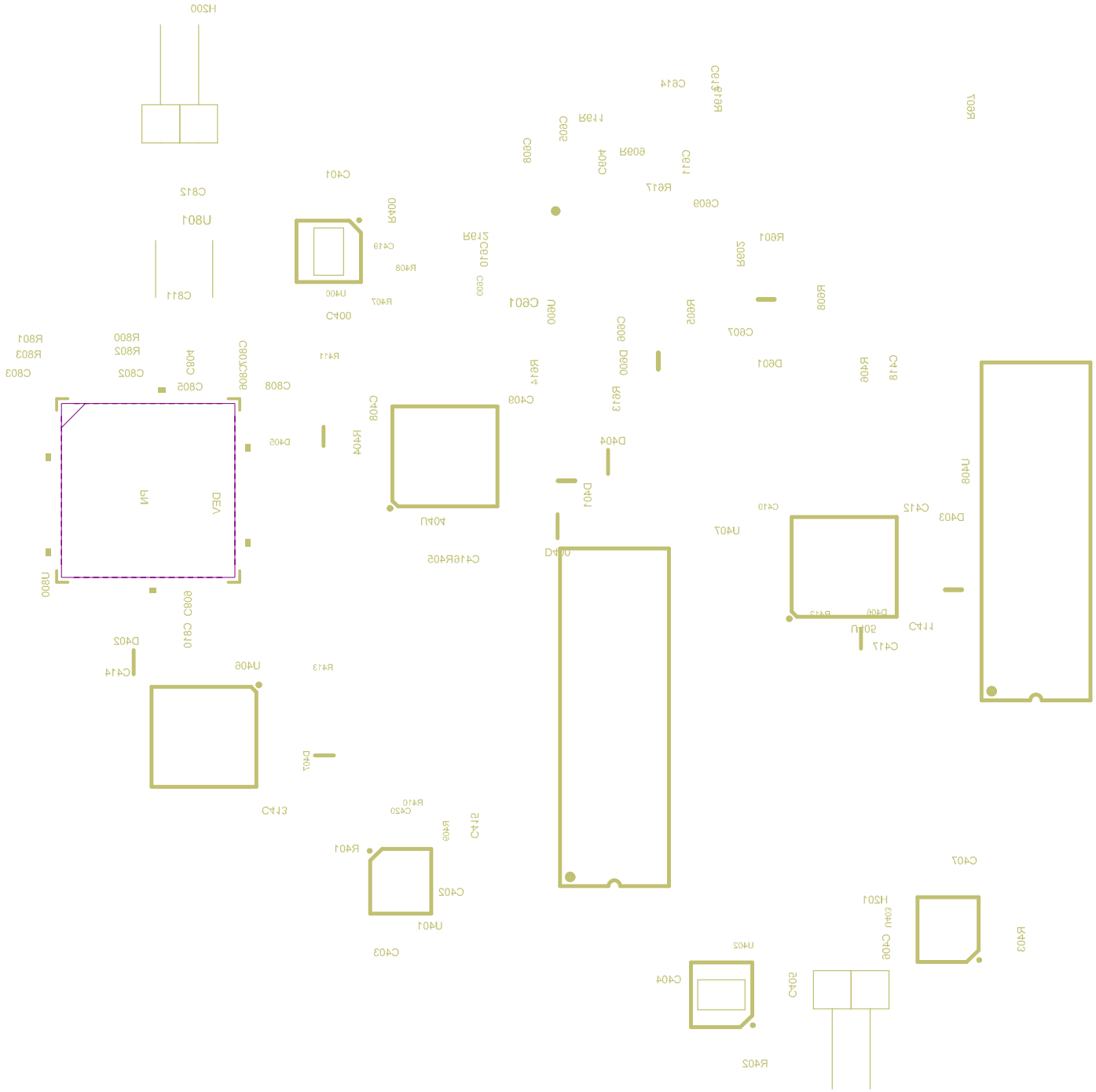
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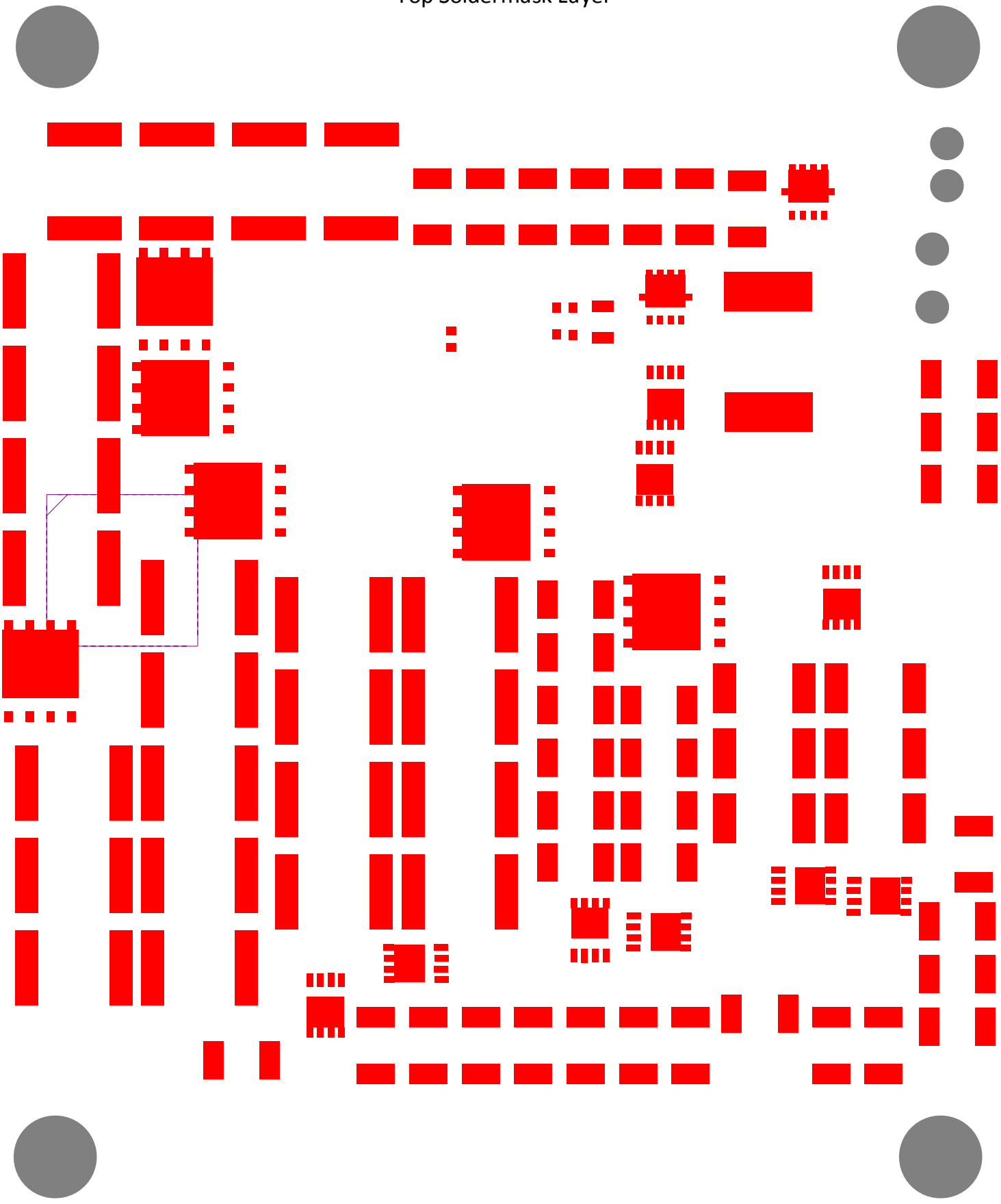
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Bottom Overlay Layer



Top Soldermask Layer



Bottom Soldermask Layer

