Doubling-resolution analog-to-digital conversion based on PIC18F45K80

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Published in *The Journal of Engineering*; Received on 30th June 2014; Accepted on 30th June 2014

Abstract: Aiming at the analog signal being converted into the digital with a higher precision, a method to improve the analog-to-digital converter (ADC) resolution is proposed and described. Based on the microcomputer PIC18F45K80 in which the internal ADC modules are embedded, a circuit is designed for doubling the resolution of ADC. According to the circuit diagram, the mathematical formula for calculating this resolution is derived. The corresponding software and print circuit board assembly is also prepared. With the experiment, a 13 bit ADC is achieved based on the 12 bit ADC module predesigned in the PIC18F45K80.

1 Introduction

The analog-to-digital converter (ADC) is usually used for digital signal processing, recording and scientific instruments. The ADC resolution and the signal input range are the primary concern [1, 2]. With the intention to realise a high-resolution ADC output, designers have been making efforts to improve it in circuits, software and so on. So far, a multi-step ADC [3, 4] and an over sampling technique [5, 6] have been applied widely. Besides, Coleman declared a resolution enhancer circuit [7] to pre-scale the input to be within an operable range of ADC. Choi [8] utilised a digital control system to configure two circuits to generate their respective analog value. However, in all of those methods, the input analog signal is the object being processed directly. In this Letter, a new method for increasing the ADC resolution is described, including its circuit, algorithm derivation and software, based on the microcomputer PIC18F45K80.

2 Circuit

As illustrated in Fig. 1*a*, the microcomputer PIC18F45K80 is one of the most widely used microcomputers. Ten 12-bit standard ADC modules are predesigned in it [9]. In this designed circuit, the analog signal input ports RA2 and RA3 are used as ADC external analog reference inputs, $V_{\text{ref}+}$ and $V_{\text{ref}-}$. The working state of relay RAY_1 is controlled by the output port RC5. A high level '1' in RC5 is to switch on the negative-positive-negative (NPN) triode Q_1, and low level '0' to switch off the Q_1. The input port RA0 is configured as the input of the analog signal. The resistances R_1 and R_2 are applied to pre-scale the voltage '*Vdd*'. The $V_{\text{ref}+}$ is shifted between '*Vdd*' and '$Vdd \times (R_2/R_1 + R_2)$'. Synchronously, the $V_{\text{ref}-}$ is shifted between '$Vdd \times (R_2/R_1 + R_2)$' and '*Vss*'. The R_3 and R_4 are assigned for current limiting. Capacitors C_1, C_2, C_3 and C_4 will improve the circuit anti-jamming ability.

The processing described in Fig. 1*b* provides two groups of different analog references for $V_{\text{ref}+}$ and $V_{\text{ref}-}$. Firstly, the port RC5 output '0' or '1'. Secondly, the triode Q_1 works in cut off or saturated region. Thirdly, the 'pin2' in the relay 'RAY1' is switched to 'pin3' or 'pin1', and 'pin7' to 'pin6' or 'pin8'. Finally, two groups of analog reference '*Vdd*, $Vdd \times (R_2/R_1 + R_2)$' and '$Vdd \times (R_2/R_1 + R_2)$, *Vss*' are, respectively, configured to $V_{\text{ref}+}$ and $V_{\text{ref}-}$.

3 Algorithm

Depending on Fig. 1*a* and before description of this circuit, with the outputting of '0' or '1' in the port RC5, the triode Q_1 will work in the cut off or saturated state, and the pin3 and pin6 of RAY_1 or the pin1 and pin8 will be connected to pin2 or pin7. The voltage of $V_{\text{ref}+}$ and $V_{\text{ref}-}$ will be defined by (1) or (2)

$$\begin{cases} V_{\text{ref}-} = Vss \\ V_{\text{ref}+} = Vdd \times \dfrac{R_2}{R_1 + R_2} \end{cases} \tag{1}$$

$$\begin{cases} V_{\text{ref}-} = Vdd \times \dfrac{R_2}{R_1 + R_2} \\ V_{\text{ref}+} = Vdd \end{cases} \tag{2}$$

Accordingly, an N-bit analog-to-digital (A/D) operation will be performed in the below steps: in the first step, an ADC output

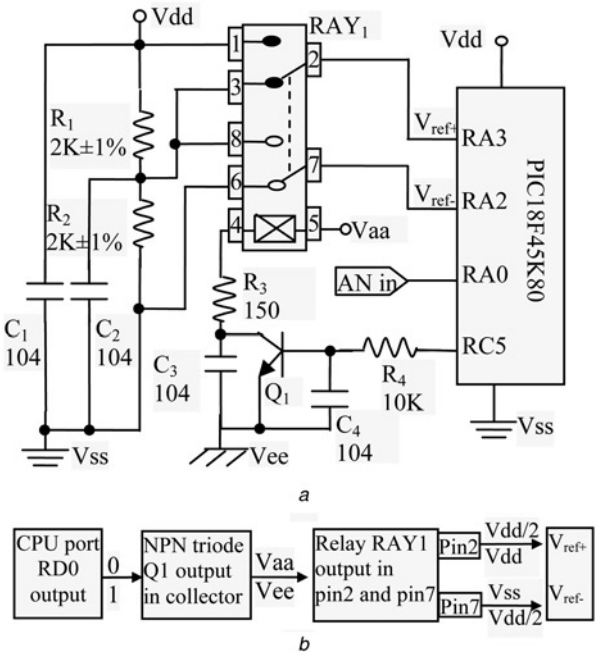

Fig. 1 *Circuit diagram and control processing*
a Circuit diagram
b Control processing
Vdd: 5VDC ± 1% requested by PIC18F45K80 and digital circuit
Vaa: another 5VDC ± 1% for analog circuit
Vss: digital ground
Vee: analog ground
AN in: analog input
0/1: low or high-level voltage

doi: 10.1049/joe.2014.0161

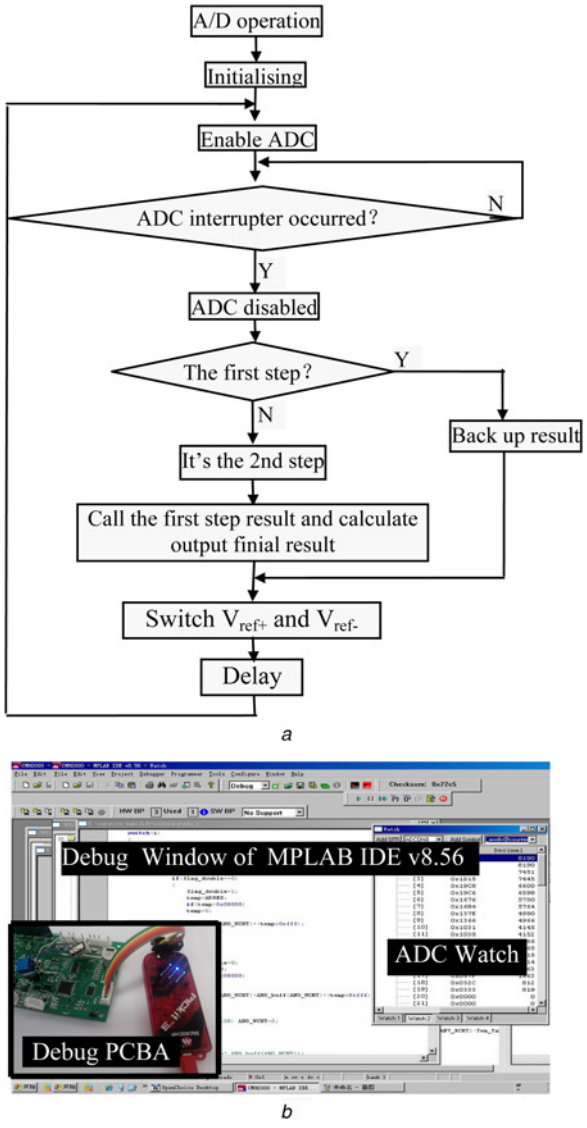

Fig. 2 *Flowchart for A/D operation and the debug windows*
a Flowchart
b Debugging windows
Debug PCBA is connected to personal computer via a debugger PICKit™3
In ADC watch, the results of ADC are displayed. The programme is edited and simulated under MPLAB IDE v8.56

'AD1' expressed in (3) is carried out when the circuit is working with the V_{ref+} and V_{ref-} meeting (1). In the second step, another output 'AD2' expressed in (4) when the circuit is working with the V_{ref+} and V_{ref-} meeting (2). In below equations, the 'Vin' is the voltage of analog signal (see (2) and (3)).

Table 1 ADC results

Names	Data					
input, V	0.0	1.0	2.0	3.0	4.0	5.0
test ADC, D_{tst}	0	1663	3365	4966	6600	8190
theoretical ADC, D_{the}	0	1638	3276	4914	6552	8191
difference, %	/	1.5	2.7	1.0	0.7	0

Note: $D_{the} = (V\text{in} - 0)/5*(2\text{^}13-1)$. The difference% $= (D_{tst} - D_{the})/D_{the}*100\%$.

Since $R_1 = R_2$, the final output of the ADC is the sum of the first and the second steps, as expressed in (5). Compared with the N-bit ADC output standard expression [10] '$(V\text{in} - V_{ref-}/V_{ref+} - V_{ref-})(2^N - 1)$', the '$ADr$' in (6) is our desired expression. The 'Vin' stands for the analog input. An $(N + 1)$-bit ADC (its resolution is $(V_{ref+} - V_{ref-}/2^{N+1})$) is achieved based on the N-bit ADC (its resolution is $(V_{ref+} - V_{ref-}/2^N)$)

$$\mathrm{AD} = \mathrm{AD1} + AD2 = \frac{V\text{in} - Vss}{Vdd - Vss} \times (2^{N+1} - 2) \quad V\text{in} \in [Vss,\ Vdd] \tag{5}$$

$$\mathrm{AD}r = \mathrm{AD} \times \left(1 + \frac{1}{2^{N+1} - 2}\right) = \frac{V\text{in} - Vss}{Vdd - Vss}(2^{N+1} - 1) \quad V\text{in} \in [Vss,\ Vdd] \tag{6}$$

4 Programming

As described in Fig. 2*a*, when powered on, the microcomputer will firstly initialise all of registers related to the ADC module including '$V_{ref+} = Vdd/2$' and '$V_{ref-} = Vss$'. Then A/D operation is enabled. Thereafter, the ADC interrupter carries out the ADC result in time. When A/D conversion is completed every time, the A/D operation is disabled to avoid wrong operation. Then, the A/D operation step is determined for the first step or second step. The ADC result will be calculated out in the second step. Or, in the first step, the ADC result is backed up until being requisitioned in the next step – the second step operation. Correspondingly, the V_{ref+} and V_{ref-} are assigned in accordance with (3) and (4). The final result is calculated out with (5) and (6) performed.

5 Tests and results

Based on the designed circuit as described in Fig. 1*a*, a debug print circuit board assembly (PCBA) is prepared as shown in Fig. 2*b*. The relay RAY1 is the Omron G6S-2G. Under the environment of MAPLAB IDE v8.56 software, we run the debugger and input the analog signals from 0 V to 5 V ± 1%. The results are listed in Table 1. Depending on these ADC results, the ADC resolution is doubled as the predesigned 12-bit.

In Table 1, the test ADC (D_{tst}) values are the results carried out in the experiment. The theoretical ADC (D_{the}) value is calculated out with '$(V\text{in} - 0)/5*(2\text{^}13-1)$'. The difference between the test ADC value and the theoretical ADC value is calculated out with

$$\mathrm{AD1} = \begin{cases} \dfrac{V\text{in} - Vss}{Vdd \times \dfrac{R_2}{R_1 + R_2} - Vss} \times (2^N - 1) & V\text{in} \in \left[Vss,\ Vdd \times \dfrac{R_2}{R_1 + R_2}\right) \\ 2^N - 1 & V\text{in} \in \left[Vdd \times \dfrac{R_2}{R_1 + R_2},\ Vdd\right] \end{cases} \tag{3}$$

$$\mathrm{AD2} = \begin{cases} 0 & V\text{in} \in \left[Vss,\ \dfrac{Vdd \times R_2}{R_1 + R_2}\right) \\ \dfrac{V\text{in} - Vdd \times (R_2/R_1 + R_2)}{Vdd - Vdd \times (R_2/R_1 + R_2)} \times (2^N - 1) & V\text{in} \in \left[\dfrac{Vdd \times R_2}{R_1 + R_2},\ Vdd\right] \end{cases} \tag{4}$$

'$(D_{tst} - D_{the})/D_{the}$*100%'. Owing to the precisions of resistances, *Vdd* and analog input are ±1% (total relative error should be ±3%), the experimental results of ADC are in the reasonable range.

6 Conclusion

A method for doubling an ADC resolution is described based on circuit diagram and a microcomputer with the internal ADC module. An *N*-bit ADC resolution is doubled by applying this method.

By applying a 12-bit ADC module integrated in the microcomputer PIC18F45K80, the relevant PCBA and software were designed for experiment, and a 13-bit ADC is realised in the experiment.

7 Acknowledgment

This project is supported by the Chinese Universities Scientific Fund (number: 14D310302).

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