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Seven-level inverter with switched capacitors

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Abstract: The seven-level (7L) inverter with a nearly sinusoidal output voltage is suitable for renewable energy conversion applications. A novel 7L inverter topology with switched capacitors is proposed here. The topology is composed of an active clamping inverter and a switched-capacitor part in series connection. The switched-capacitor part, consisting of three switches and two clamped capacitors, can provide 1/3 or 2/3 level of output voltage. By connecting switched-capacitor part in forward or backward series to the inverter output, a 7L output voltage waveform can be obtained with enough redundancy switching states to balance the voltage of switching capacitors. A modified modulation method is also proposed to make the topology operating properly. The voltage of switched-capacitor part can be sustained E and $2E$ alternately by adjusting a modulation index according to the capacitor voltage and load current. The effectiveness of the proposed topology is validated by both simulative and experimental results. Comparing with conventional 7L inverter topology, less number of devices were adopted in the proposed topology with a simple and practicable modulation method.

1 Introduction

Multilevel inverters have been widely used in renewable energy conversion applications due to small volume, high efficiency, and high power quality [1–3]. There is a growing interest in the studies of multilevel inverters including their topologies and modulation methods. The five-level inverter has been studied to a great extent and can be roughly categorised into three groups: diode clamped inverter, flying capacitor inverter, and cascaded H-bridge inverter [4–6]. The higher output voltage level is a necessary concern that influences output performance of multilevel inverters. As these five-level topologies are hard to extend to seven-level (7L) topologies limited by volume, cost, efficiency and power quality [7–9]. Therefore, it is logic and desirable to find a simplified topological structure to achieve 7L output voltage [10–12].

There have been considerable researches on the 7L inverter. A 7L inverter topology consisting of two unsymmetrical DC power sources has been presented in [13], which cannot guarantee clamped capacitor voltage stability in actual and dynamic situations. Sun *et al*. [14] present a cascaded structure of the 7L inverter topology with a single source, which still needs a number of power switches. A new type of 7L active neutral point clamped inverter topology that utilises half-bridge PEBB is presented in [15], and it suffers from large number of DC sources. Hybrid 7L inverter topology with a single DC is in [16], whereas the topology requires complex capacitor voltage balancing algorithm.

Once the topology of the multilevel inverter is specified, a proper modulation method is critical, which determines the output performance such as waveform quality and efficiency [17–19]. Modulation methods such as space vector pulse-width modulation (PWM), carrier disposition modulation, and carrier phase shift modulation have been designed for multilevel inverters [18, 20, 21]. More specifically, for space vector PWM technology, as the output voltage levels increase, the number of basic vector and the choice of the redundant states are relatively complex, which are not suitable for 7L inverter. In [22], the phase opposition disposition modulation method is used for improved 7L active neutral point clamped inverter. Although problem of multistep jumps in output voltage is solved, the output voltage harmonic content also increases. The sine PWM method with a single carrier is utilised in [23] to achieve the modulation of mixed cascaded 7L inverter. Two reference signals with opposite amplitude are used in [24] to generate the driven signals of switches. The total harmonic distortion (THD) of its output voltage is fine, whereas the inverter is in low efficiency.

The main contributions of this paper are listed as follows:

i. A novel 7L inverter topology with switched capacitors is proposed, which demonstrates a reduction in device count and gate driver signals. Switched-capacitor part is able to generate 1/3 or 2/3 level of output voltage. The 7L voltage waveform can be formed by connecting switched-capacitor part in forward or backward series to the active clamping inverter.
ii. A modulation method based on the decomposition of modulation signal according to the series and parallel states is processed. Also, the clamped capacitor voltage control method is developed by adjusting the modulation index.

This paper is organised as follows: Section 2 presents the topology and operating principles of the proposed 7L inverter. Section 3 deals with the modulation method. Section 4 discusses the clamped capacitor control method. Section 5 reports simulation and experimental results. Section 6 concludes the work. Section 7 shows the acknowledgements.

2 7L inverter topology and operating principles

2.1 Topology of 7L inverter

The structure of a novel 7L inverter with switched capacitors is shown in Fig. 1. The proposed topology is composed of an active clamping inverter and switched-capacitor part, and the former is accountable for the generation of multilevel voltage, while the latter is accountable for the increase in redundancies. The switched-capacitor part consists of three switches S_9, S_{10}, and S_{11} and two clamped capacitors C_3 and C_4 shown in the red dashed box of Fig. 1, which are able to generate two voltage levels (E and $2E$) with the rated voltage E of C_3 and C_4. As states of S_9, S_{10}, and S_{11} switches, C_3 and C_4 are in series or parallel connection, the switched-capacitor part is capable of generating E and $2E$ voltage levels. When the current i_C of the clamped capacitor part flows into point c and flows out point d, the switched-capacitor part is in forward series to the active clamping inverter, and on the contrary,

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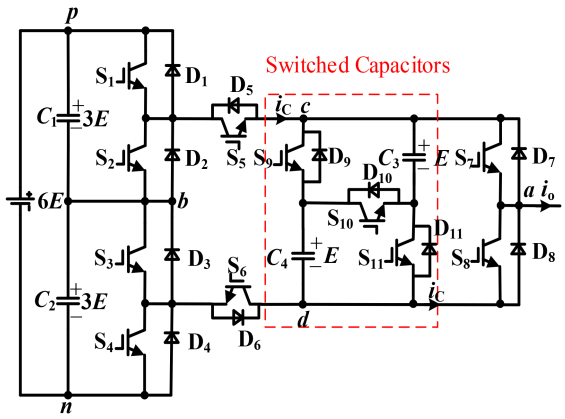


Fig. 1 *Topology of novel 7L inverter with switched capacitors*

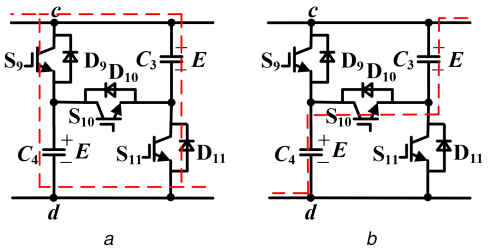


Fig. 2 *Switching states of switched-capacitor part*
(a) Parallel state, ***(b)*** Series state

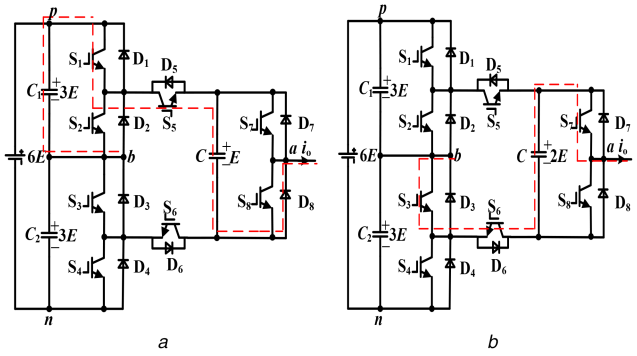


Fig. 3 *Switching states of active clamping inverter at 2E level of output voltage*
(a) Switching state *a*, ***(b)*** Switching state *b*

if i_C flows out point *c* and flows into point *d*, the switched-capacitor part will be in backward connection to the active clamping inverter. By connecting switched-capacitor part in forward or backward series to the active clamping inverter, 7L voltage through $-3E$ to $3E$ with the interval of E can be formed. The DC link comprises two capacitors in series connection with the rated voltages $3E$ of C_1 and C_2. Assuming that the neutral point *b* is zero potential and output current i_o is positive when flowing out of point *a*.

2.2 Operating principles of switched-capacitor part

As switching states of S_9, S_{10}, and S_{11} switches, C_3 and C_4 are in series or parallel connection, switched-capacitor part generates E and $2E$ voltage levels. Meanwhile, redundancy switching states at E and $2E$ levels increase, which is benefit to balance the voltage of clamped capacitor C_3 and C_4. Operation principles of switched-capacitor part are shown in Fig. 2.

From Fig. 2*a*, when switches S_9 and S_{11} are conducted and S_{10} is blocked, clamped capacitor C_3 and C_4 are connected in parallel, in this way, output voltage of switched-capacitor part is E.

From Fig. 2*b*, when switches S_9 and S_{11} are blocked and S_{10} is conducted, clamped capacitor C_3 and C_4 are connected in series, and the output voltage of switched-capacitor part is $2E$.

For the two cases, current flows into the clamped capacitor C_3 and C_4 when they are in forward connection to the active clamping inverter and out of them when they are in backward connection to the active clamping inverter.

2.3 Operating principles of active clamping inverter

The switched-capacitor part can be considered as a clamped capacitor C, where the voltage is E and $2E$ levels alternately. Fig. 3 shows the current path and switching states for $2E$ level of 7L inverter output voltage.

From Fig. 3*a*, when voltage of equivalent clamped capacitor C is E and switches S_1, S_3, S_5, and S_8 are conducted. If output current i_o is positive, switched-capacitor part is in forward connection to the circuit, and the current path is $S_1 \rightarrow S_5 \rightarrow C \rightarrow D_8 \rightarrow a \rightarrow b \rightarrow C_1$; if output current i_o is negative, switched-capacitor part is in backward connection to the circuit, and the current path is $a \rightarrow S_8 \rightarrow C \rightarrow D_5 \rightarrow D_1 \rightarrow C_1 \rightarrow b$.

From Fig. 3*b*, when voltage of equivalent clamped capacitor C is $2E$ and switches S_1, S_3, S_6, and S_7 are conducted. If output current i_o is positive, the switched-capacitor part is in backward connection to the circuit, and the current path is $S_3 \rightarrow D_6 \rightarrow C \rightarrow S_7 \rightarrow a \rightarrow b$; if output current i_o is negative, switched-capacitor part is in forward connection to the circuit, and the current path is $a \rightarrow \mathrm{D}_7 \rightarrow C \rightarrow S_6 \rightarrow D_3 \rightarrow b$.

2.4 Operating principles of novel 7L inverter with switched capacitors

With the combination of voltages from DC-link capacitors and switched capacitors, the proposed inverter is capable of outputting the 7L voltage waveform. The voltage combination patterns and states of clamped capacitors are listed in Table 1. In Table 1, u_{ab}, u_{pn}, and u_{cd} represent output voltage of the proposed 7L inverter, voltage of DC-link input, and voltage of switched-capacitor part, respectively; '/' represents that the clamped capacitor is bypassed; $i_o > 0$ indicates that output current flows out point *a*, and $i_o < 0$ indicates that output current flows into point *a*. '+' represents the clamped capacitor is charged, while '−' represents the clamped capacitor is discharged. There are two redundant switching states at E and $2E$ levels of output voltage, respectively, so clamped capacitors are in charge and discharge states correspondingly. It is vital to select switching states under different current directions, resulting in generating 7L output voltage waveform.

There are totally 12 switching states from 1 to 12 of the proposed 7L inverter. For instance, switching states at $2E$ level are discussed in detail.

Switching state 2: Switches S_1, S_3, S_5, S_8, S_9, and S_{11} are conducted, so in this way, the positive electrodes of the DC-link capacitor C_1 and the clamped capacitor C_3 and C_4 are connected together with C_3 and C_4 in parallel connection. Additionally, the voltage across C_1 is $3E$, C_3 and C_4 are both E, after $3E$ minus E, $2E$ level of output voltage is then obtained. According to this switching state, the current path is shown in Fig. 4*a*. If output current i_o is positive, the current paths are depicted as $S_1 \rightarrow S_5 \rightarrow S_9 \rightarrow C_4 \rightarrow D_8 \rightarrow a \rightarrow b \rightarrow C_1$ and $S_1 \rightarrow S_5 \rightarrow C_3 \rightarrow S_{11} \rightarrow D_8 \rightarrow a \rightarrow b \rightarrow C_1$, C_3 and C_4 both charge during this state. If output current i_o is negative, the current paths are depicted as $a \rightarrow S_8 \rightarrow C_4 \rightarrow D_9 \rightarrow D_5 \rightarrow D_1 \rightarrow C_1 \rightarrow b$and $a \rightarrow S_8 \rightarrow D_{11} \rightarrow C_3 \rightarrow D_5 \rightarrow D_1 \rightarrow C_1 \rightarrow b$, thus, C_3 and C_4 both discharge.

Switching state 3: Switches S_1, S_3, S_6, S_7, and S_{10} are conducted, so in this way, the negative electrodes of the clamped capacitor C_4 and zero potential point *b* are connected together with C_3 and C_4 in series connection. Additionally, as rated voltages of DC link are zero, C_3 and C_4 are both E, after 0 adds $2E$, $2E$ level of output voltage is then obtained. According to this switching state, the current path is shown in Fig. 4*b*. If output current i_o is positive, the current paths are described as

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Table 1 7L output voltage and states of clamped capacitors

S. no.	u_{ab}	u_{pn}	u_{cd}	C_3/C_4 states	
				$i_o > 0$	$i_o < 0$
1	3*E*	3*E*	/	/	/
2	2*E*	3*E*	*E*	+	−
3	2*E*	0	2*E*	−	+
4	*E*	0	*E*	−	+
5	*E*	3*E*	2*E*	+	−
6	0	0	/	/	/
7	0	0	/	/	/
8	−*E*	0	*E*	+	−
9	−*E*	−3*E*	2*E*	−	+
10	−2*E*	−3*E*	*E*	−	+
11	−2*E*	0	2*E*	+	−
12	−3*E*	−3*E*	/	/	/

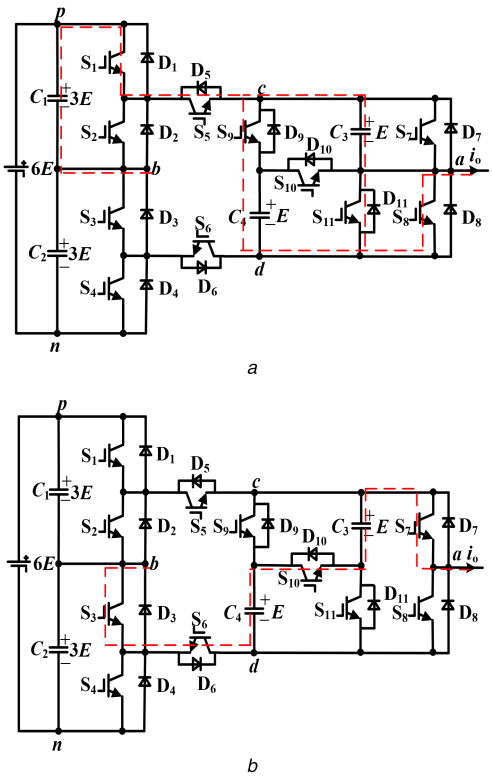


Fig. 4 *Switching states of 7L inverter with switched capacitors at 2E level*
(a) Switching state 2, ***(b)*** Switching state 3

$S_3 \rightarrow D_6 \rightarrow C_4 \rightarrow S_{10} \rightarrow C_3 \rightarrow S_7 \rightarrow a \rightarrow b$, thus C_3 and C_4 are both in discharge condition. On the other hand, if output current i_o is negative, the current paths are described as $a \rightarrow D_7 \rightarrow C_3 \rightarrow D_{10} \rightarrow C_4 \rightarrow S_6 \rightarrow D_3 \rightarrow b$, thus C_3 and C_4 both charge.

Analysis of the other ten kinds of switching states is similar. Table 2 illustrates different switching states at seven output voltage levels. From Table 2, '1' and '0' represent on and off states of switches, respectively; '/' represents state of the switch can either be 1 or 0. There are four pairs of complementary switches (S_1, S_2), (S_3, S_4), (S_5, S_6), (S_7, S_8), and (S_9, S_{10}) and three pairs of switches (S_1, S_3), (S_2, S_4), and (S_9, S_{11}) which require the same switching signal for each pair, respectively, so S_1, S_5, S_7, and S_9 are able to operate independently of each other to get rid of forbidden switching states.

3 Modulation method

As there are four independent switches S_1, S_5, S_7, and S_9 in the proposed topology, phase-shifted pulse-width modulation method can be adopted. To simplify modulation technology, a modified modulation wave is used to compare with two triangular carriers. The two carrier signals u_{ca1} and u_{ca2} are phase shifted by 180° and correspond to switch S_1, S_5, S_7, and S_9. The carrier signals range from 0 to 1/3 at the same frequency, and the sinusoidal modulation signal u_{ref} ranges from 0 to 1. The sinusoidal modulation signal needs to be rectified to guarantee normal performance during six intervals of output voltage, and revised modulation signal u_{ri} is shown as a piecewise function (1). The diagram of modulation method is shown in Fig. 5, and the revised modulation wave is drawn in bold yellow line. According to the aforementioned analysis of switching states, the switch S_1 is always on in the positive half cycle of the modulation wave and normally off in the negative half cycle. Switching states of one switch between S_5, S_7, and S_9 can be obtained by inverting the others during each output voltage internal

$$u_{ri} = \begin{cases} u_{ref} - 2/3 & u_{ref} \geq 2/3 \\ u_{ref} - 1/3 & 1/3 \leq u_{ref} < 2/3 \\ u_{ref} & -1/3 \leq u_{ref} < 1/3 \\ u_{ref} + 1/3 & -2/3 \leq u_{ref} < -1/3 \\ u_{ref} + 2/3 & u_{ref} < -2/3 \end{cases} \quad (1)$$

From Tables 1 and 2, different switching states have distinct impacts on the clamped capacitors. In order to ensure that clamped capacitors have both charging and discharging states which contribute to voltage balancing per carrier period, each internal of output voltage should has switching states corresponding to charging and discharging states. Taking positive half cycle for an example, the switching states 4/5 and 6 are chosen when the output voltage is from (0, *E*) and when the output voltage is from (*E*, 2*E*), the switching states 2/3 and 4/5 are chosen. Meanwhile, the switching states 1 and 2/3 are chosen when the output voltage is from (2*E*, 3*E*). The switching principles of different switching states in the whole output voltage internals of the new 7L inverter topology are shown in Fig. 6.

It can be seen from the above analysis that the switch S_1 is always on during the positive half cycle of carrier and S_5, S_7, and S_9 are frequently switched alternately throughout the whole carrier cycle. Therefore, the operating frequencies of the switches S_1–S_4 and S_5–S_{11} are consistent, respectively, switching frequency of S_5–S_{11} is equivalent to half of the bridge output switching frequency, and thus frequency doubling can be achieved.

Since the frequency of two carriers is high enough, the output current i_o can approximately be regarded as constant value in a carrier period. For switched capacitors, the differential equation of the clamped capacitor C_3 can be written as

$$C_3 \frac{\Delta u_{C_3}}{\Delta D_s T_s} = i_o \quad (2)$$

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Table 2 Switching states at different output voltage levels

S. no.	u_{ab}	S_1	S_5	S_7	S_9
1	$3E$	1	1	1	/
2	$2E$	1	1	0	1
3	$2E$	1	0	1	0
4	E	1	0	1	1
5	E	1	1	0	0
6	0	1	0	0	/
7	0	0	1	1	/
8	$-E$	0	1	0	1
9	$-E$	0	0	1	0
10	$-2E$	0	0	1	1
11	$-2E$	0	1	0	0
12	$-3E$	0	0	0	/

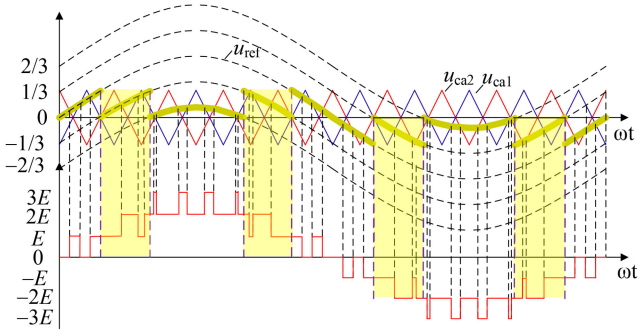


Fig. 5 *Principle of modulation*

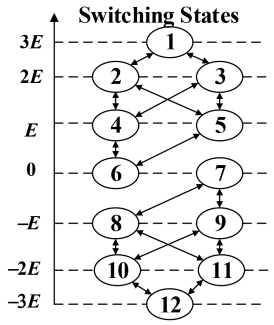


Fig. 6 *State machine of novel 7L inverter*

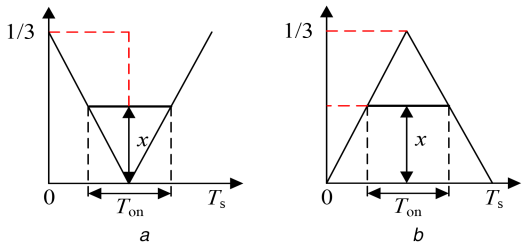


Fig. 7 *Relationship of D and x*
(a) Magnitude of modulation signal is larger, ***(b)*** Magnitude of carrier signal is larger

$$C_3\frac{\Delta u_{C_3}}{\Delta D_P T_s}=\frac{i_o}{2} \tag{3}$$

where ΔD_s is the duty ratio variation when clamped capacitor C_3 and C_4 are in series connection and ΔD_p the duty ratio variation when the clamped capacitor C_3 and C_4 are in parallel connection.

It can be seen from (2) and (3) that if the capacitor voltage variation at series and parallel states are the same, in order to maintain the clamped capacitor voltage to E in a carrier period, the change of the duty ratio during parallel state must be twice as much as that during series state. That is to say, the time of parallel state should be twice as much as that of series state. Fig. 7 shows the relationship of the duty ratio D and modulation signal magnitude x during the positive cycle.

Assuming that the magnitude of modulation signal is larger than the carrier wave, so the switch is turned on, as shown in Fig. 7*a*. Then, D can be written as

$$D=3x \tag{4}$$

When the PWM polarity is reversed, if magnitude of modulation signal is smaller than that of carrier signal, the switch is turned on as shown in Fig. 7*b*. So, D can be written as

$$D=1-3x \tag{5}$$

Based on (1)–(5), the revised modulation signal is able to be further decomposed during six intervals of output voltage, in this way, the decomposed modulation signal u_r is assigned to each switching state, as listed in Table 3. Based on the proposed topology, this kind of modulation wave decomposition method is the basis to realise the clamped capacitor voltage balancing.

4 Clamped capacitor control method

In the case of clamped capacitor C_3 voltage unbalanced, which will cause increased voltage harmonic distortion and affect output power quality, the clamped capacitor voltage should be balanced to E. To facilitate the discussion, ideal assumptions of the novel 7L inverter topology are made as follows: (i) the two clamped capacitors in switched-capacitor part are symmetrical with exactly the same parameters; (ii) the switching frequency is much larger than the fundamental frequency of output current, and output current can be considered unchanged per carrier period.

Considering the clamped capacitor C_3 as the research object (the same as C_4), C_3 are in charging and discharging states at the output level of $\pm E$ and $\pm 2E$, while is bypassed at other output levels. So, C_3 has both charging and discharging states during each output voltage internal.

The differential equation of C_3 voltage is written as

$$C_3\frac{\Delta u_{C_3}}{T_s}=(D_p-D_n)i_{C_3} \tag{6}$$

Based on (6), the reference and measured voltage deviation of C_3 is written as

$$\Delta u_{C_3}=T_s(D_p-D_n)i_{C_3}/C_3=\Delta D T_s i_{C_3}/C_3 \tag{7}$$

where D_p is the duty ratio of charging state, D_n the duty ratio of discharging state, and ΔD the deviation between D_p and D_n.

From (7), it can be seen that the voltage control of the clamped capacitor can be converted into the duty ratio control of the charging and discharging states. As long as the duty ratio of

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Table 3 Revised modulation signal under different switching states

u_{ab}	S. no.	u_r
(2E, 3E)	1	u_{ri}
	2	$(6u_{ri} + 1)/9$
	3	$(3u_{ri} + 2)/9$
(E, 2E)	2	$2/3u_{ri}$
	3	$1/3u_{ri}$
	4	$(6u_{ri} + 1)/9$
	5	$(3u_{ri} + 2)/9$
(0, E)	4	$2/3u_{ri}$
	5	$1/3u_{ri}$
	6	u_{ri}
(−E, 0)	7	u_{ri}
	8	$2/3u_{ri}$
	9	$1/3u_{ri}$
(−2E, −E)	8	$(6u_{ri} - 1)/9$
	9	$(3u_{ri} - 2)/9$
	10	$2/3u_{ri}$
	11	$1/3u_{ri}$
(−3E, −2E)	10	$(6u_{ri} - 1)/9$
	11	$(3u_{ri} - 2)/9$
	12	u_{ri}

charging and discharging states are equal in each carrier period, the clamped capacitor voltage can be maintained to a value.

If there is a voltage deviation between reference and measured voltage of C_3, the correction pulse of each switching transistor can be obtained in order to balance C_3 voltage by injecting a correction voltage into the reference modulation voltage. Therefore, the correction voltage can be considered as a controllable degrees of freedom, which is essential for C_3 voltage balancing.

Taking output voltage interval (0, E) and output current $i_o > 0$ as an example. For switching state 4, C_3 is discharged with C_3 and C_4 in parallel connection. Defining $2u_z$ is the correction voltage, so the corrected reference modulation voltage is written as

$$u_{rrp} = 2u_{ri}/3 - 2u_z \quad \in (0, 1/3) \tag{8}$$

For switching state 5, C_3 is charged with C_3 and C_4 in series connection. The correction voltage in this state must be u_z in order to ensure that voltage of the clamped capacitor is balanced in a carrier period. So, the corrected reference modulation voltage is as follows:

$$u_{rrs} = u_{ri}/3 + u_z \quad \in (0, 1/3) \tag{9}$$

While the charging state corresponds to the decomposed modulation voltage pluses correction voltage, discharging state corresponds to the decomposed modulation voltage minus correction voltage.

After overlaying the correction voltage, difference between the charging and discharging duty ratio can be expressed as

$$\Delta D = 3u_z \tag{10}$$

The overlaid correction voltage must be limited in the case of polarity changing of the reference modulation voltage. The maximum and minimum voltage correction are different during six output voltage internals. Three cases in terms of u_{ri} are discussed as follows.

Case I: When $u_{ri} < 1/4$, the range of u_z is written as follows:

$$-u_r/3 \le u_z \le u_r/3 \tag{11}$$

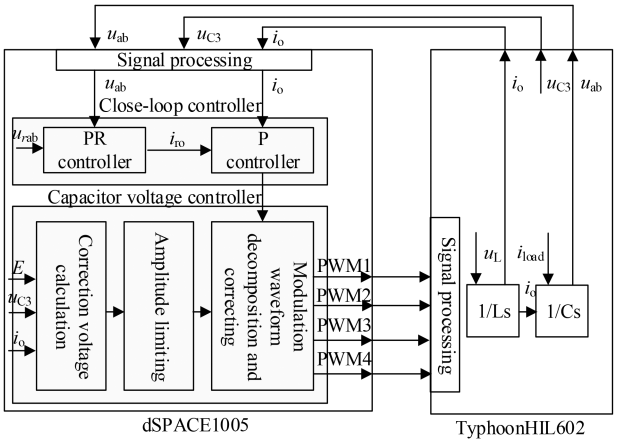


Fig. 8 *Flowchart of control methods*

Case II: When $1/4 \le u_{ri} \le 1/2$, the range of u_z is written as follows:

$$u_r/3 - 1/6 \le u_z \le u_r/3 \tag{12}$$

Case III: When $u_{ri} > 1/2$, the range of u_z is written as follows:

$$u_r/3 - 1/6 \le u_z \le 1/3 - u_r/3 \tag{13}$$

The correction voltage during other five intervals of output voltage can also be derived in this way. Detecting the clamped capacitor voltage and output current direction in each control cycle, thus, the clamped capacitor voltage control can be carried out by allocating charging and discharging states time.

5 Simulation and experimental results

To verify theoretical analysis, the behaviour of 7L inverter with switched capacitors has been verified by numerical simulations. Meanwhile, a single-phase 7L inverter prototype based on dSPACE1005 and TyphoonHIL602 has also been developed in the laboratory. Control methods include modified modulation, the clamped capacitor voltage balancing, and double close-loop control, as depicted in Fig. 8. The dSPACE 1005 is regarded as a main controller as well as four PWM signals generator and TyphoonHIL602 as the main circuit signals generator. The inner loop of output current and outer loop of output voltage are adopted for the double closed-loop control, while the inner loop uses P controller and the outer loop uses PR controller. To obtain the PWM signals, PWM and clamped capacitor algorithms are implemented. To illustrate the clamped capacitor control technology, for example, if the clamped capacitor voltage is smaller than the reference voltage E, a correction voltage greater than 0 will be gained with clamped capacitor control algorithm, and injecting it to the decomposed reference modulation voltage after limitation disposition, in this way, the modulation index is adjusted, then four PWM signals are obtained through PWM method and these signals are sent to TyphoonHIL602 as switch driver signals. As charging time increases and discharging time decreases per carrier cycle with this capacitor voltage controller, the clamped capacitor voltage is easy to be maintained at E.

The quantitative parameters for the proposed inverter are mentioned in Table 4, where carrier frequency f_s is 10 kHz, L and C_5 represent inductance and capacitance of the inductor and capacitor from the filter, respectively, and R represents load resistance.

In order to demonstrate the performance of the modified modulation method, Fig. 9 shows the simulation results of 7L output voltage, inductor current, and filtered output voltage with initial modulation index at 0.829. From Fig. 9*a*, a 7L output voltage waveform is obtained, and the peak value of it is 375 V, while the valley value is −375 V and each output voltage step is 125 V. Fig. 9*b* shows the inductor current, where the amplitude is ∼10 A. The filtered output voltage is nearly sinusoidal at

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Table 4 Values of elements in simulations and experiments

Parameter	Value
u_{pn}	750 V
u_{ab}	311 V/50 Hz
f_s	10 kHz
C_3/C_4	200 μF
C_5	4 μF
L	300 μH
R	32.26 Ω

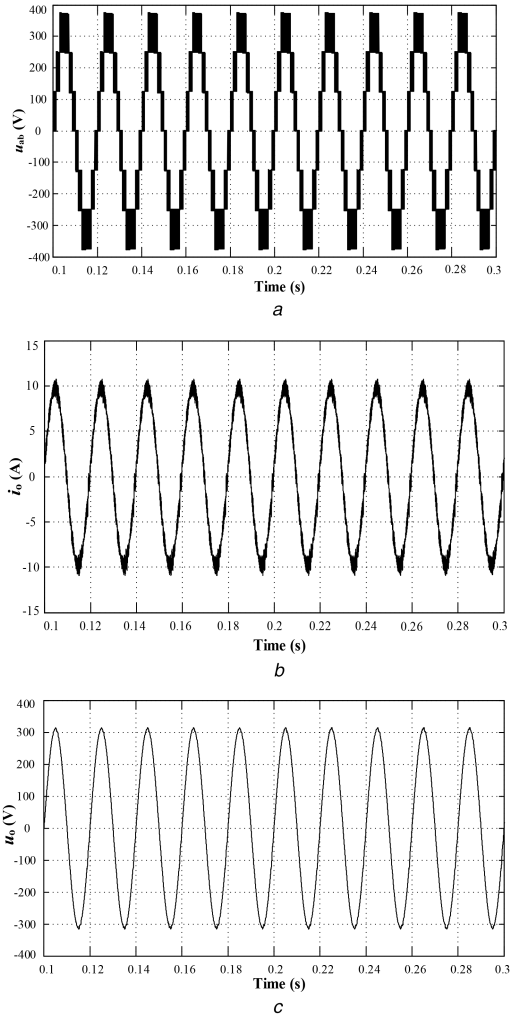


Fig. 9 *Simulation results of output voltage*
(a) 7L output voltage, ***(b)*** Inductor current, ***(c)*** Filtered output voltage

fundamental frequency of 50 Hz in Fig. 9*c*. Figs. 10*a* and *b* illustrate harmonic spectra of 7L voltage and filtered output voltage, respectively. The 7L voltage THD is 24.06%, while the filter output voltage THD is 0.53%. It can be seen that the fundamental amplitude of output voltage is 311.1 V, which means the effective value is 220 V.

The clamped capacitor voltage is plotted in Fig. 11. From Fig. 11*a*, with the proposed voltage balancing method, the voltage of clamped capacitor C_3 is balanced at 125 V with ripple of 1.28%, which is essential to generate 7L output voltage. From Fig. 11*b*, it is observed that one charging state and one discharging state are included in each carrier period, in other words, the clamped capacitor voltage can approximately be balanced per carrier period.

Fig. 12 shows the experiment results of output voltage; Fig. 12*a* is the 7L output voltage which matches with the result of simulation in Fig. 9*a*. The filtered output voltage is given in Fig. 12*b*. Fig. 13 shows the experimental results of clamped

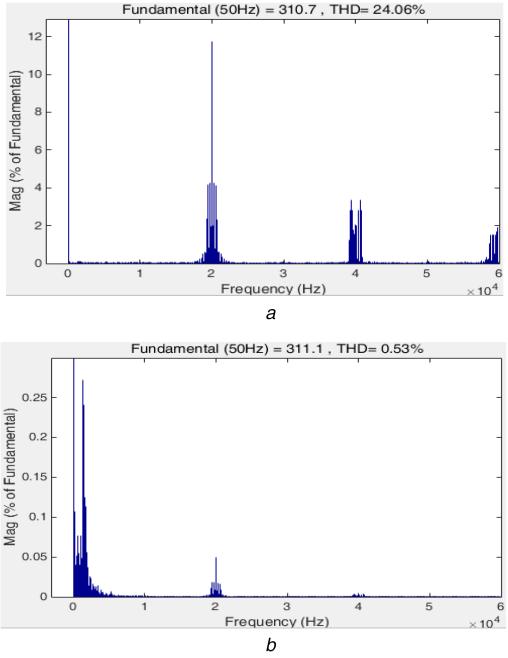


Fig. 10 *Harmonic spectra of output voltage*
(a) 7L output voltage, ***(b)*** Filtered output voltage

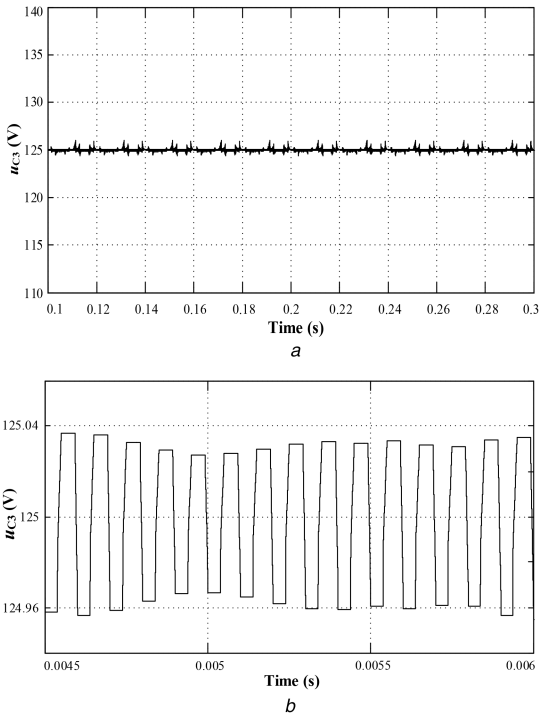


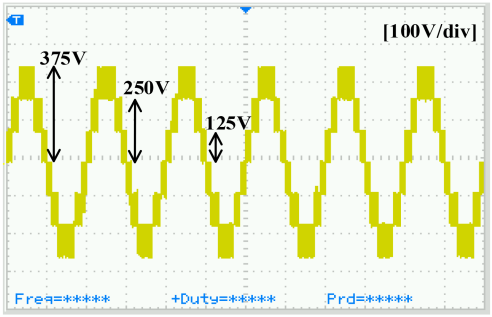
Fig. 11 *Clamped capacitor voltage*
(a) Scale of 0.02 s, ***(b)*** Scale of 500 μs

capacitor voltage, and matches with the result of simulation result in Fig. 11. These results validate the effectiveness of the proposed 7L topology and its modulation method.

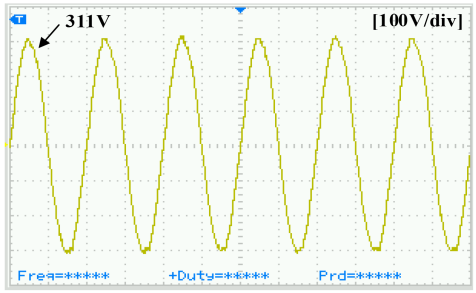
6 Conclusion

This paper has presented a novel 7L inverter with switched capacitors. The configuration utilises switched-capacitor part to generate two voltage levels E and $2E$, which increases the redundancy states. Also, the topology is able to realise seven output voltage levels with reduced number of switch transistors and gate drivers resulting in low cost. In addition, its modulation is processed by decomposing the revised modulation signal according to the series and parallel states. Also, the clamped capacitor voltage is controlled with the method of adjusting the modulation index.

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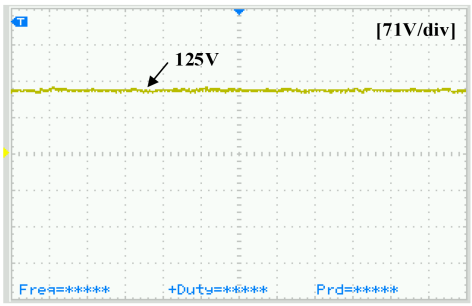


a

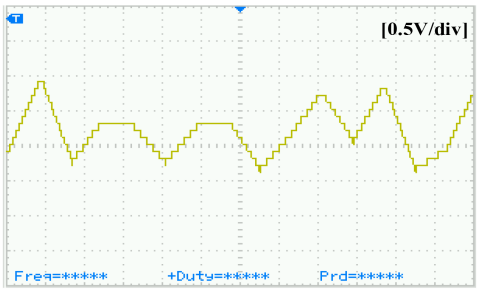


b

Fig. 12 *Experimental results of output voltage*
(a) 7L output voltage, ***(b)*** Filtered output voltage



a



b

Fig. 13 *Experimental results of clamped capacitor voltage*
(a) Scale of 0.02 s, ***(b)*** Scale of 50 µs

THD of the 7L waveform and filtered output voltage are 24.06 and 0.53%, respectively. Also, the clamped capacitor voltage is approximately balanced at 125 V with ripple of 1.28%. Simulation and experimental results verified the feasibility of the proposed 7L inverter and its modulation method.

7 Acknowledgment

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