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A FIVE-LEVEL CASCADE MULTILEVEL INVERTER THREE-PHASE MOTOR DRIVE USING A SINGLE DC SOURCE

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ORNL Subcontractor with
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A Five-Level Cascade Multilevel Inverter Three-Phase Motor Drive Using a Single DC Source

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Abstract

A method is presented showing that a 5-level cascade multilevel inverter for a three-phase permanent magnet sychronous motor drive can be implemented using only a single DC link to supply a standard 3-leg inverter along with three full H-bridges supplied by capacitors.

It is shown that the capacitor voltages can be regulated while achieving an output voltage waveform that is 20% greater than that obained using the standard 3-leg inverter alone.

Finally conditions are given in terms of the power factor and modulation index that determine when the capacitor voltage can regulated.

1 Introduction

A cascade multilevel inverter is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Such inverters have been the subject of research in the last several years [1][2][3][4], where the DC levels were considered to be identical in that all of them were either batteries, solar cells, etc. In [5], a multilevel converter was presented in which the two separate DC sources were the secondaries of two transformers coupled to the utility AC power. Corzine et al [6] have proposed using a single DC power source and capacitors for the other DC sources. A method was given to transfer power from the DC power source to the capacitor in order to regulate the capacitor voltage. A similar approach was later (but independently) proposed by Du

et al [7]. These approaches required a DC power source for each phase. Similar methods have also been proposed by Veenstar and Rufer [8][9]. The approach here is very similar to that of Corzine et al [6] and Du et al [7] with the important exception that only a single standard 3-leg inverter is required as the power source (one leg for each phase) for the three phase multilevel inverter. This topology was proposed by Özpineci [10].

Specifically, the interest here is in using a single DC power source connected to a standard 3-leg inverter which in turn is connected to capacitors to form a 3-phase 5-level cascade multilevel inverter to be used as a drive for a PM traction motor. The 5-level inverter consists of a standard 3-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg and using a capacitor as a DC source. It is shown that one can simultaneously maintain the regulation of the capacitor voltage while achieving an output voltage waveform which is 25% higher than that obtained using a standard 3-leg inverter by itself.

2 Multilevel Inverter Architecture

Figure 1 shows a DC source connected to a single leg of a standard 3-leg inverter.

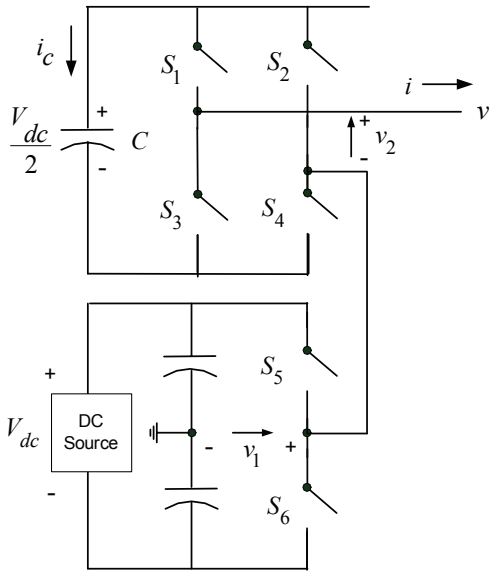

Figure 1: One leg of a 3-leg inverter connected to a full H-bridge with a capacitor DC source.

The output voltage v_1 of this leg (with respect to the ground) is either $+V_{dc}/2$ (S_5 closed) or $-V_{dc}/2$ (S_6 closed). This leg is connected in series with a full H-bridge which in turn is supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S_1&S_4 closed), 0 (S_1&S_2 closed or S_3&S_4 closed), or $-V_{dc}/2$ (S_2&S_3

closed). An example output waveform that this topology can achieve is shown in Figure 2.

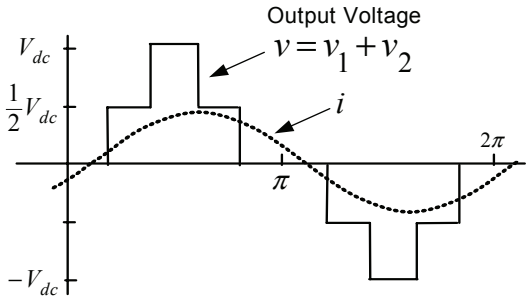

Figure 2: Five-level output waveform of the multilevel inverter.

When the output voltage $v = v_1 + v_2$ is required to be zero, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ or $v_1 = +V_{dc}/2$ and $v_2 = +V_{dc}/2$. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage. In more detail, consider Figure 3.

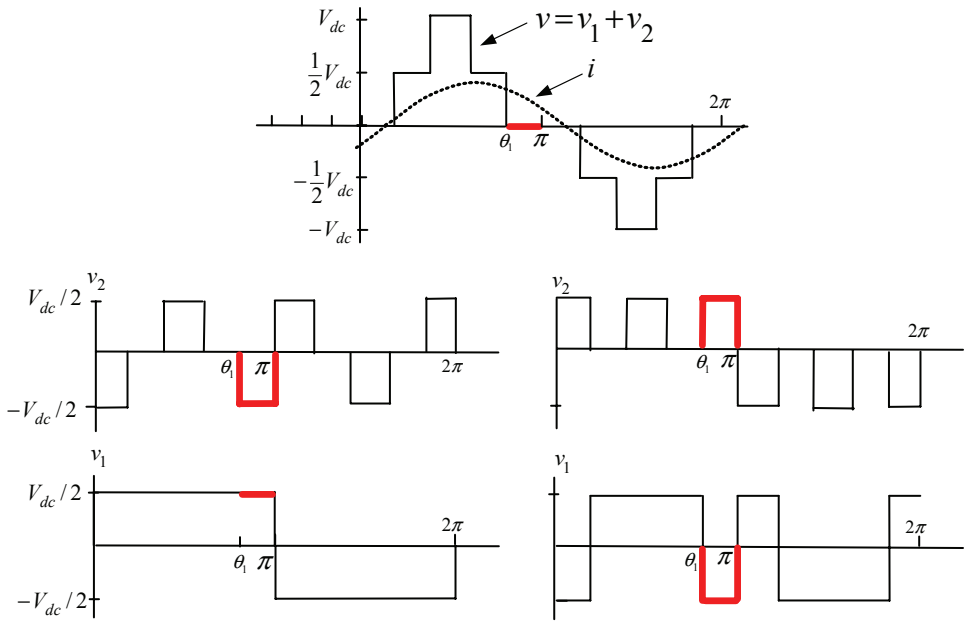

Figure 3: To make the output voltage zero for $\theta_1 \leq \theta \leq \pi$, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ (bottom left) or $v_1 = +V_{dc}/2$ and $v_2 = +V_{dc}/2$ (bottom right).

In the interval $\theta_1 \leq \theta \leq \pi$, the output voltage in Figure 3 is zero and the current $i > 0$. If $S_1\&S_4$ are closed (so that $v_2 = +V_{dc}/2$) along with S_6 closed (so that $v_1 = +V_{dc}$), then the capacitor is *discharging* ($i_c = -i < 0$ see Figure 1) and $v = v_1 + v_2 = 0$. On the other hand, if $S_2\&S_3$ are closed

(so that $v_2 = -V_{dc}/2$) and S_5 is also closed (so that $v_1 = -V_{dc}/2$), then the capacitor is *charging* ($i_c = i > 0$ see Figure 1) and $v = v_1 + v_2 = 0$.

The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charge and discharge of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, and S_5 are closed depending on whether it is necessary to charge or discharge the capacitor.

Remark

As Figure 3 illustrates, this method of regulating the capacitor voltage depends on the voltage and current not being in phase. That is, one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the ability to regulate the capacitor voltage depends on the power factor.

3 Simulation Results Using Multilevel PWM

A simulation of the multilevel converter driving a PM synchronous machine was carried out. The basic block diagram for the simulation is shown in Figure 4

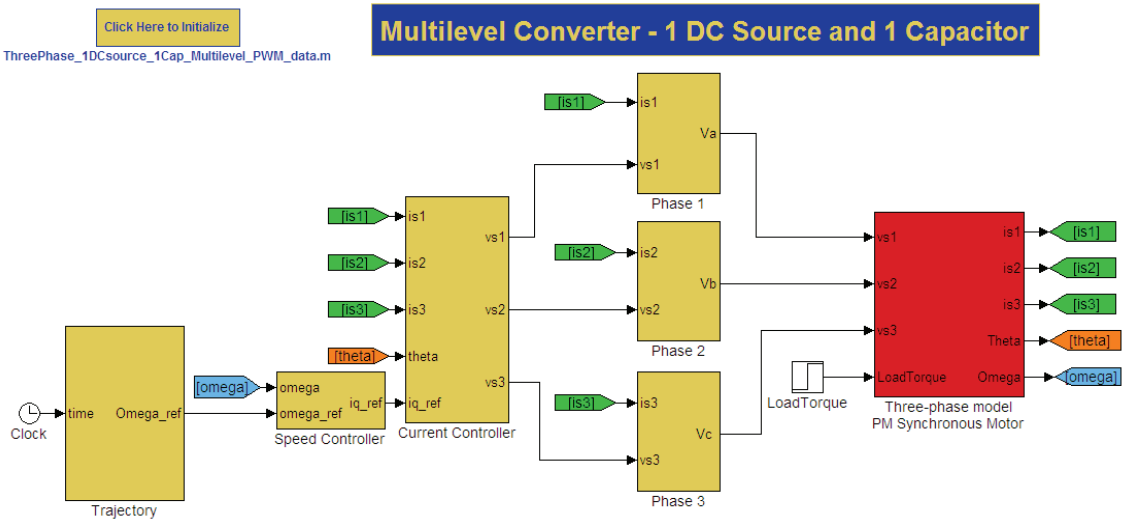

Figure 4: Top level Simulink block diagram.

The motor is controlled using a standard field-oriented controller [11]. The blocks marked phase 1, phase 2, and phase 3 contain the modeling of the multilevel converter. The switching scheme is based on the standard multilevel pwm scheme [12]. The scheme is modified so that during those time periods when the multilevel inverter has an output of zero volts, either the switches S_1, S_4, and

S_6 are closed or the switches S_2, S_3, and S_5 are closed depending on whether the current is positive or negative and whether it is necessary to charge or discharge the capacitor.

The DC link voltage V_{dc} was set to 200 V so that the 3-leg inverter supplies ± 100 V. The capacitors were regulated to 100 V. The motor's inertia is $J = 0.1$ kg-m^2, the motor has $n_p = 4$ pole-pairs, the stator resistance is $R_S = 0.065$ Ohms, the stator inductance is $L_S = 3$ mH, the torque/back-emf constant $K_T = K_b = 0.37$ Nm/A (V/rad/sec) and the load torque $\tau_L = 19$ Nm. The capacitor value is $C = 0.01$ F.

For comparison purposes, simulations were performed using both the multilevel inverter of Figure 1 capable of supplying up to ± 200 V and a standard 3-leg inverter (i.e., only the bottom half of Figure 1) capable supplying ± 100 V. Though the multilevel inverter can supply up to ± 200 V, it cannot do this and maintain regulation of the capacitor voltages. As pointed out in the above remark, the ability to regulate the capacitor voltage depends on the power factor of the load. The PM motor was run to achieve the highest possible speed under the given load and available voltage. This is shown in Figure 5. The standard 3-leg inverter could only achieve a maximum speed of 212 rad/sec while the proposed multilevel inverter could get the motor up to 275 rad/sec using the same DC source voltage.

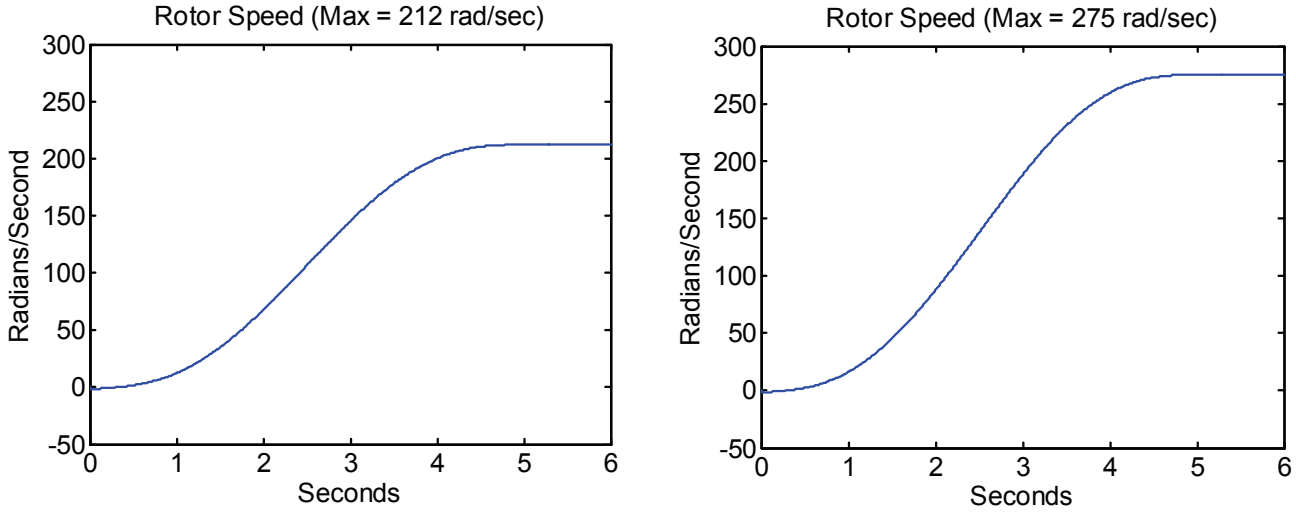

Figure 5: Rotor speeds achievable using a standard 3-leg inverter (left) and the proposed multilevel inverter (right).

The corresponding voltages for the speed trajectories of Figure 5 are shown in Figure 6. The standard 3-leg inverter is supplying a nearly six step wave form of $V_{dc}/2 = 100$ V maximum corresponding to a fundamental voltage of $(4/\pi)V_{dc}/2 = 127$ V peak while the multilevel inverter is outputting 170 V peak in steady state and up to 180 V before steady state.

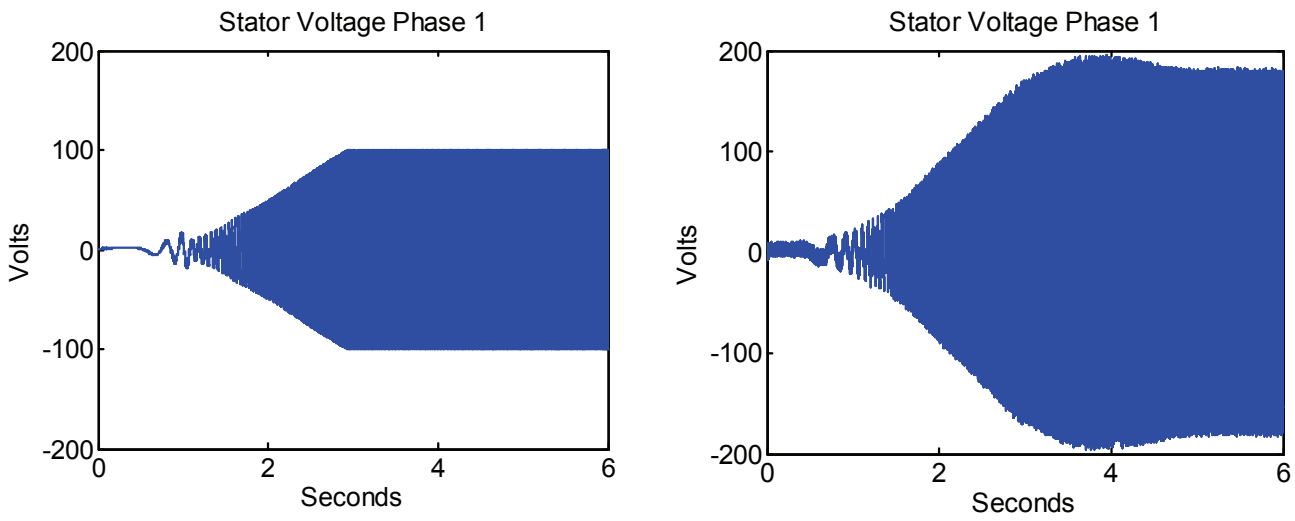

Figure 6: Left: Voltage using a standard 3-leg inverter. Right: Voltage obtained using the proposed multilevel inverter.

The corresponding torques for the above trajectories shown in Figure 7. The chattering shown in the torque response of the standard 3-leg inverter is due to the fact that the voltage is undergoing saturation (see the left-side of Figure 6).

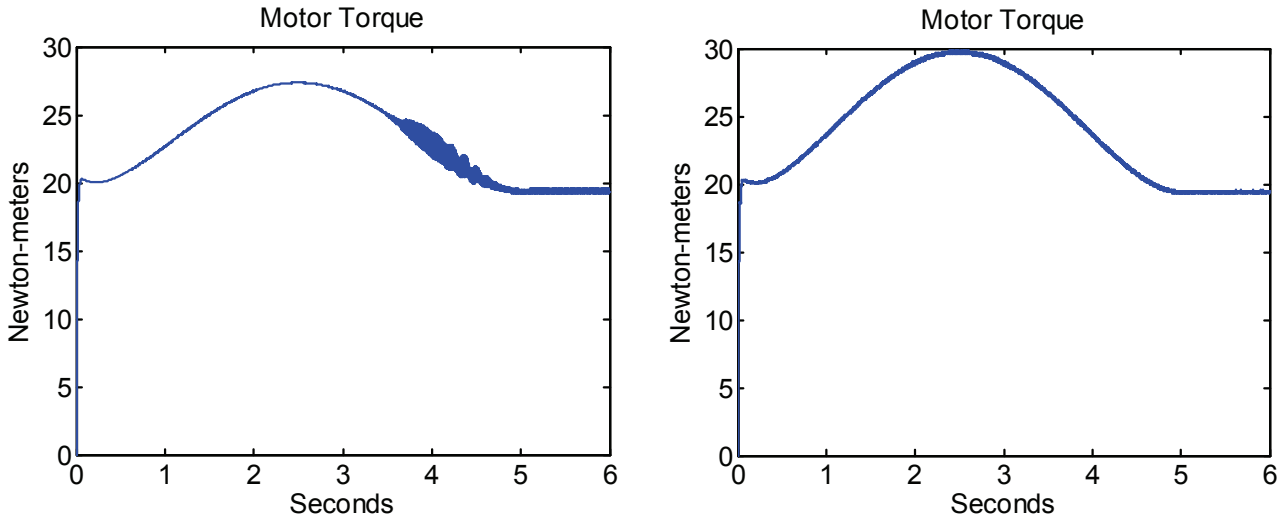

Figure 7: Left: Motor torque using standard 3-leg inverter. Right: Motor torque using proposed multilevel inverter.

The stator currents are shown in Figure 8. The current used in the multilevel inverter is higher because it requires more torque to accelerate the motor to its higher speed (see Figure 5).

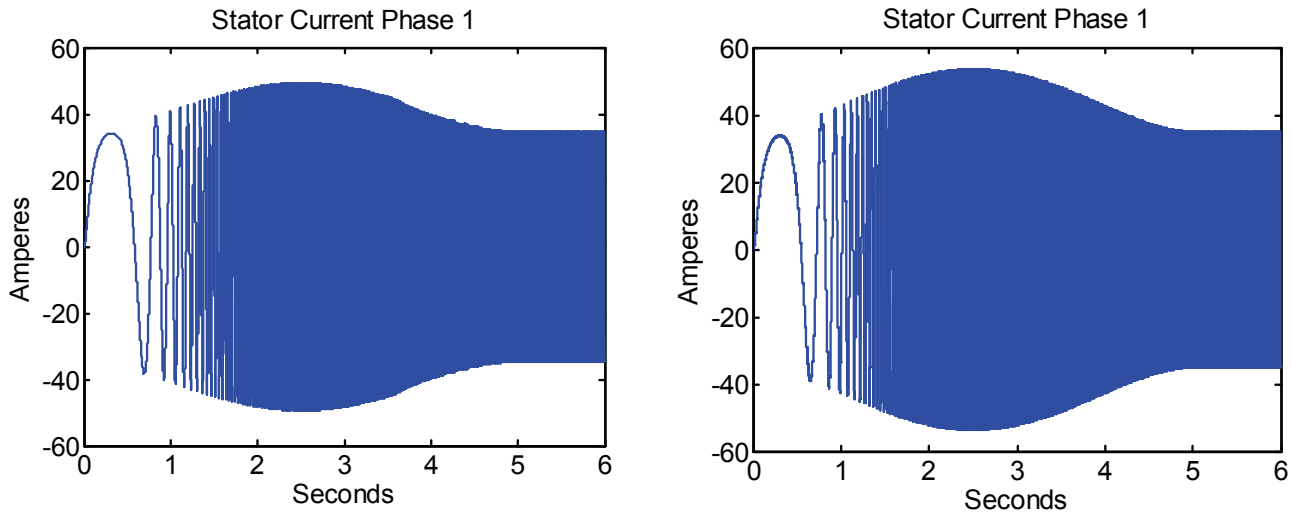

Figure 8: Left: Stator current for the standard 3-leg inverter. Right: Stator current for the proposed multilevel inverter.

The capacitor voltage as a function of time is plotted in Figure 9 showing that it is kept within about 2 volts of the desired value.

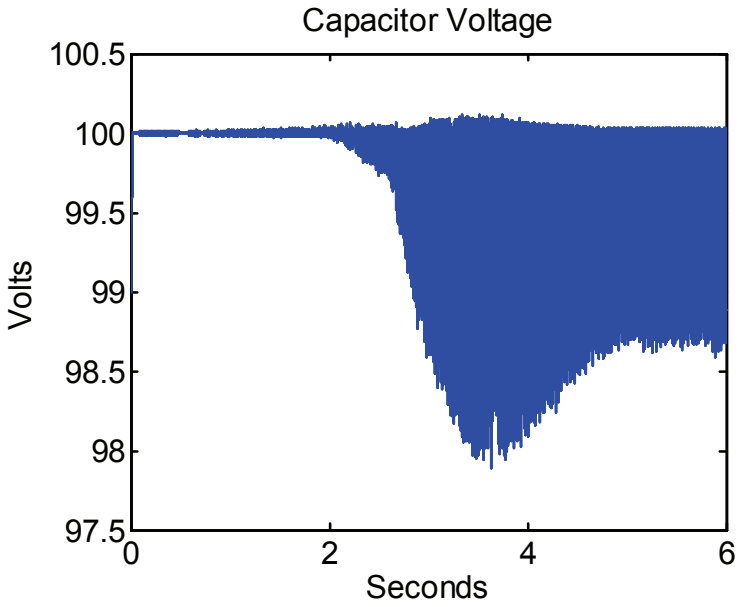

Figure 9: Capacitor voltage versus time.

An enlarged view of the capacitor voltage is shown in Figure 10 showing the regulation of the voltage in more detail. The variation in the voltage will be less if a larger value of capacitance is used ($C = 0.01$ F in the simulation).

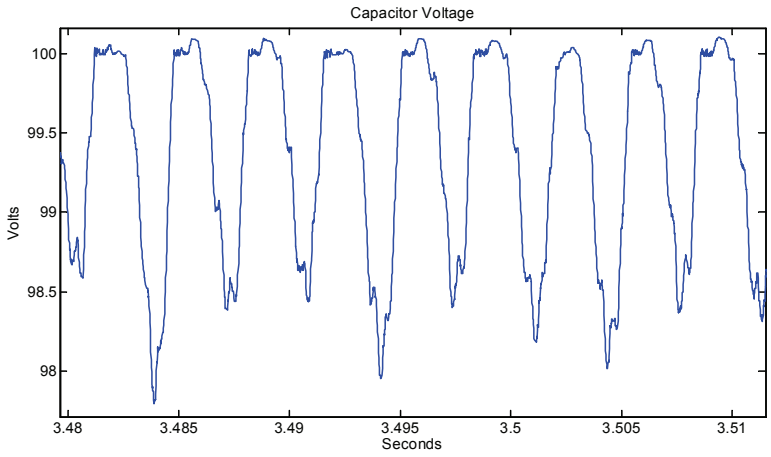

Figure 10: Expanded view of the capacitor voltage as a function of time.

To illustrate how the capacitor voltage regulation works, scaled versions of the capacitor voltage, stator voltage, and stator current for phase 1 are shown in Figure 11.

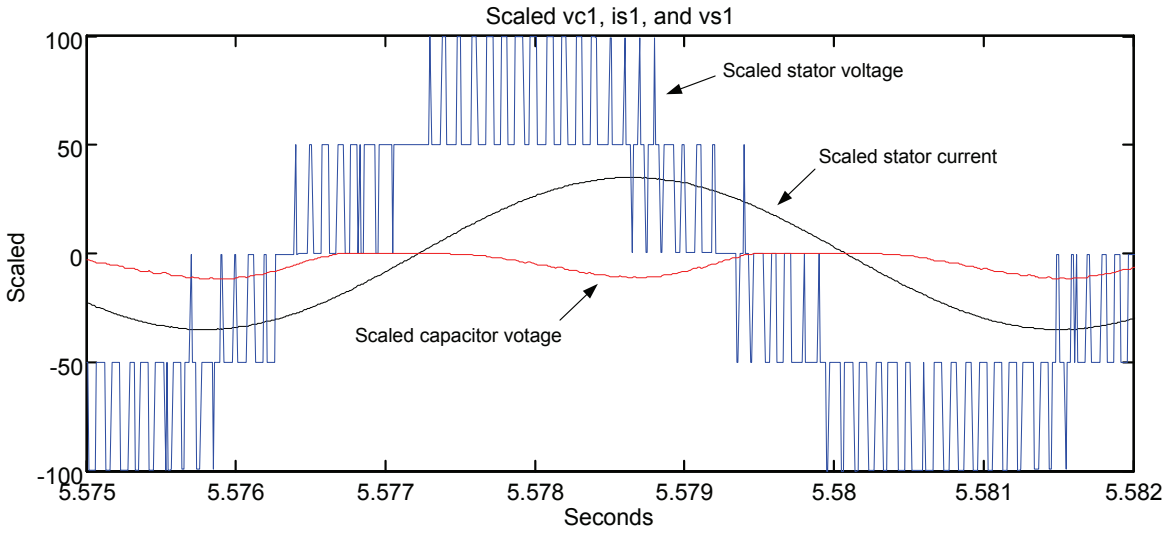

Figure 11: Scaled versions of the capacitor voltage, phase voltage, and phase current.

Note that the capacitor voltage decreases during those times the inverter is supplying ± 100 V is constant during those times the inverter is supplying ± 50 V, and is increasing (recharging) during those times the inverter is supplying 0 V. For example, a little after $t = 5.577$ seconds, the current becomes positive and the inverter is required to put out (up to) 200 V (only 100 in the figure due to the scaling) by the pwm scheme. The capacitor voltage (red) then decreases. Then shortly before $t = 5.579$ seconds, the inverter is only required to supply up to 100 V (only 50 in the figure due

to the scaling) and the capacitor voltage is constant. At about $t = 5.579$ seconds, the multilevel pwm scheme is having the inverter supply 0 V for significant time intervals so that capacitor voltage increases.

4 Simulation Results - Fundamental Frequency Switching

In this section a fundamental frequency switching scheme is used. By fundamental frequency switching, it is meant that each device switches once per cycle in contrast to a pwm scheme for which each device turns on and off several times a cycle (see Figure 11). Typically a fundamental switching scheme results in a higher harmonic content in the lower frequency spectrum (closer to the fundamental) than a pwm method, but has lower switching losses. In the 5-level multilevel inverter under consideration here, a fundamental switching scheme is implemented by choosing two angles θ_1 and θ_2 for when the devices are to be switched on as indicated in Figure 12. By symmetry of the waveform, the rest of the switchings occur at $\pi - \theta_1, \pi - \theta_2, \pi + \theta_1, \pi + \theta_2, 2\pi - \theta_1, 2\pi - \theta_2$.

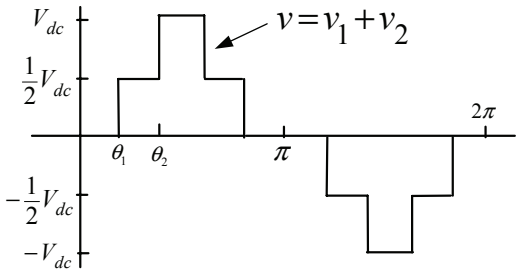

Figure 12: Fundamental frequency waveform.

With the nominal capacitor voltage chosen as $V_{dc}/2$, one computes the switching angles θ_1 and θ_2 as in [13][14]. Briefly, the Fourier series expansion of the (staircase) output voltage waveform of the multilevel inverter as shown in Figure 12 is

$$V(\omega t) = \frac{4}{\pi}\frac{V_{dc}}{2} \times \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n}\Big(\cos(n\theta_1) + \cos(n\theta_2)\Big)\sin(n\omega t). \tag{1}$$

Ideally, given a desired fundamental voltage V_1, one wants to determine the switching angles θ_1 and θ_2 so that (1) becomes $V(\omega t) = V_1 \sin(\omega t)$. In practice, one is left with trying to do this approximately. For three-phase systems, the triplen harmonics in each phase need not be canceled as they automatically cancel in the line-to-line voltages. In this case, where there are 2 DC sources, the desire is to cancel the 5^{th} order harmonic as it tends to dominate the total harmonic distortion.

The mathematical statement of these conditions is then

$$\begin{aligned} \cos(\theta_1) + \cos(\theta_2) &= m \triangleq \frac{V_1}{\frac{4}{\pi}\frac{V_{dc}}{2}} \\ \cos(5\theta_1) + \cos(5\theta_2) &= 0 \end{aligned} \tag{2}$$

This is a system of two transcendental equations in the two unknowns θ_1 and θ_2. There are many ways one can solve for the angles (see, for example, [15], [16], and [17]). Here the approach in [13] and [18] is used. It is found that a solution to (2) exists for $0.6 \leq m \leq 1.909$ and these solution angles are plotted in Figure 13. Note that the fundamental is given by

$$V_1 = m\frac{4}{\pi}\frac{V_{dc}}{2}. \tag{3}$$

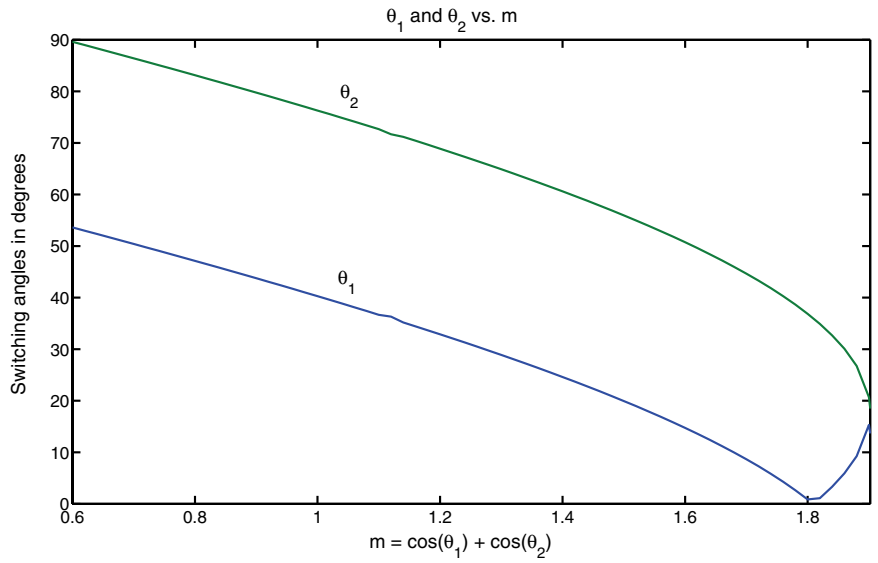

Figure 13: θ_1 and θ_2 versus m.

In the simulations presented here, the same PM motor as chosen for the multilevel pwm scheme was used, but the motor was driven open-loop rather than closed-loop. The voltage magnitude was ramped from 90 V to 180 V during the time interval from 0 to 3 seconds. The stator electrical frequency f_S was brought up smoothly from 0 to 175 Hz in 5 seconds resulting in a peak speed of $2\pi f_S/n_p = 275$ rad/sec. This is the same speed trajectory as used in the closed-loop multilevel pwm implementation above. The resulting speed response is shown in Figure 14, which is somewhat

oscillatory due to the open-loop control. Because it is driven open loop, it is much more difficult to have the machine go up in speed with a significant load torque at the start. As a result, only a viscous friction load torque was used with the viscous friction coefficient chosen as $f = 0.07$ so that at maximum speed the load torque is $f\omega_{\max} = f(2\pi f_S/n_p) = 0.07 * 275 = 19$ Nm giving the same steady-state load-torque as in the multilevel pwm case.

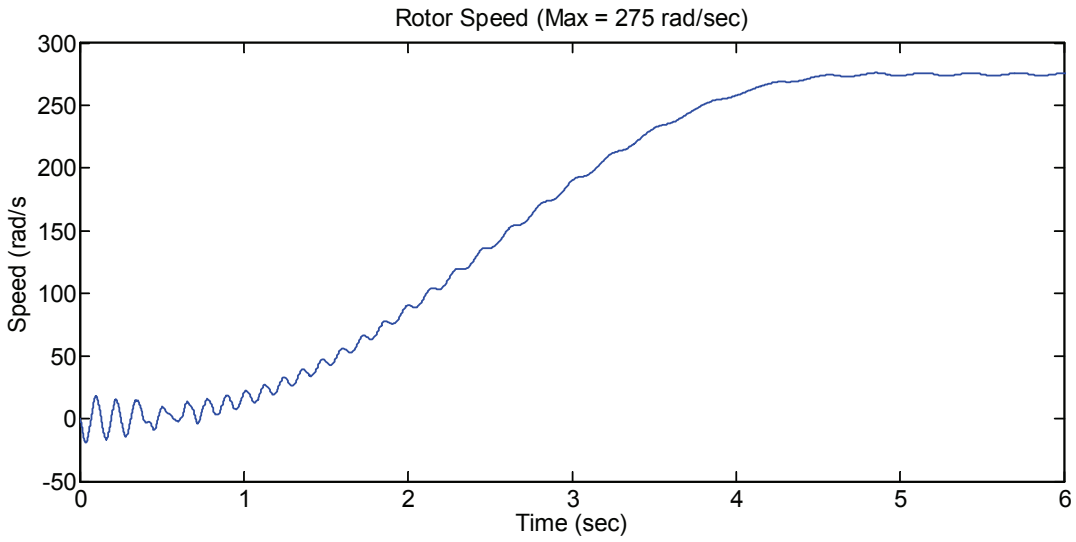

Figure 14: Rotor speed in rad/sec versus time in seconds.

The commanded voltage magnitude [see (3)] and the computed fundamental of the inverter output are given in Figure 15.

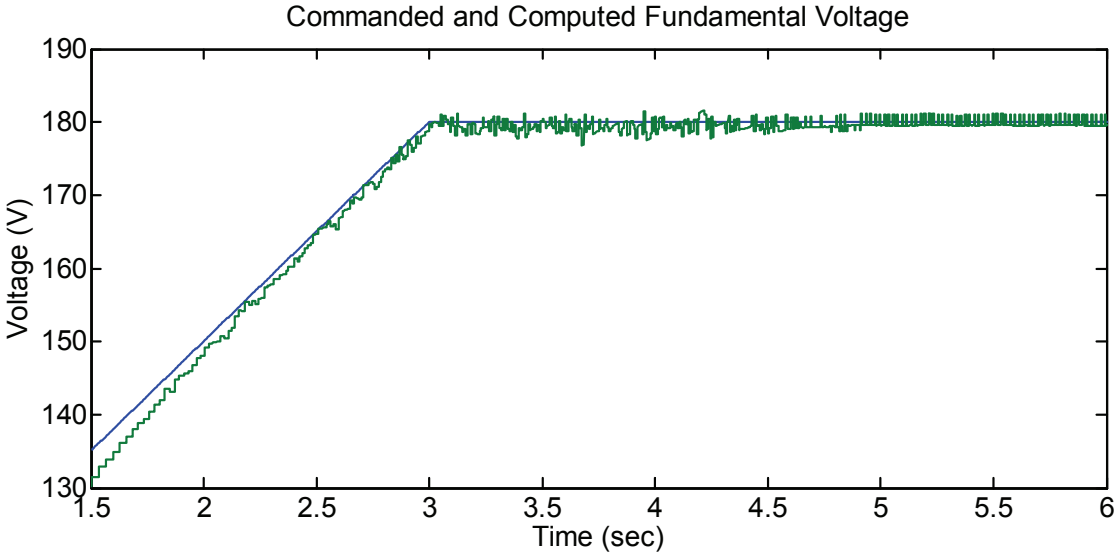

Figure 15: Commanded and computed fundamental voltage in Volts versus time in seconds.

The computed fifth harmonic of the voltage is plotted versus time in Figure 16. During the end of the run when the speed is close to being constant, the fifth-harmonic is about 0.7 V compared to the 180 V of the fundamental.

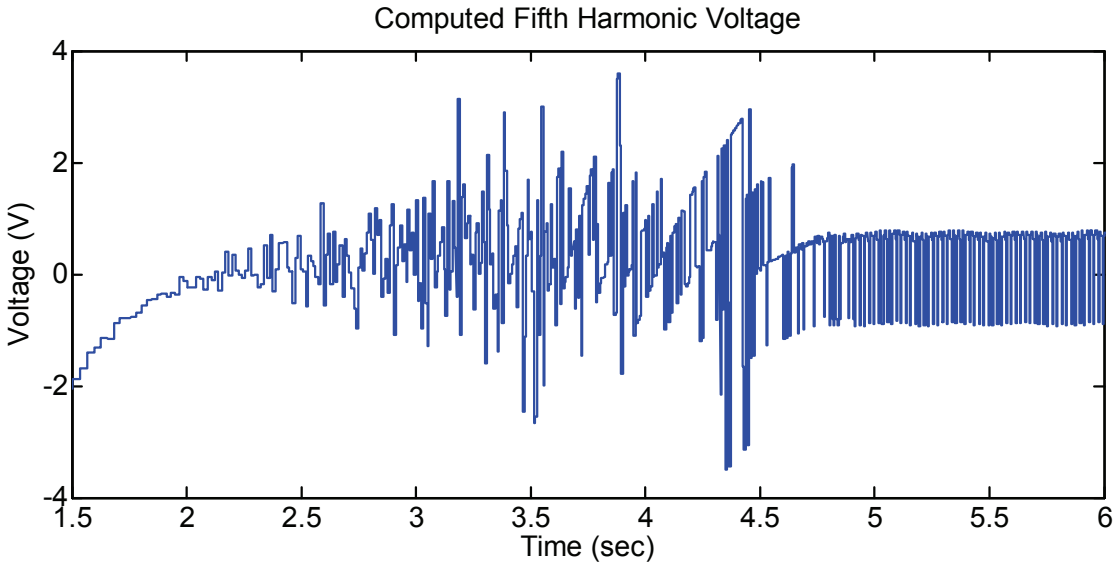

Figure 16: Computed fifth-harmonic of the voltage in volts versus time in seconds.

The motor torque is shown in Figure 17, which as explained above, is oscillatory due to the open-loop control. Note that at the end of the run, the torque is oscillating about 19 Nm to counteract the (viscous-friction) load torque.

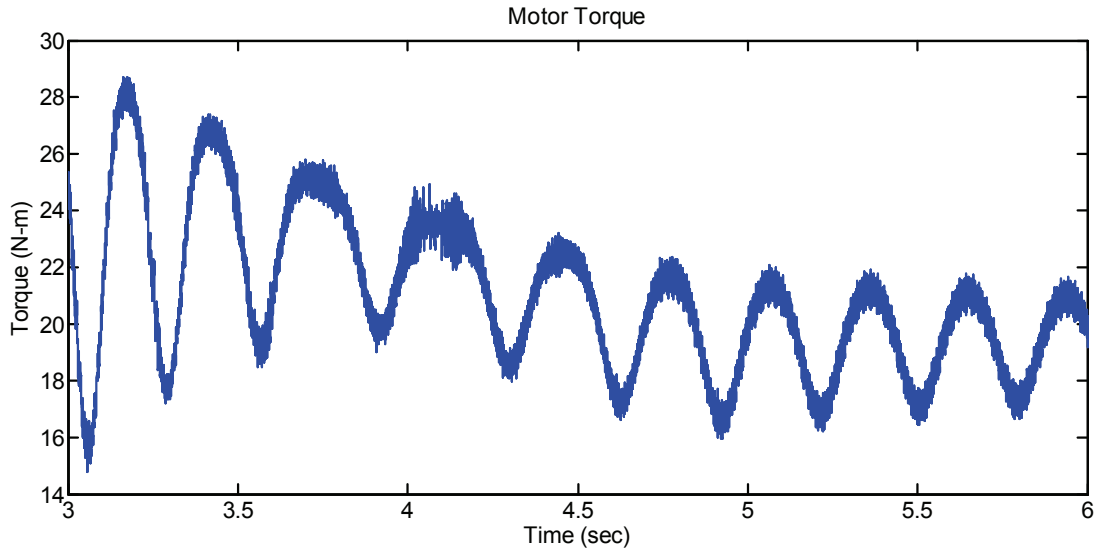

Figure 17: Torque in N-m versus time in seconds.

An enlarged section of the inverter output voltage of phase 1 is given in Figure 18 and shows the fundamental switching scheme for a stator frequency of $f_S = 175$ Hz.

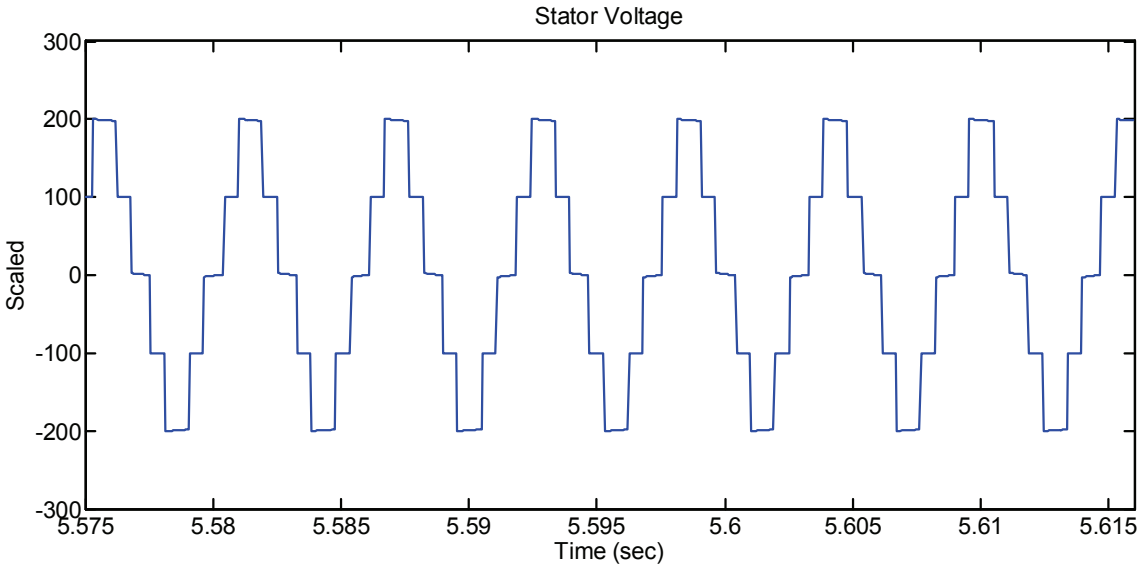

Figure 18: Enlarged view of the phase 1 voltage in Volts versus time in seconds.

The stator current response of phase 1 is plotted in Figure 19 and uses somewhat more current than the closed-loop pwm scheme (see Figure 8).

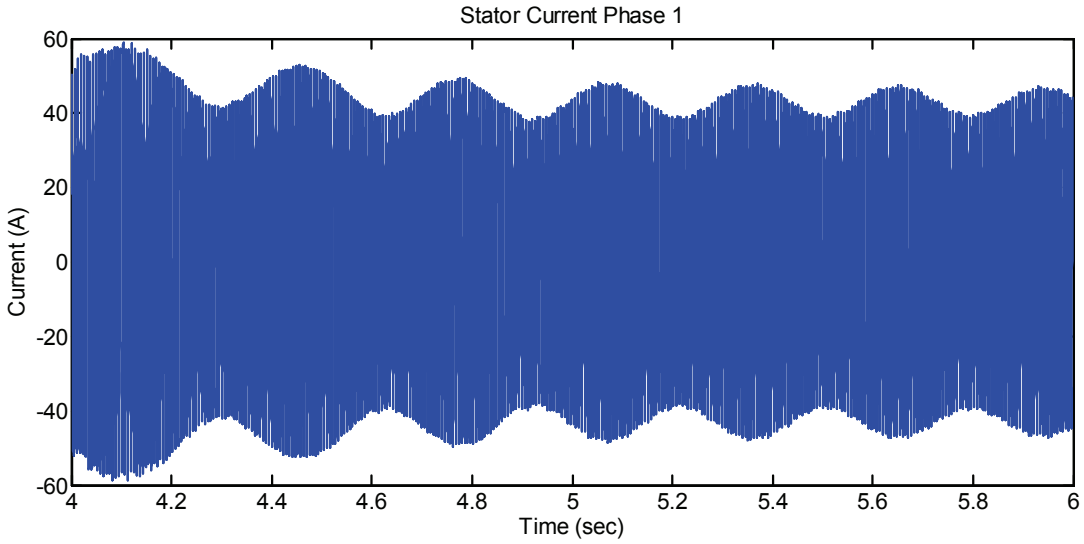

Figure 19: Phase 1 stator current versus time.

The capacitor voltage is shown in Figure 20 showing that the scheme regulates the voltage within

3 volts of the nominal value. The value of the capacitance is $C = 0.01$ F as in the multilevel pwm case. An enlarged view of the capacitor voltage for $5.5 \leq t \leq 5.525$ is shown in Figure 21.

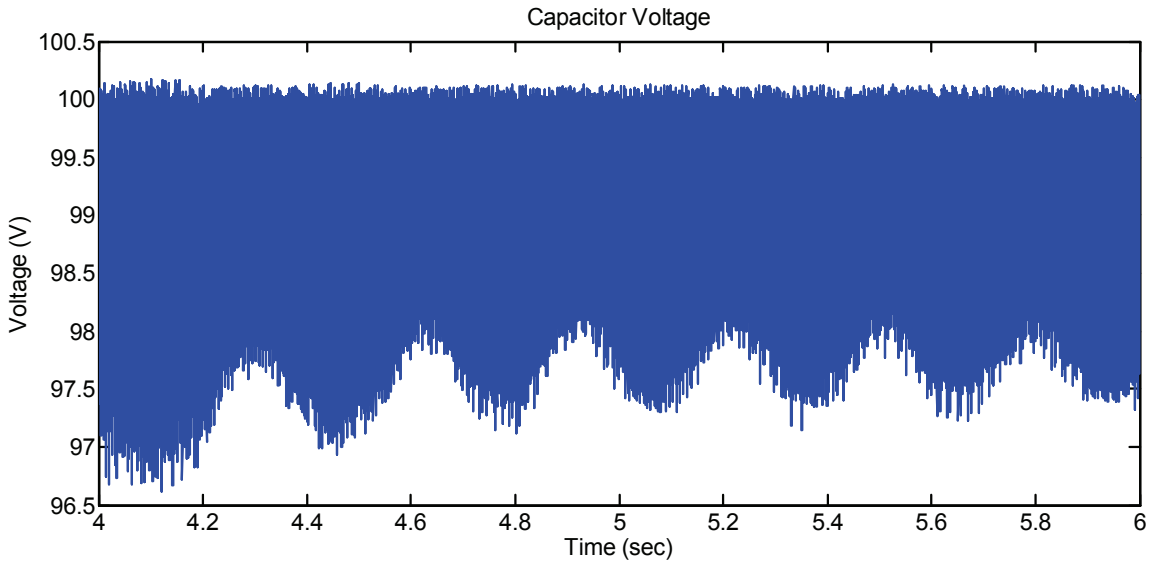

Figure 20: Capacitor voltage in volts versus time in seconds.

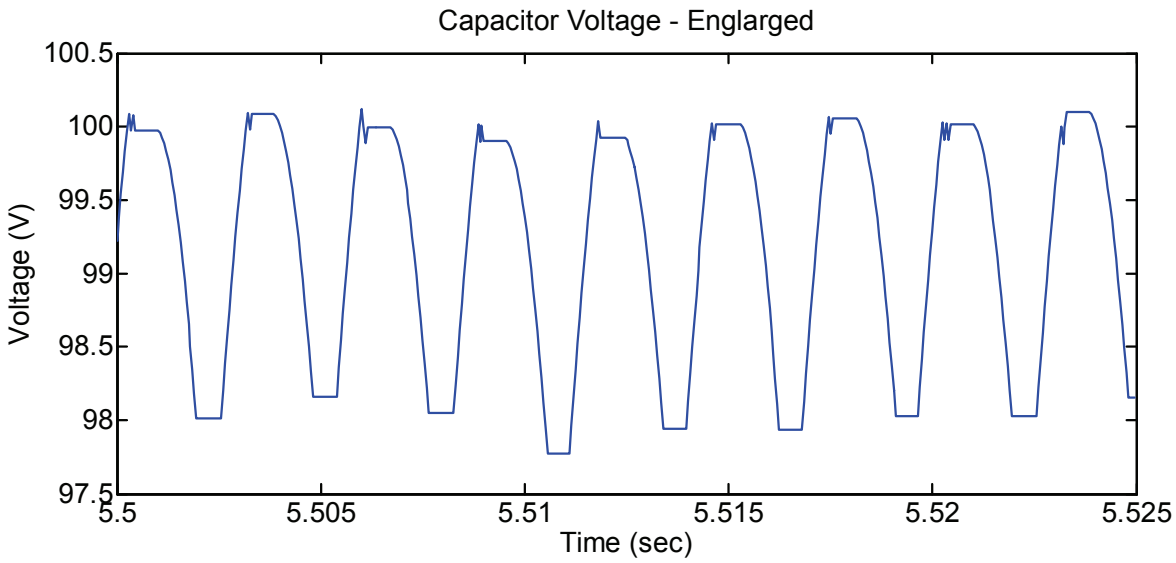

Figure 21: An enlarged view the capacitor voltage in Volts versus time in seconds.

Scaled versions of the capacitor voltage, stator current, and stator voltage versus time are shown in Figure 22. Note that the capacitor discharges when the inverter is supplying ± 200 V, stays constant when the inverter is supplying ± 100 V, and recharges when the inverter is supplying 0 V.

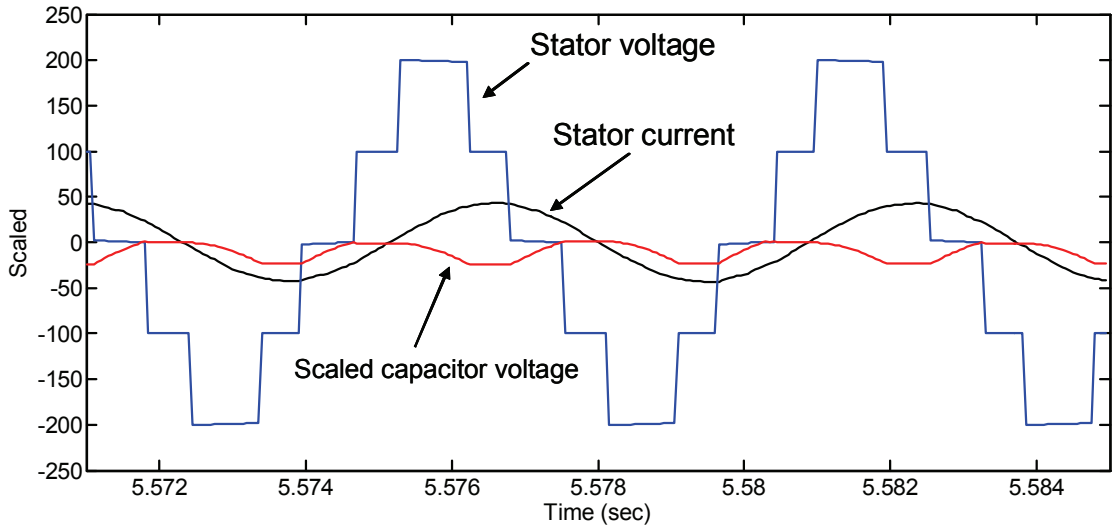

Figure 22: Scaled capacitor voltage, stator current, and stator voltage versus time in seconds.

For example, a little after $t = 5.575$ seconds, the stator current becomes positive and the inverter is required to supply 200 V. The capacitor voltage then decreases. Following this, when the inverter is only required to supply 100 V, the capacitor voltage is constant. Next, the inverter is putting out 0 V so that capacitor is charging and its voltage increases.

5 Conditions for Capacitor Voltage Regulation

Let

$$\begin{aligned} v_f(\theta) &= V\sin(\theta) \\ i(\theta) &= I\sin(\theta-\varphi) \end{aligned}$$

where $v_f(\theta)$ is the fundamental component of the voltage, $i(\theta)$ is the current, and φ is the power factor angle. The objective here is to compute the conditions on θ_1, θ_2, and φ to ensure the capacitor can be regulated to a desired value.

5.1 $0 < \varphi < \theta_1$

Consider the case where $0 < \varphi < \theta_1$ as illustrated in Figure 23. During the interval $\theta_2 < \theta < \pi - \theta_2$, the capacitor loses the amount of charge $\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta$ while during the intervals $0 < \theta < \theta_1$ and $\pi - \theta_1 < \theta < \pi$ the capacitor can be recharged (by choosing the switch positions appropriately) by the amounts $\int_0^{\varphi} I\left|\sin(\theta-\varphi)\right| d\theta + \int_{\varphi}^{\theta_1} I\sin(\theta-\varphi)d\theta$ and $\int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta$, respectively.

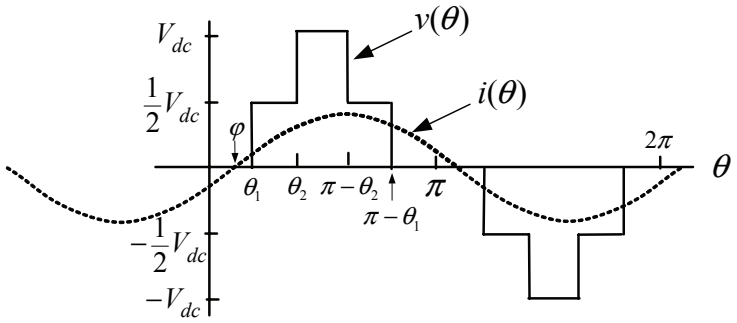

Figure 23: $0 < \varphi < \theta_1$

In this case, keeping the capacitor charged requires

$$\begin{aligned} \int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta &< \int_0^{\varphi} I\left|\sin(\theta-\varphi)\right| d\theta + \int_{\varphi}^{\theta_1} I\sin(\theta-\varphi)d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta \\ I\cos(\theta_2+\varphi) + I\cos(\theta_2-\varphi) &< (I\cos(0) - I\cos(\varphi)) + (-I\cos(\theta_1-\varphi) + I\cos(0)) + \\ &\quad (I\cos(\varphi) - I\cos(\theta_1+\varphi)) \\ \cos(\theta_2)\cos(\varphi) &< \cos(0) - \cos(\theta_1)\cos(\varphi) \end{aligned}$$

or finally, the condition in this case is

$$\cos(\varphi) < \frac{1}{\cos(\theta_1) + \cos(\theta_2)} \tag{4}$$

5.2 $\theta_1 < \varphi < \theta_2$

Consider the case $\theta_1 < \varphi < \theta_2$ as in Figure 24. During the interval $\theta_2 < \theta < \pi - \theta_2$, the capacitor loses the amount of charge $\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta$ while during the intervals $0 < \theta < \theta_1$ and $\pi - \theta_1 < \theta < \pi$ the capacitor can be recharged (by choosing the switch positions appropriately) by the amount $\int_0^{\theta_1} I\left|\sin(\theta-\varphi)\right| d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta$.

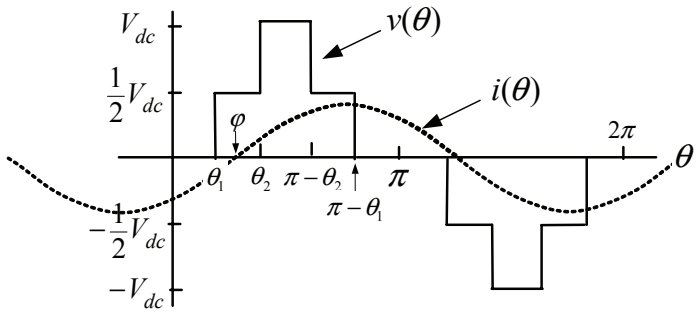

Figure 24: $\theta_1 < \varphi < \theta_2$

Thus keeping the capacitor voltage regulated requires

$$\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta < \int_0^{\theta_1} I\left|\sin(\theta-\varphi)\right| d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta$$

Expanding

$$\begin{aligned} I\cos(\theta_2+\varphi) + I\cos(\theta_2-\varphi) &< (I\cos(\theta_1-\varphi) - I\cos(\varphi)) + (I\cos(\varphi) - I\cos(\theta_1-\varphi)) \\ 2I\cos(\theta_2)\cos(\varphi) &< 2I\sin(\theta_1)\sin(\varphi) \end{aligned}$$

or finally, the condition is

$$\frac{\cos(\theta_2)}{\sin(\theta_1)} < \tan(\varphi). \tag{5}$$

5.3 $\theta_2 < \varphi < \pi/2$

Finally, consider the case where $\theta_2 < \varphi < \pi/2$ as shown in Figure 25. During the subinterval $\theta_2 < \theta < \varphi$ the capacitor is being charged as the current is negative while it is discharging in subinterval $\varphi < \theta < \pi - \theta_2$. Thus the total discharge in the interval $\theta_2 < \theta < \pi - \theta_2$ is $\int_{\theta_2}^{\pi-\theta_2} I \sin(\theta - \varphi) d\theta$.

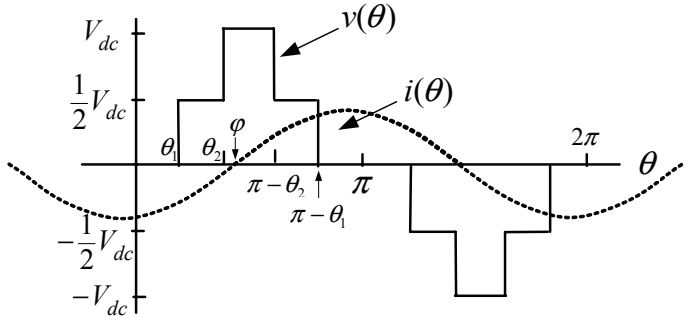

Figure 25: $\theta_2 < \varphi < \pi/2$

Thus keeping the capacitor voltage regulated requires

$$\int_{\theta_2}^{\pi-\theta_2} I \sin(\theta - \varphi) d\theta < \int_0^{\theta_1} I \left|\sin(\theta - \varphi)\right| d\theta + \int_{\pi-\theta_1}^{\pi} I \sin(\theta - \varphi) d\theta$$

Expanding

$$\begin{aligned} I\cos(\theta_2 + \varphi) + I\cos(\theta_2 - \varphi) &< (I\cos(\theta_1 - \varphi) - I\cos(\varphi)) + (I\cos(\varphi) - I\cos(\theta_1 + \varphi)) \\ 2I\cos(\theta_2)\cos(\varphi) &< 2I\sin(\theta_1)\sin(\varphi) \end{aligned}$$

or finally, the condition is

$$\frac{\cos(\theta_2)}{\sin(\theta_1)} < \tan(\varphi) \tag{6}$$

which has the same form as the previous case.

5.4 Capacitor voltage regulation as a function of m and φ.

In summary, the conditions for capacitor voltage regulation in terms of θ_1, θ_2, and φ are

$$\begin{aligned} &0 < \varphi < \theta_1 \qquad \cos(\varphi) < \frac{1}{\cos(\theta_1) + \cos(\theta_2)} = \frac{1}{m} \\ &\theta_1 < \varphi < \pi/2 \qquad \frac{\cos(\theta_2)}{\sin(\theta_1)} < \tan(\varphi). \end{aligned} \tag{7}$$

Notice at the boundary of the two conditions where $\varphi = \theta_1$, the two conditions are identical. These conditions can be rewritten as

$$\begin{aligned} &0 < \varphi < \theta_1 \qquad \varphi > \cos^{-1}(1/m) \\ &\theta_1 < \varphi < \pi/2 \qquad \varphi > \tan^{-1}\left(\frac{\cos(\theta_2)}{\sin(\theta_1)}\right). \end{aligned} \tag{8}$$

Figure 13 is a plot of θ_1 and θ_2 in degrees versus m (the modulation index is $m/2$). For any given value of m and φ, the values of θ_1 and θ_2 are found via Figure 13 and thus whether or not the capacitor voltage can be regulated is straightforwardly checked using the conditions (7). What these conditions say is, for any given value of m in the interval $0.6 \leq m \leq 1.909$ (i.e., where conditions (2) have a solution), the capacitor voltage can be regulated provided the power factor angle is large enough.

6 Conclusions

A cascade multilevel inverter topology has been proposed that requires only a single standard 3-leg inverter and capacitors as the power sources. The capacitors obtain their power from the 3-leg inverter allowing the cascade multilevel inverter to put out significantly more voltage from a given DC power source than just a three leg inverter alone. Both multilevel pwm and fundamental frequency switching schemes were considered. Finally, subject to conditions in terms of the power factor and modulation index ($= m/2$), it was shown that the capacitor voltages could be regulated.

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