

Universal Converter Using Silicon Carbide

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**Dallas Marckx (Principal Investigator)
Brian Ratliff
Matthew Jones**

**Peregrine Power LLC
27350 SW 95th Avenue, Suite 3030
Wilsonville, OR 97070
503.682.7001
503.682.6014 fax
dmarckx@peregrinepower.com**

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1 EXECUTIVE SUMMARY

In this project, Peregrine Power LLC (Peregrine) began developing a high power (one MW or more) converter with silicon carbide devices for use in a variety of distributed and alternative energy systems, such as wind turbines, and fuel and photovoltaic cells. Due to the high rating, medium voltage is highly recommended to reduce current in all current carrying components, thus dramatically reducing size and eventually cost. Peregrine has targeted 4,160VAC as the ultimate operating voltage, requiring power devices rated at over 10,000V. This is enabled by the use of SiC. The use of SiC devices leads to lower losses, higher temperature and higher switching speed, which in turn lead to smaller size and cost.

In Phase I, the Peregrine team addressed certain issues that stand in the way of a successful outcome. Two of the primary issues are the degradation of SiC device performance at elevated temperature and the need for high temperature packaging. Many promoters of SiC devices promise tremendous size reductions due to the high temperature capability of some SiC devices, but they generally do not account for the increase in conduction losses at higher temperature, which tends to offset the higher temperature benefits. The degree of this offset is important in selecting the best devices and best operating temperature for the project's applications. As a practical matter, the precise determination of losses at elevated temperature was necessary before the Peregrine team could proceed to complete the inverter design.

The Peregrine team obtained and tested a variety of SiC power devices in Phase I to determine their static and dynamic characteristics over a spectrum of temperatures from room temperature to 300°C. This data was used to predict the size and performance of a SiC-based inverter for the multi-MW applications. The results of Phase I continue to show that significant improvements can be made by using SiC devices, but the precise selection of devices will be a function of the application. The three primary variables in an application which dictate the appropriate type of SiC device are voltage, temperature and switching frequency. In Phase I, all of these variables were increased substantially in an inverter using SiC BJTs with the result that a reduction in weight of material is projected to exceed a factor of six compared to an inverter using standard silicon devices.

On the date of this writing (January 1, 2007), 10,000V SiC MOSFETs are in fact available from Cree. Those have been under development with DARPA funding for several years. One of the early applications of those devices will be a high frequency transformer for use on future aircraft carriers. Peregrine has teamed with a group of companies and people in a proposal to DARPA to supply that innovative system and has had many discussions with Cree about the availability, cost and performance of its 10,000V SiC MOSFETs. Had Phase II of this DOE SBIR project been funded, a 4,160VAC converter would have been actually developed in the near future, thus making a high power, high voltage converter available for many energy systems. The extraordinary simplicity of the topology using 10,000V SiC devices would undoubtedly have led to higher performance at reduced cost for the industry.

2 CONCLUSIONS

The major conclusions reached in Phase I are as follows:

- SiC devices continue to look superior to silicon devices in high power applications in part because of their substantially high voltage stopping capability. After four decades of development, there is still no silicon device in the market capable of becoming the basic power semiconductor in a modern, six-device inverter for 4,160VAC applications – more complicated topologies are necessary. SiC devices, on the other hand, have already been fabricated in prototype form at sufficient voltage for this application and commercial introduction of one or two of types of SiC devices can be expected during the next several years. The development of 10,000V SiC devices is actively supported by DARPA and the Navy, with Northrop Grumman, Cree and Purdue University under contract to carry out the development work.
- The benefits of using SiC are the greatest when a substantial increase is necessary in voltage, temperature or switching frequency. The level of benefit is thus a strong function of the application.
- The high power energy system applications targeted in this project are benefited greatly from SiC because all three of the above operating conditions are present, namely, higher voltage, higher temperature and higher switching frequency.
- Whether elevated temperature with SiC devices leads to benefits depends on the application. In general, conduction losses increase with increasing temperature, whereas switching losses do not. In applications with low switching speeds where conduction losses dominate, the increase in thermal gradient is offset by the increase in losses. The offset is much greater with a JFET and indeed the offset essentially eliminates the high temperature advantage. The BJT's conduction losses do not rise so steeply with temperature and thus higher temperature makes more sense with them. If the application calls for high switching speeds, SiC at elevated temperature always wins out.
- A 480VAC, three-phase inverter operating at 275°C and switching at 20kHz to minimize the size of passive filter elements will have weight/material of less than one-sixth of that required with a comparable inverter using silicon IGBTs. This inverter would use SiC BJTs. A similar comparison for inverters operating at 4,160VAC should give significantly better results, but there is no credible technical basis at this time to quantify the losses in the necessary 10,000V devices. However, the fundamental physics of SiC is simply superior to silicon, particularly at high voltages.
- Device and power module packaging for a 200°C junction temperature is straight-forward, and packaging for 300°C appears to be feasible although considerable experimental work will be required.
- The filter hardware for high power, SiC-based inverters is dominated in weight/material by two large inductors. The inductance of these is inversely proportional to the switching frequency and thus can be reduced by a factor of ten by increasing the frequency from 1kHz where it is today in typical 4,160VAC inverters (drives, e.g.) to 10kHz. High power inductors for 10 and 20kHz applications are not made today, but there appears to be no fundamental obstacle to their design and fabrication.

3 BACKGROUND

3.1 Power Electronics Generally

Power electronics is the segment of electronics dedicated to the conversion of electrical power from one form to another using power semiconductors. Power electronics has become fundamental to the generation, distribution and use of power throughout the civilian world. The project focused on power electronics for renewable and distributed power systems, almost all of which produce power in an unusable form which must be converted into a usable form. An inverter is required (at a minimum) by fuel cells, photovoltaic cells, variable speed wind and hydro turbines, micro turbines and all of the types of energy storage systems now being marketed or developed.

Like all other major components of advanced generation and storage systems, there is intense pressure to increase performance and reduce cost. The use of wide band gap materials in power semiconductors is one of the major leaps forward in power electronics. As noted in the SBIR/STTR solicitation, they offer dramatic improvements in efficiency, voltage level, higher switching frequency, higher operating temperature and other important parameters. These benefits are discussed in more detail later.

Peregrine as a business is focusing on the application (as opposed to the production) of SiC devices and has several projects underway in which SiC power semiconductors are being applied to specialized systems, primarily for the military. The military (DARPA and Air Force, e.g.) have made substantial investments in the development of SiC and a variety of prototype switches are becoming available. Now is the appropriate time to get serious about applications. The military applications will lead the civilian market due to their special needs and lower regard for cost, but ultimately the civilian markets for power electronics will be greatly impacted too. Peregrine will be involved in the early military applications, but intends to be part of the civilian applications that follow. Due to its experience in developing compact converters, Peregrine is well positioned to evaluate and apply these revolutionary power semiconductors.

The converter proposed in this project has a topology that can carry out all of the conversion functions required by any type of renewable or distributed energy system. Any particular renewable or distributed energy system will use all or a subset of the converter, so it might be termed a "universal" converter which can demonstrate all of the needed conversion capabilities. The work product of this project therefore represents a technology platform from which a wide range of converter types and ratings can be designed.

3.2 Advantages of Silicon Carbide

All commonly used power semiconductors in power converters today are based on standard silicon technology which has a variety of known limitations that power electronics designers must work around. SiC has been known for over two decades to have much better properties and has thus received substantial development funding by military and civilian organizations. SiC is termed a "wide band-gap" material in reference to the stability of the outer electrons. A larger amount of energy must be injected to lift the electrons to a state where they will facilitate electrical or molecular processes. Thus, SiC will not readily conduct electricity (movement of outer electrons), and has a very high breakdown voltage and dielectric constant. It is chemically stable and in fact is the third hardest material known.

The favorable characteristics of SiC compared to silicon are discussed in detail in a variety of technical reports. An excellent example is "Impact of SiC Power Electronic Devices for Hybrid Electric Vehicles" by Dr. Leon M. Tolbert, et al, (2002) prepared for Oak Ridge National Laboratory. Pertinent information can also be found in many of the other listed references. Each of the potential benefits will now be summarized and qualified where there are factors which may reduce the benefit significantly.

- **Lower resistance and conduction losses.** A SiC semiconductor die is much thinner on account of its higher breakdown strength and is doped to a much higher level. This may lead to lower losses and smaller, less expensive heat removal hardware. The basic physics indicate that the forward resistance across the blocking layer of a MOSFET, for example, is about $1/400^{\text{th}}$ of

that for silicon. Qualification: This is a startling theoretical limit that has attracted much attention. However, experts will quickly add that this figure is highly misleading. The statement describes only the blocking or drift region. This is an important layer through which the current must pass from source to drain, but the current must pass through other regions and connections which also contribute substantially to the total resistance. In fact, some SiC devices have higher conduction losses than their silicon counterparts. To bring this point home, at comparable temperatures and current densities, some of the SiC devices tested in this project had similar conduction losses as the silicon devices they would replace. The conduction loss for SiC devices will undoubtedly improve in the years ahead and beat the silicon counterparts, but it will not be an order of magnitude better at similar current densities. The overall losses for SiC MOSFETs when replacing standard silicon IGBTs are expected to be reduced by about 1/3 over the next five years or so.

- **Lower switching losses, due to faster turn-on/ turn-off characteristics.** This is a true statement for nearly all SiC devices without much need for qualification. In addition, devices with extraordinarily fast, low loss switching (e.g., MOSFETs and Schottky diodes) can be used at higher voltages when made of SiC. Thus, a SiC MOSFET can be realistically used in a 480 or 690 volt converter, rather than a silicon IGBT, to increase switching frequency from, say, 5 kHz to 50 kHz. A MOSFET could not be used effectively in this application if made of silicon. While a Schottky diode might be rated at less than 200 volts when made of silicon, it can easily withstand 1,200 to 1,700 volts when made of SiC. A Schottky can then be used as the reverse or anti-parallel diode which accompanies a transistor to protect it from reverse voltage bias. The SiC Schottky, which is in the market today, has little reverse recovery current, a significant source of switching losses in a typical inverter bridge, particularly at low power. Qualification: Translating the switching improvements into a bottom line product improvement is, however, a function of the application. If higher speed switching is not needed, the product improvement would be small. The higher speed is needed in this project to reduce the size of the passive elements in the output filter, as discussed later.
- **Higher breakdown voltage, permitting higher voltage applications.** Most types of SiC devices will be able to withstand nearly ten times the voltage of their silicon counterparts. Some SiC devices (e.g., IGBTs) may be able to withstand more than 20,000V. This characteristic can be used to increase the voltage of an energy system, thus decreasing current, and the size and cost of all current-carrying components. This benefit is quite real and requires no qualification. Indeed, this is the basis in this project for recommending the use of medium voltage (4,160VAC) for applications above one MW.
- **Higher thermal conductivity.** SiC has conductivity about three times as high as standard silicon; thus losses in the form of heat will be conducted from within the semiconductor with a much lower temperature drop across the semiconductor material. That, coupled with its lesser thickness, allows the die to be driven much harder and reduces material and cost. Qualification: Higher conductivity is always a plus, but this scientific fact is probably not as important as the next listed benefit. If the device temperature is increased to, say 300°C, the conductivity within the extraordinarily thin layer of the SiC die is not particularly important. The maximum temperature difference within the SiC die to drive its heat outward might only be several degrees C.
- **Much higher operating temperature, well over 400°C.** This should be compared to 125 to 150 °C with standard silicon technology. This characteristic leads to the use of much greater temperature differentials, and less material and potentially cost. It also leads to the ability to use low-cost air cooling hardware rather than liquid cooling to a much higher power level. Qualifications: The first qualification is that some devices, such as the MOSFET and IGBT, contain an oxide which is fundamental to their operation. The oxide layer will breakdown beginning in the 200 °C area. Ongoing R & D may increase the temperature at which the oxide degrades, but it is clear that with these devices, the high temperature capability of SiC cannot be fully exploited. The second qualification is that while the SiC device can withstand the higher

temperature, nothing else in the semiconductor package can – at least at this time. Higher temperature packaging designs must be developed if the high temperature benefit is to be realized. The final qualification is that if high temperature is not an absolute requirement for a given application this capability might have little value. A favorable impact then would depend upon exploiting high temperature to reduce material and cost.

- ***Much greater ruggedness and reliability.*** This is the natural product of being a wide band gap material. Qualification: The greater ruggedness will undoubtedly be necessary since the devices will be subject to much greater punishment. With higher voltages and currents, there may be exposure to much higher dv/dt and di/dt . Until these conditions are actually experienced in SiC devices, it is not clear if the devices will be sufficiently rugged without protective measures. In addition, high reliability will require time to realize. The primary failure mechanisms in a mature power semiconductor are de-lamination of substrates and detachment of wire bonds, both caused by wide and frequent thermal cycling. The use of much higher operating temperatures will only exacerbate the thermal cycling problem and require better matching of coefficients of thermal expansion (CTEs) in the device package.
- ***Positive temperature feedback as to resistance.*** This property automatically causes current to be shared well among SiC dies which are paralleled to achieve higher currents. Increases in current cause increases in temperature, which in turn increases resistance and prevents current runaway in any particular die. This property will be extraordinarily important over the next few years, because the ampacity of SiC devices will be inadequate without the paralleling of dies. As the defect rate in SiC wafers falls, larger die will become available, but the paralleling of die will probably continue, as it has for silicon IGBTs and MOSFETs.
- ***High current density.*** The maximum current density for most types of SiC dies is at least 200 amps/cm² and in some types will exceed 300 amps/cm² - two to three times the maximum current density of silicon devices. This property will eventually tend to reduce cost, thus offsetting some of the cost disadvantages of SiC device fabrication. Qualification: For many types of devices, increasing current density increases forward conduction losses in a linear fashion. The current capability of SiC may in fact not be exploited by the designer; rather losses will be minimized by using low current densities in order to make even larger reductions in material and cost of cooling hardware.

3.3 Topology & Applications

Figure 1 shows the topology to be used in the converter being developed in this project. In general, it is comprised of two back-to-back inverters with a DC bus in between. The power devices shown in Figure 1 are SiC MOSFETs, which are indeed important candidates for this project, but they could also be BJTs, GTOs, JFETs or IGBTs. The inverter (along with the output filter) is the target of this project. This topology is responsive to a wide variety of applications. A variant can be used with essentially any type of renewable or distributed energy system. The form of electricity from any anticipated source (DC or AC of any frequency or voltage) can be converted into the form required by any load (DC or AC of any frequency or voltage). The basic conversion capabilities will now be described in the context of specific energy systems.

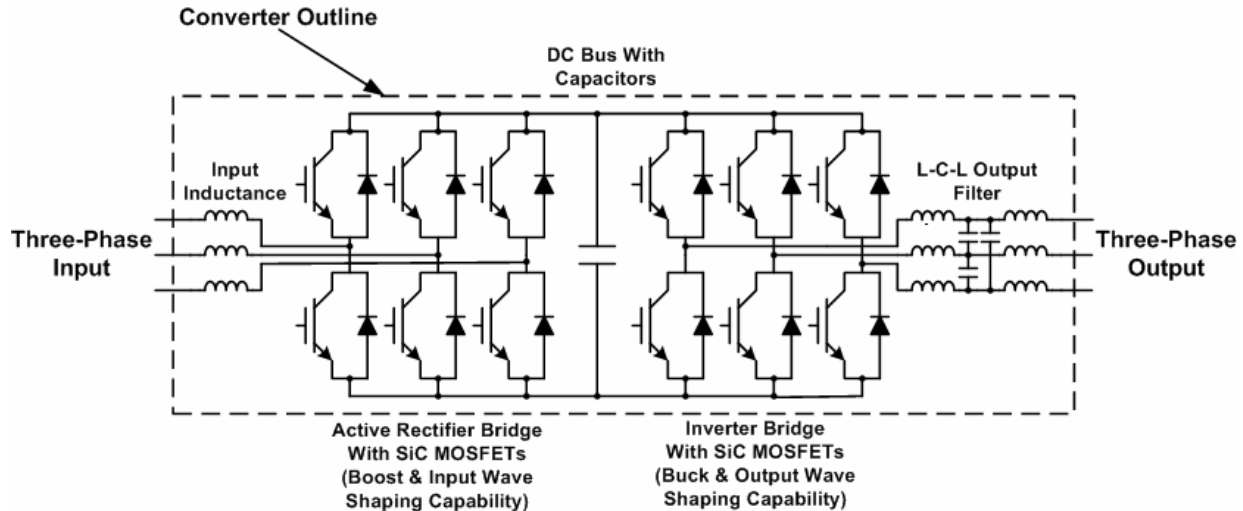


Figure 1. Circuit Topology of Conversion System with SiC Devices

3.3.1 Fuel Cells

A fuel cell produces unregulated DC over a range of voltages as the load changes. Generally, the voltage supplied to a load or the grid must be regulated to a constant value under all circumstances. Thus, the voltage of the output of the fuel cell must be bucked (reduced) or boosted as the power level changes. Using the inductance at the input (shown), the input stage is capable of boosting to maintain a constant DC bus voltage. In addition, this configuration is capable (normally using a hard switching PWM strategy) of shaping the waveform of the current imposed back on the generation system. This provides important benefits, as will be discussed below. When applied to a fuel cell, the input bridge processes DC, which only needs four active switches rather than the six shown, but the principle of operation remains the same.

The output inverter bridge (generally using a PWM hard switching strategy) produces power of any desired frequency (including zero Hz or DC). The output filter removes the carrier (PWM) frequency and smooths the waveform so high quality power can be delivered to the load or grid. The output inverter bridge can be used to regulate voltage giving another control variable for output voltage. Again, if the output must be DC, the output inverter bridge need only contain four switches rather than the six shown, but the principle of operation remains the same. Thus, a version of the proposed topology is ideal for linking the output of a fuel cell to a load or grid.

3.3.2 Photovoltaic Cells

Photovoltaic cells are, of course, quite different than fuel cells, but their output has the same characteristics – DC with varying voltage. The same functionality described for the fuel cell above is necessary in a generation system based on photovoltaic cells.

The ability to impress voltage on or regulate current from the PV source has value. For any given amount of incident solar radiation, a photovoltaic cell can operate at a continuum of voltage/current values defined by a single curve. One of the points on the curve gives the highest amount of power. Maintaining this maximum requires the ability to impose varying voltages (or regulate current) back on the string of PV cells as the incident radiation varies. The proposed topology has this capability and thus can be made to continuously seek the maximum.

3.3.3 Variable Speed Wind Turbines

All large wind turbines either do (or will) use variable speed systems with solid state converters to increase energy production, control mechanical stresses in the drive train and regulate the power factor imposed on the grid. As the speed of the generator in a variable speed wind turbine varies up and down, the voltage and frequency of the generator output varies up and down in proportion to speed. The input and output of the converter will be three-phase AC in this application, so the version shown in Figure 1 (six power switches in both of the input and output inverter bridges) is appropriate. The input inductor might be eliminated if the inductance of the generator is sufficient (normally it is). This converter will impose sinusoidal current back on the generator, so it will not be subject to harmonics heating, an important factor in minimizing the cost of the generator. The converters used in most large, commercial variable speed wind turbines today use precisely the topology shown in Figure 1.

3.3.4 Variable Speed Generator Set

Generator sets using reciprocating engines (\$5 to 6 billion worldwide market) benefit from variable speed operation in two primary ways: (1) speed can be optimized at all power levels, thus saving fuel (up to 40 percent) when operating at less than full power, and (2) more power can be generated from any given engine by higher speed operation (super-synchronous). Variable speed gensets are of great interest to many segments of the genset market, particularly those sensitive to fuel cost (prime power applications) or size (portable applications). The preferred generator here is normally the PM type. The converter requirements for this generation method are the same as for the variable speed wind turbine since in both cases the source is usually a three-phase rotating generator and the load is three-phase (single-phase at low power).

3.3.5 Micro Turbines

This application is the same as the variable speed wind turbine and genset, with one added requirement. The turbine engine must be spun up to a fairly high speed before being ignited, so the converter must operate in reverse (as a drive) for starting. The proposed topology can readily operate that way too since it is bi-directional and has four-quadrant capability. In fact, the wide-spread value in industry of the drive mode of operation is discussed in the next paragraph.

3.3.6 Variable Frequency Drives

While a drive is not a fundamental part of a generation industry, it is very important to the world's energy economy. The greatest single use of electricity in industry is in powering motors and the market for drives (motor controls) exceeds \$12 billion annually. This is the largest single market for power electronics in the world. Drives can save over 50 percent in energy in some cases over standard across-the-line motors and can also give precise control over manufacturing processes. Virtually all AC drives in the market today are the same as, or subsets of, the topology shown Figure 1. In fact, the most complex AC drive (capable of 4-quadrant operation) has precisely this topology, except that it is operated most of the time in reverse. The variable speed generator here becomes a motor whose speed (or torque or position) is controlled by the converter. This drive topology not only controls the motor, but has excellent power quality upstream and complies with IEEE519, the North American standard on harmonic distortion.

4 ANTICIPATED PUBLIC BENEFITS

In the previous sections, detailed technical benefits of the proposed approach were given. First, the benefits of using SiC devices were listed. In summary, SiC-based power electronics will lead to higher performance, smaller size and lower overall system cost. Second, the many types of energy systems where the proposed circuit topology could be applied were described. Thus, the project will improve the performance and cost of energy for many renewable and distributed energy systems, making them more competitive and encouraging their use.

Renewable energy and distributed power lead to unique benefits. Renewable energy uses no costly fuel which is in limited supply, has little or no effluent or other environmental impact, and reduces dependence on foreign oil. Distributed power offers several utility system benefits, such as reduced current levels on distribution lines, lower system losses and reduced risk of blackouts and similar events.

The specific beneficiaries will include all customers of public utilities – consumers, commercial establishments and industrial plants. Other beneficiaries are the utilities themselves and the suppliers of hardware and services used to produce or maintain the renewable and distributed energy systems.

5 PHASE I PROJECT & RESULTS

5.1 Phase I Objectives & Work Plan

The Phase I technical objectives were

- to design a SiC-based universal converter with the following specifications:
 - 10 kW (or more), scalable to 500 kW
 - Compact, air cooled
 - Three-phase, 480 VAC
 - Output filter enabling the production of high quality power
 - Operation at 250 degrees C, and
- to evaluate the improvements in size/weight, efficiency, power quality, cost and other important characteristics.

If the improvements were found to be substantial, the approach would be deemed to be feasible and actual hardware development in Phase II would be recommended.

The original work plan was as follows:

- Task 1 Meet With DOE
- Task 2 Characterize SiC MOSFETs & Converter
- Task 3 Design Semiconductor Power Block and Heat Sink
- Task 4 Design Driver and Control Cards
- Task 5 Design Output Filter
- Task 6 Assess & Report

5.2 Adjustments to Phase I Objectives & Work Plan

During Task 1, several modifications to the proposed work plan were made at the outset because the team actually began at a starting point that was substantially more advanced than had been anticipated in the Phase I proposal. This was the result of having just finished three other small projects in which SiC devices had been evaluated for three applications. The applications included a 5kW inverter for Army mobile power, a 40kW converter for a Navy actuator and 1.5MW inverter for large wind turbines. These projects led to the following results:

- Peregrine strongly recommended medium voltage (4,160VAC) for all multi-MW applications. This is enabled by the use of SiC and leads to many system benefits, as well as inverter performance and cost benefits.
- A high temperature packaging design for SiC devices had been developed and now needed to be tested.
- The team had developed a much better understanding of how to exploit the unique advantages of SiC. Further efforts should be revised to reflect that knowledge.
- The team was in a much better position to select appropriate devices for specific applications, given the various potential suppliers and their technologies.

Rather than carrying out a balanced converter design exercise (including control cards, gate drive circuits, enclosure, etc), it was believed to be more productive to focus on specific problems that might stand in the way of a successful outcome. Those were now the critical path. In addition, the team was anxious to test a variety of SiC devices to learn first-hand about their performance characteristics rather than blindly accepting published data and commentary, some of which is overly promotional.

Indeed, the Peregrine team could not proceed with any inverter design without knowing what the losses were going to be at various temperatures for various candidate devices over a temperature range from room temperature up to 300°C. Neither the literature or SiC device vendors had the information needed to design a high power inverter that would actually operate at full power over extended periods of time. Of particular concern was the degradation of performance of SiC devices at elevated temperature.

The full list of critical problems identified by Peregrine in its prior work is as follows:

1. Deterioration in performance of SiC devices at high temperature (conduction losses, switching losses and gain (β) in current gated devices)
2. Control and protection issues associated with the normally-on property of SiC JFETs
3. Lack of reliable high temperature power semiconductor packaging
4. Improvement of reliability of SiC devices in general through duration testing
5. Increasing the temperature capability of components other than the SiC devices (if they are placed near the SiC power semiconductors)
6. Availability of high voltage devices (10,000 volts devices for 4,160VAC applications)
7. Reduction in cost by using volume-oriented packaging techniques and piggy-backing on existing medium voltage power electronics products.

Therefore, the Phase I objectives were changed with the approval of DOE in the kick-off meeting to take on as many of these issues as possible with the limited time and budget of a Phase I SBIR project. The work plan tasks were changed to the following:

- Task 1. Meet with USDOE
- Task 2. Obtain Appropriate SiC Devices
- Task 3. Design & Build Test Fixture
- Task 4. Carry Out High Temperature Testing
- Task 5. Design High Temperature Package
- Task 6. Characterize High Power SiC-Based Inverter
- Task 7. Project Administration and Reporting

Phase I, as actually carried out, addressed the issues labeled as 1, 2, 3, 6 and 7 above, with primary emphasis on 1. The team now believes it can move ahead to develop prototype inverters leading to the targeted 4,160VAC inverter design rated at 1MW. The detailed results of Phase I will be covered below.

5.3 Research Team

The research team for Phase I was comprised of the following:

- Dallas Marckx, Principal Investigator
- Brian Ratliff, Staff Engineer – Thermal & Materials
- Matthew Jones, Staff Engineer – Power Electronics
- Dr. Amit Jain, Senior Engineer – Power Electronics
- Larry Rinehart, Consultant - Power Semiconductors and Packaging
- Dr. Cathy Biber, Consultant - Thermal Management

A variety of other people made significant contributions:

- Dr. David Grider and Dr. Anant Agarwal of Cree, Inc.
- Dr. Jian Zhao of Rutgers University
- Dr. Peter Friedrichs of SiCED Ltd.
- Dr. Leonid Fursin of United Silicon Carbide, Inc.
- Dr. Leon Tolbert of University of Tennessee
- Dr. William Erdman of Behnke, Erdman and Whitaker, Inc.

5.4 Phase I Test Results - SiC Performance at Elevated Temperature

5.4.1 Test Objectives

The reason for testing at elevated temperatures was to determine the performance of each candidate SiC device over a wide temperature range. The testing was also able to reveal relationships of key modeling parameters of devices with respect to the changing temperature. These relationships can show the maximum safe operating area for devices or be used to model full converters at different junction temperature operating points.

The most prominent temperature-dependent characteristics for a device are (1) the static forward current-voltage curves, (2) the leakage current when devices are intended to stop forward current, (3) the gating requirements to turn the switches on and off, and change in such gating requirements with temperature, and (4) the losses during switching. The static forward current-voltage curves show a designer the best voltage range for operating a device and give the conduction losses that will be incurred in a converter. The leakage current characteristics are important in determining the breakdown voltage and maintaining the health of the device. A change in the gating requirements for the device with increased temperature can make the gate driver ineffective in turning the device on or off, which might cause converter malfunction or even destruction. The switching characteristics are important in determining the switching losses in a converter and in setting an appropriate switching frequency.

5.4.2 Test Set-Up & Procedure

The test equipment used is given in Table 1.

Type	Model	Manufacturer	Serial #
Tester	STI 5150	Scientific Test Inc	219
Power Supply	GPS 2303	Instek	EF903460
Power Supply	210-01R	Bertan Associates Inc.	71978
Multimeter	9005	Triplett	1021366336
Oscilloscope	DL71420-D/B5/N2	Yokogawa	12V916290J
Voltage Probe	700988	Yokogawa	
Current Probe	CWT3/100M	Power Electronics Measurement Ltd.	7703

Table 1. Test Equipment

A semiconductor tester was used to obtain the static characterization of each device. Each device was mounted on a hot plate, thermally insulated, and electrically wired to the semiconductor tester, as shown in Figure 2.



Figure 2. Static Test Setup for High Temperatures

For the Schottky diode, the STI 5150 was used to measure the forward voltage for multiple current levels to obtain forward I-V curve. The leakage current of the device was measured when the reverse voltage was 1000V. All measurements were taken over a temperature range from 20°C to 300°C.

For the JFET, the STI 5150 was used to measure the drain-source voltage for multiple drain current levels, keeping the gate-source voltage at a fixed 3V, giving forward I-V curve for a particular temperature. This was done over a temperature range of 20°C to 300°C. To find the leakage current of the device, the STI 5150 was not used because it was unable to provide the needed gate-source voltage of -30V to properly turn-off the device at higher temperatures. As seen in Figure 3, a 30V power supply was used to bias the gate-source voltage to -30V. A separate power supply was used to provide a drain-source voltage of 800V. The leakage drain current was measured by using a series sensing resistor of 100kΩ and measuring the voltage drop across the resistor with a handheld meter. This was also done with the JFET mounted to the hotplate and recorded for the temperature range of 20°C to 300°C.

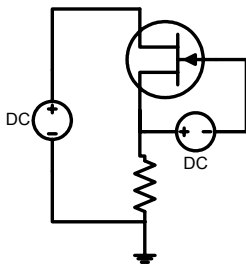


Figure 3. Biasing of Gate Circuit

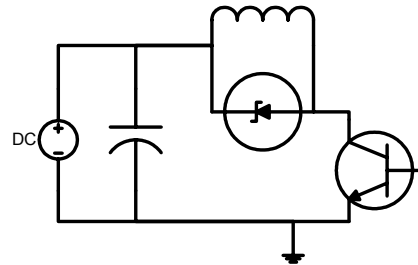


Figure 4. Inductive Load Switching Circuit

For the BJT, measurements were taken for the collector-emitter voltage for multiple collector current levels, keeping the base current at a fixed 500mA. This gave the forward I-V curve for a particular temperature. The base-emitter voltage was measured with the collector current at 10A and a base current of 500mA. The leakage collector current was measured when the device had a collector-emitter voltage of 1000 V with the base shorted to the emitter. Each of these tests were done by with the STI 5150 for the full temperature range.

The switching characterization was done by conducting an inductive load double-pulse test. The circuit diagram in Figure 4 shows the basic setup. A power supply was used to create a 600V DC bus and a hand-wound air core inductor with measured inductance of 2.1mH was used the inductive load. The current through the device was about 7.3A at the time the device was switched. A SiC Schottky used for the freewheeling diode was mounted to the same hotplate as the SiC BJT. The base driver used a 12V supply through a 13Ω resistance for turning on the device with about 700mA base current. A -3V base-emitter bias was applied through a 50mΩ on-resistance MOSFET to turn off the BJT. The collector-emitter voltage was measured, along with the collector current at turn-on and turn-off of the switch. The testing took place over a temperature range of 20°C to 300°C. The JFET was tested at 0.5A drain current, 100V drain-source voltage with the same inductance and the diode at 20°C. The gate driver turned the device on with +3V gate-source voltage through a 25Ω resistance and turned the device off with -30V gate-source voltage through a 10Ω resistance. The JFET's switching was not tested at elevated temperatures due to a large amount of ringing brought on by the very fast switching time of the JFET and the stray inductance of the test circuit caused by the long wires necessary to keep most of the instruments away from the hotplate.

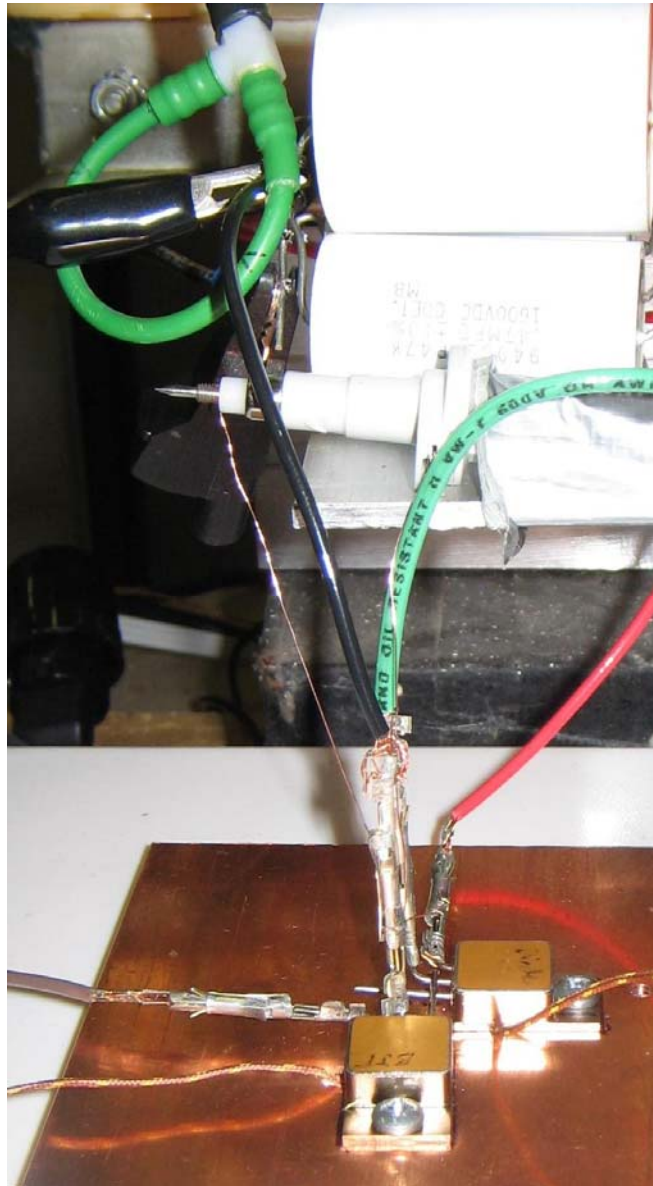


Figure 5. Dynamic Test Setup for High Temperatures

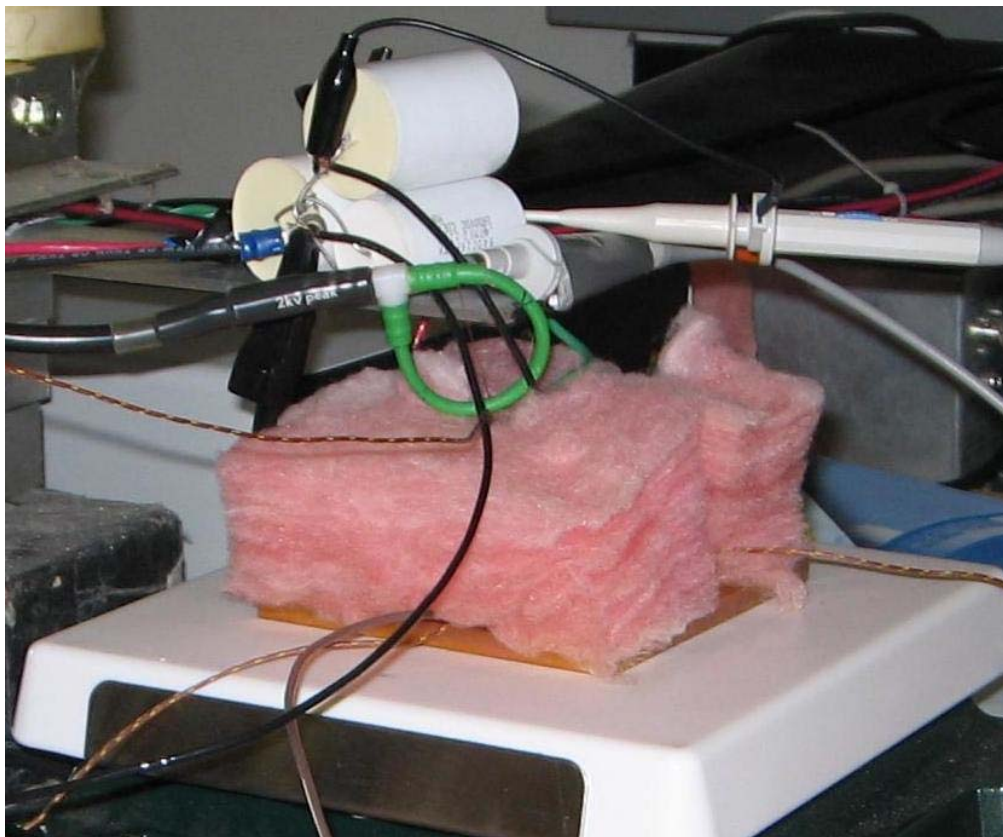


Figure 6. Dynamic Test Setup for High Temperatures

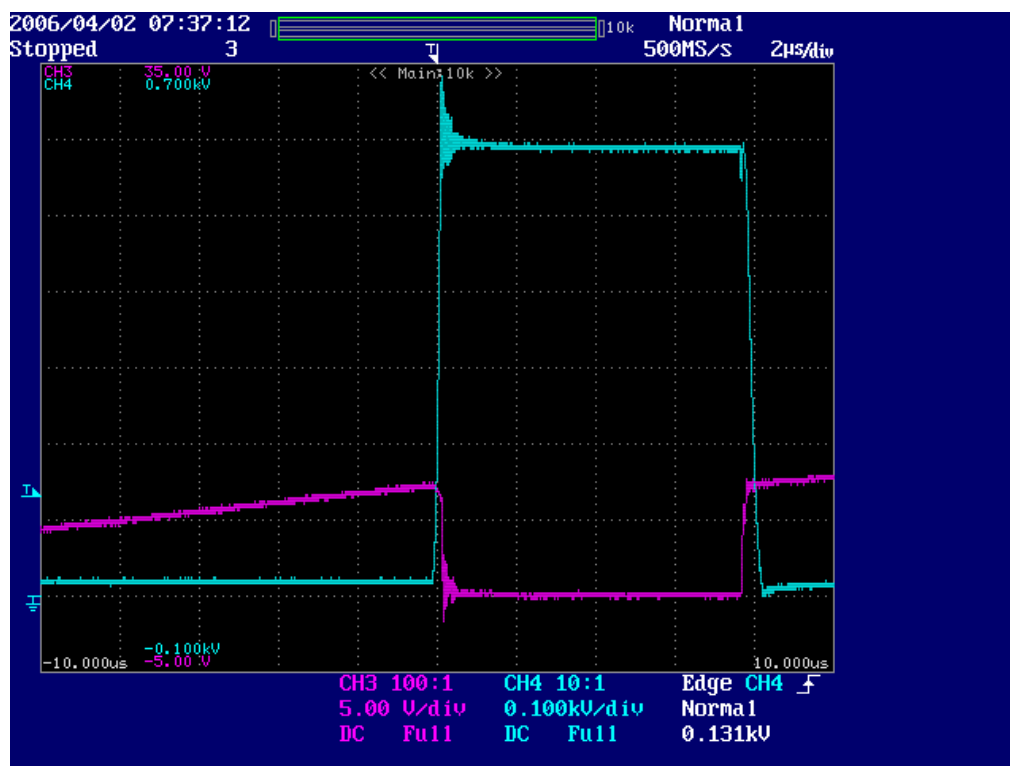


Figure 7. Oscilloscope of SiC BJT Double-Pulse Switching at 50°C

The following SiC devices were ordered:

- BJTs from Cree
- JFETs from SiCED (Germany)
- BJTs from United Silicon Carbide
- Schottkys from Cree
- BJTs from TranSiC (Sweden)

These particular devices were selected because they will be able to withstand temperatures of over 300°C, a requirement in most of Peregrine's current work. All of the devices were received except for the BJTs from TranSiC, who had offered samples without cost. At the time of this writing, they have still not been received.

Cree's Schottky diodes are commercial devices rated at a blocking voltage of 1200V and a forward current of 20A. They can be operated continuously to 175°C when purchased as a fully packaged part. The parts data sheet for the regular packaged product can be found at <http://www.cree.com/products/pdf/CSD20120.PDF>. However, the Schottky dies were purchased by Peregrine loose (no packaging) and mounted according to Peregrine's specifications by Solid State Devices Inc. for operation to 300°C.

Cree's BJTs were rated at a blocking voltage of 1500V and forward current of greater than 30A; forward I-V characteristics were provided for typical devices at 25°C and 250°C, and a reverse I-V characteristic was also provided at 25°C. This data is included in Figures 8 and 9.

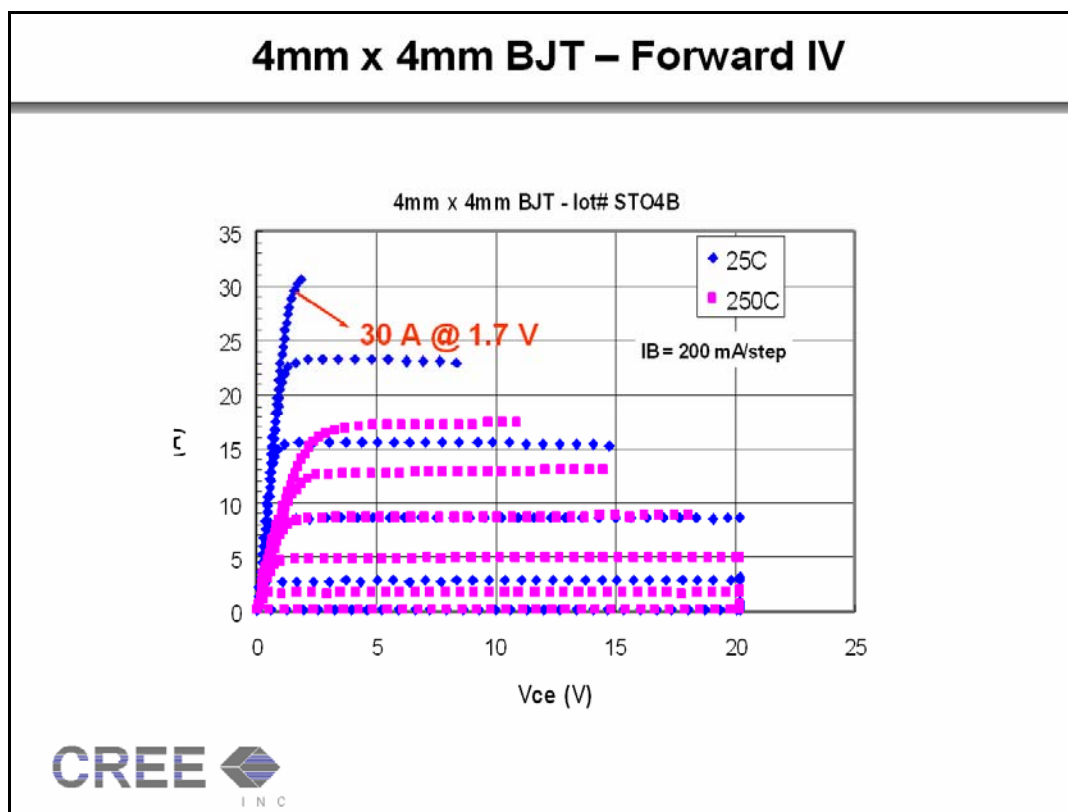


Figure 8. Cree's BJT – Forward IV Characteristics

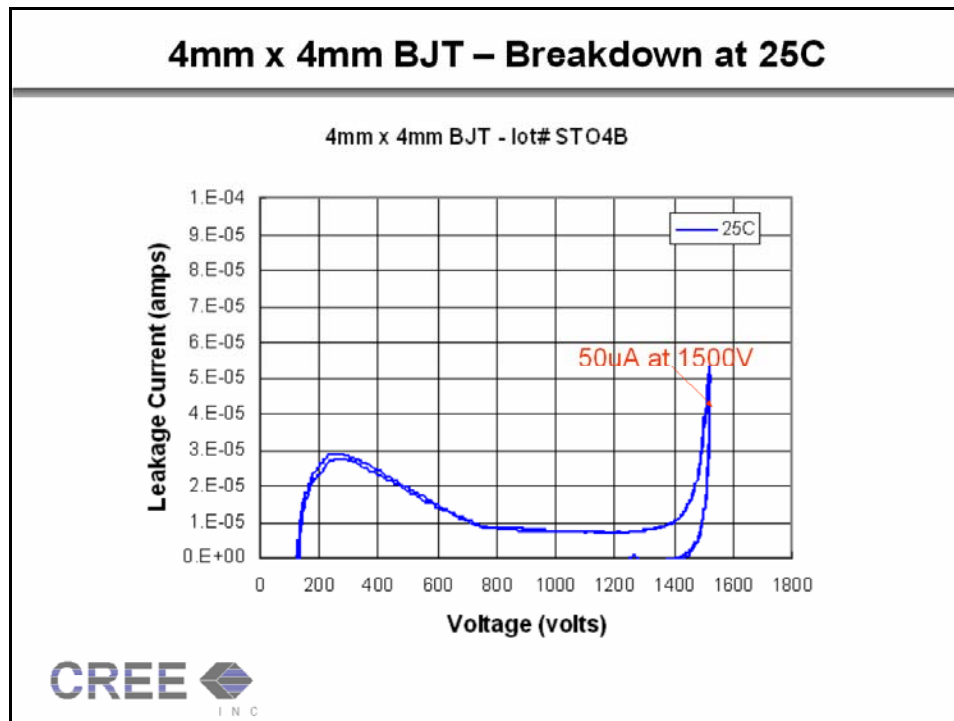


Figure 9. Cree's BJT – Breakdown Characteristics

United Silicon Carbide's BJTs were rated at a blocking voltage of greater than 1000V, forward current of greater than 10A, and specific on-resistance of less than $10\text{m}\Omega\text{cm}^2$. Forward and reverse I-V probing of each die was provided and a typical forward I-V characteristics after wire-bonding. This data is included in Figures 10 and 11.

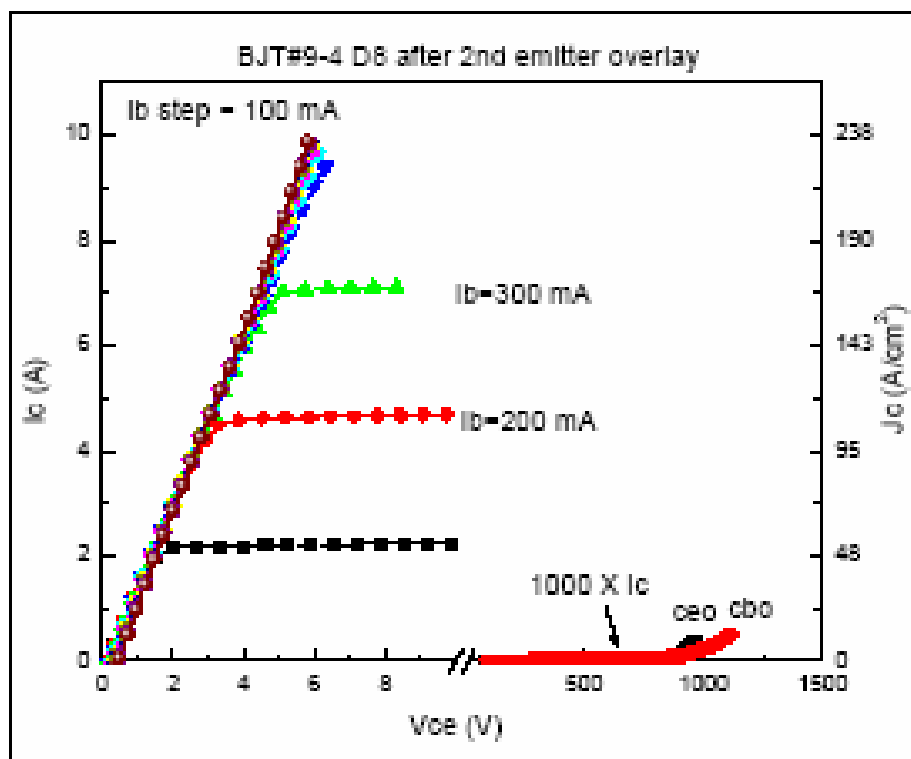


Figure 10. USCI's BJT Forward Characteristics from Die Probing

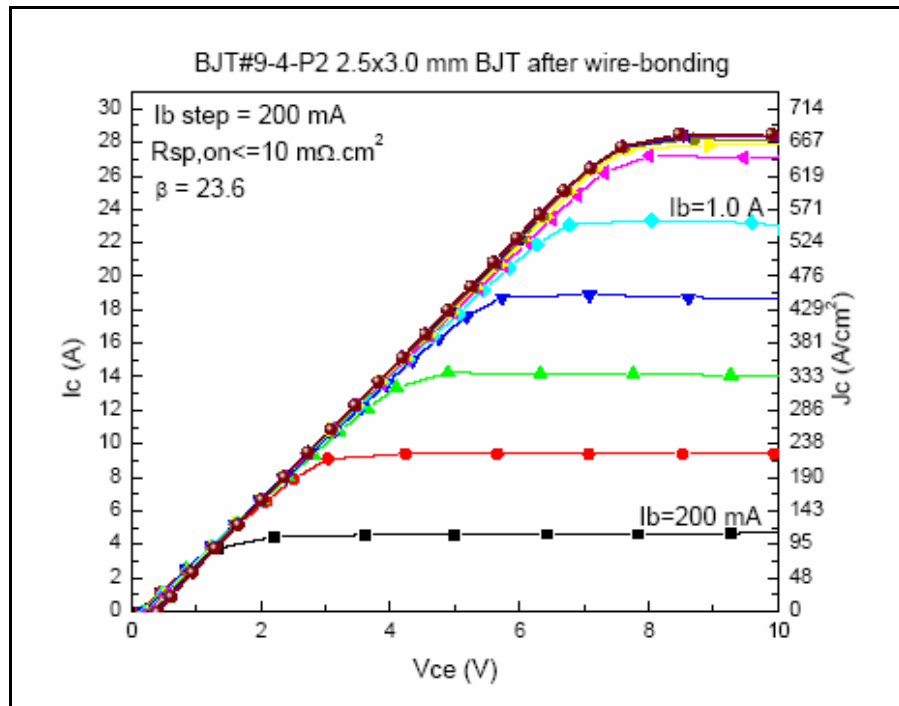


Figure 11. USCI's BJT Forward Characteristics after Wire-Bonding

SiCED's JFETs were rated at a blocking voltage of 1200V with an on-resistance of less than 0.35Ω at room temperature.

5.4.3 Results

The collected data for the Schottky diode is tabulated on the following page. The built-in voltage of the diode drops linearly with temperature and the on-resistance of the diode increases with temperature. The leakage current was found to have an exponential relationship with temperature. The SiC Schottky diode is well-deserving of the marketing name Zero Recovery Diode. The team was unable to accurately measure the reverse recovery loss of the diode on the time scale of the oscilloscope when set to measure the switching losses of the BJT. It is assumed they are negligible compared to the transistor switching losses when calculating for the inverter models.

The on-resistance for the JFET increases exponentially with temperature. This causes over 5 times the conduction losses at 300°C when compared to 20°C . This is precisely that type of loss behavior that was expected in some devices and it will offset the gains that would be achieved by using elevated temperature to decrease size. The leakage current peaked at about $10\mu\text{A}$ at 245°C , and then decreased almost as steeply as it had risen. An observation on the gate drive requirements at high temperature was that the current from the gate increased dramatically as the temperature increased. We observed a constant -60mA for a gate current at 180°C and this had increased to -110mA at 290°C ; the gate-source voltage was held at a constant -30V . The current capacity will need to be considered carefully when designing at gate driver for the JFET at high temperatures. A non-temperature related observation with the leakage current of the JFET was that when the JFET was turned off with -30V gate-source voltage and the drain-source voltage was increased, the leakage current would spike at approximately 770V . The leakage current would gradually decrease until it would be near the team's measurement limit. The drain-source voltage would then be increased and the effect would be seen again after a change of $10\text{--}20\text{V}$. The voltage at which the spike would be seen was gradually pushed higher if the device was allowed to settle the leakage current back to a low amount. The switching energy was measured for room temperature and matched very well to data from other sources.

If [A] \ T [°C]	20	50	60	70	80	90	100	110	120	130	140	150	160	170
0.01	0.789	0.735	0.720	0.706	0.686	0.672	0.652	0.637	0.623	0.608	0.589	0.574	0.559	0.542
0.02	0.808	0.759	0.745	0.725	0.708	0.696	0.681	0.664	0.647	0.632	0.618	0.603	0.589	0.569
0.05	0.838	0.786	0.774	0.759	0.740	0.730	0.716	0.701	0.686	0.672	0.657	0.642	0.628	0.613
0.1	0.855	0.813	0.799	0.784	0.769	0.759	0.740	0.730	0.716	0.706	0.691	0.676	0.662	0.652
0.2	0.882	0.842	0.828	0.818	0.803	0.794	0.779	0.769	0.755	0.745	0.735	0.720	0.708	0.696
0.5	0.930	0.896	0.886	0.877	0.867	0.862	0.852	0.842	0.833	0.823	0.813	0.808	0.794	0.794
1	0.994	0.969	0.960	0.955	0.950	0.945	0.940	0.935	0.930	0.926	0.926	0.921	0.916	0.916
2	1.092	1.092	1.087	1.084	1.087	1.092	1.092	1.096	1.101	1.106	1.111	1.118	1.126	1.136
5	1.355	1.414	1.424	1.443	1.468	1.482	1.512	1.536	1.565	1.600	1.634	1.668	1.707	1.746
10	1.785	1.946	1.966	2.020	2.083	2.120	2.190	2.249	2.332	2.405	2.484	2.562	2.652	2.742
11	1.873	2.049	2.078	2.132	2.205	2.249	2.327	2.396	2.488	2.569	2.654	2.742	2.845	2.947
12	1.956	2.156	2.190	2.249	2.332	2.379	2.466	2.542	2.640	2.733	2.830	2.928	3.040	3.153
13	2.044	2.261	2.293	2.366	2.454	2.508	2.601	2.689	2.794	2.899	3.001	3.109	3.236	3.358
14	2.132	2.361	2.410	2.484	2.581	2.640	2.742	2.835	2.952	3.065	3.182	3.294	3.436	3.568
15	2.215	2.464	2.518	2.601	2.703	2.769	2.884	2.982	3.109	3.233	3.363	3.485	3.636	3.783
16	2.303	2.567	2.630	2.718	2.821	2.899	3.026	3.128	3.265	3.402	3.534	3.675	3.836	3.993
17	2.386	2.664	2.742	2.835	2.947	3.031	3.162	3.280	3.426	3.573	3.719	3.866	4.044	4.208
Ir [μA] @ 1kV	1.812	2.208	2.09	2.405	2.513	2.610	2.786	2.918	3.123	3.338	3.570	3.866	4.337	4.921
If [A] \ T [°C]	180	190	200	210	220	230	240	250	260	270	280	290	300	
0.01	0.525	0.510	0.496	0.476	0.462	0.444	0.427	0.413	0.393	0.379	0.364	0.349	0.330	
0.02	0.559	0.535	0.525	0.510	0.496	0.476	0.462	0.447	0.432	0.415	0.398	0.383	0.369	
0.05	0.603	0.584	0.574	0.554	0.540	0.525	0.515	0.501	0.486	0.471	0.457	0.447	0.427	
0.1	0.637	0.623	0.613	0.598	0.589	0.574	0.559	0.545	0.535	0.525	0.508	0.496	0.486	
0.2	0.686	0.676	0.664	0.652	0.642	0.632	0.623	0.608	0.598	0.589	0.579	0.564	0.559	
0.5	0.784	0.779	0.769	0.769	0.759	0.752	0.745	0.740	0.735	0.737	0.730	0.720	0.716	
1	0.916	0.916	0.916	0.916	0.916	0.916	0.921	0.921	0.926	0.926	0.935	0.935	0.940	
2	1.145	1.160	1.165	1.179	1.194	1.209	1.223	1.243	1.263	1.277	1.297	1.321	1.341	
5	1.785	1.834	1.878	1.927	1.980	2.034	2.090	2.151	2.220	2.278	2.347	2.425	2.493	
10	2.835	2.960	3.050	3.172	3.294	3.416	3.543	3.683	3.831	3.973	4.120	4.286	4.442	
11	3.050	3.192	3.297	3.429	3.563	3.705	3.841	3.998	4.161	4.315	4.484	4.664	4.842	
12	3.265	3.421	3.538	3.685	3.836	3.988	4.139	4.315	4.496	4.669	4.847	5.048	5.248	
13	3.485	3.656	3.783	3.949	4.110	4.281	4.442	4.630	4.833	5.023	5.221	5.443	5.656	
14	3.705	3.895	4.032	4.208	4.388	4.569	4.750	4.955	5.170	5.380	5.595	5.834	6.068	
15	3.929	4.134	4.281	4.476	4.667	4.867	5.060	5.282	5.516	5.741	5.976	6.234	6.484	
16	4.154	4.374	4.530	4.740	4.945	5.162	5.370	5.609	5.858	6.103	6.352	6.635	6.906	
17	4.383	4.618	4.789	5.016	5.233	5.463	5.687	5.946	6.215	6.474	6.740	7.043	7.333	
Ir [μA] @ 1kV				5.651	7.126	8.842	34.33	52.11	80.32	121.4	295.0	279.9	510.1	

Table 2. Measured Data for SiC Schottky Diode at Elevated Temperatures

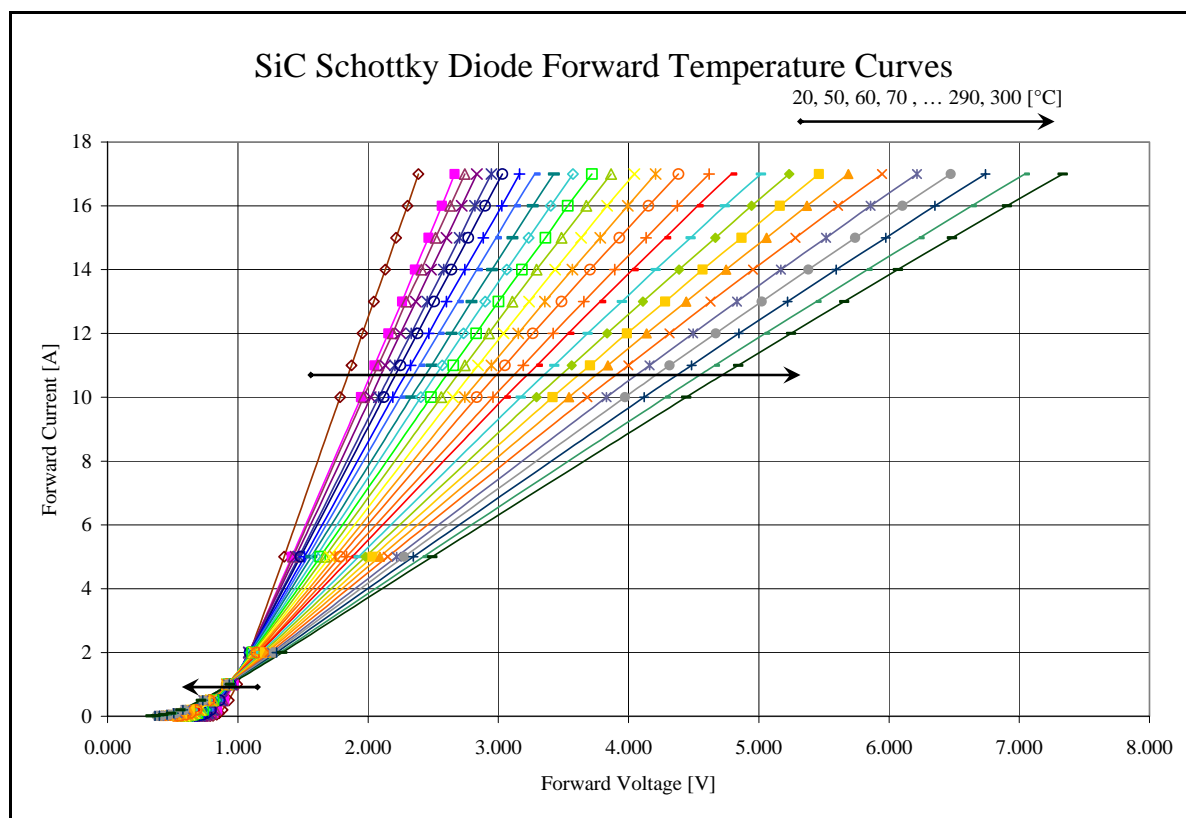


Figure 12. Measured Forward IV Temperature Curves of SiC Schottky Diode

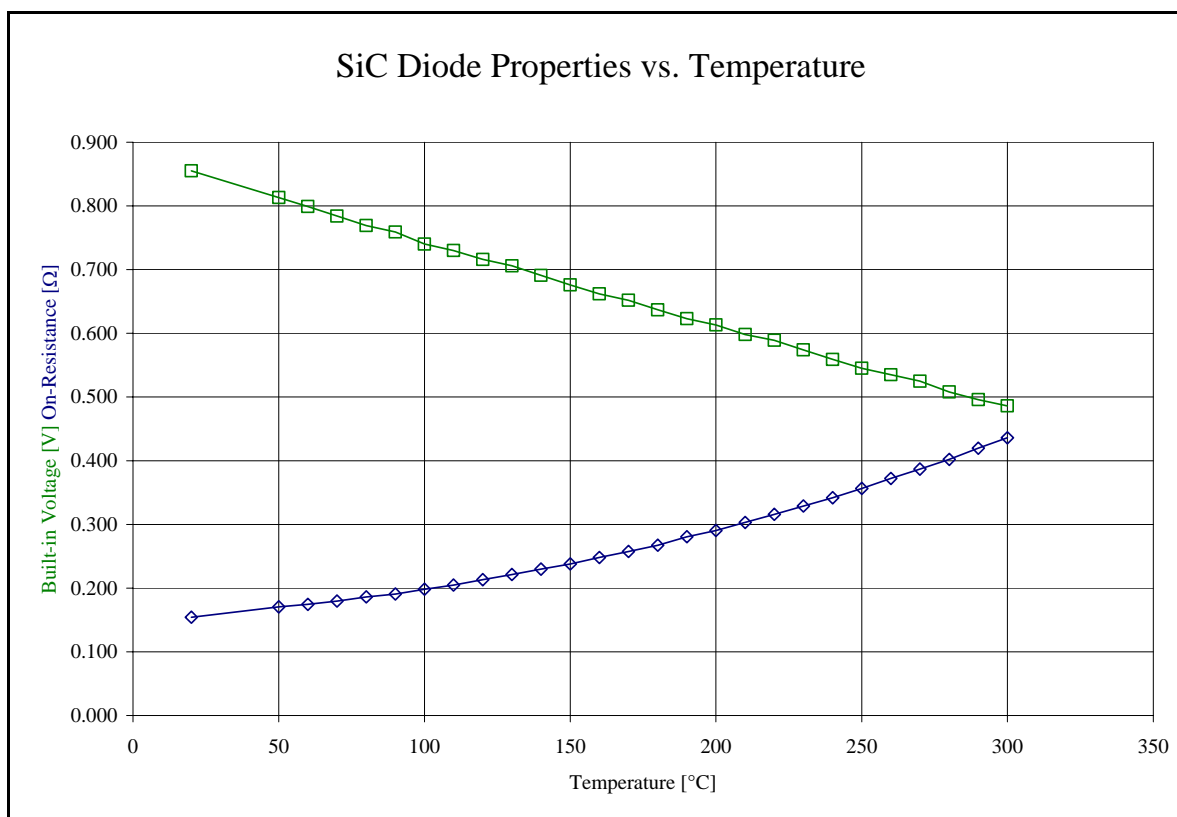


Figure 13. Temp Dependence of On-Resistance and Built-in Voltage of SiC Schottky Diode

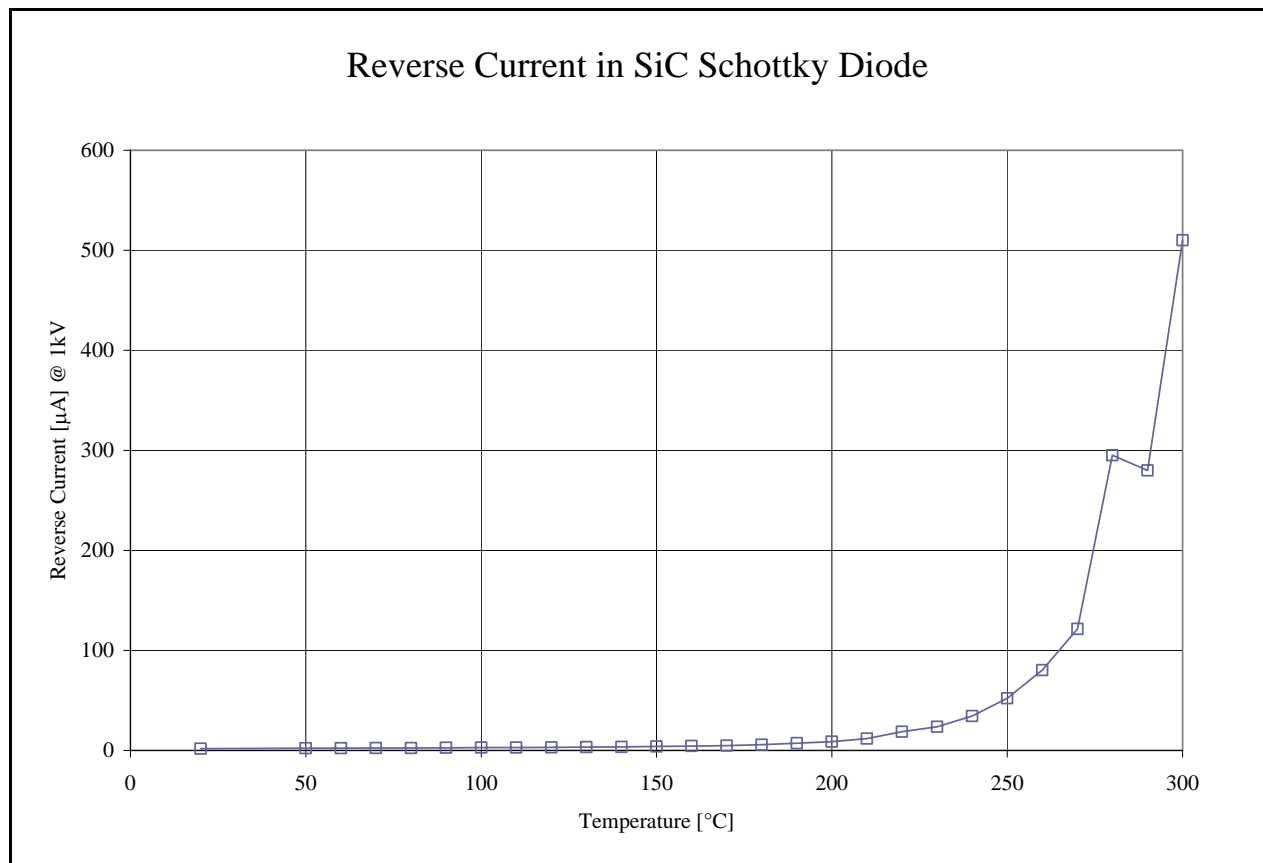


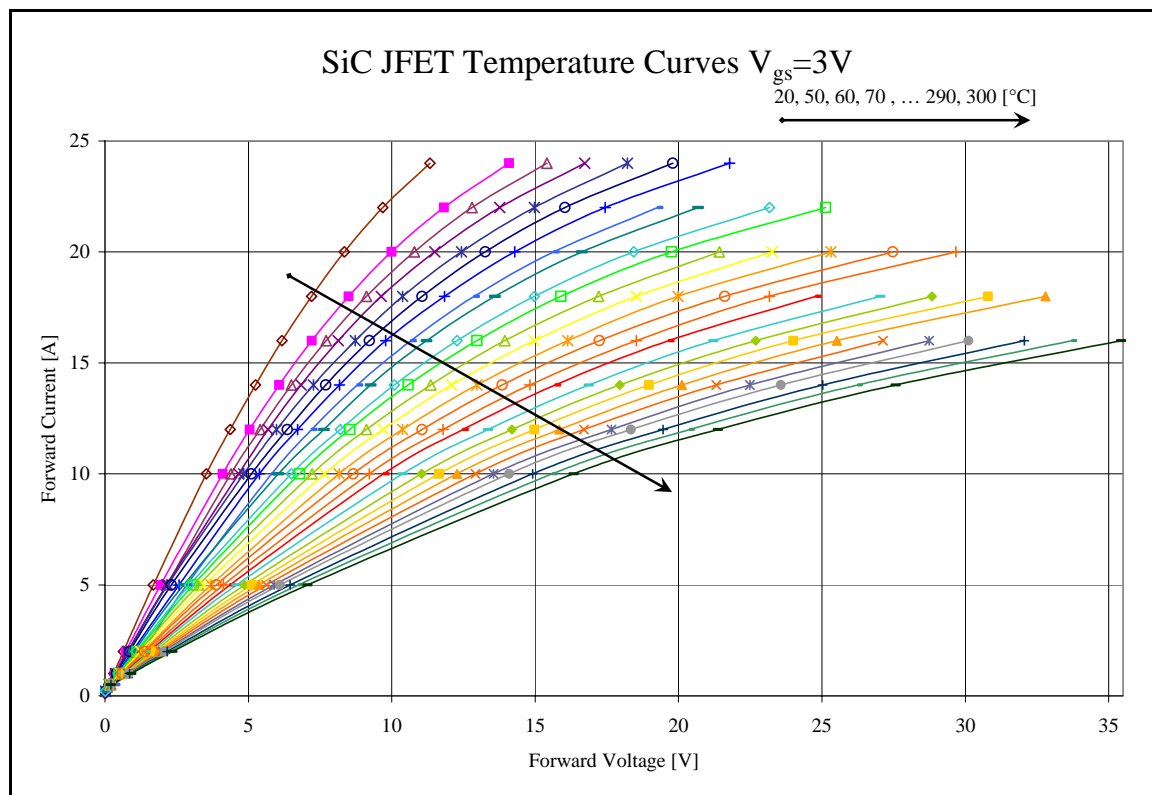
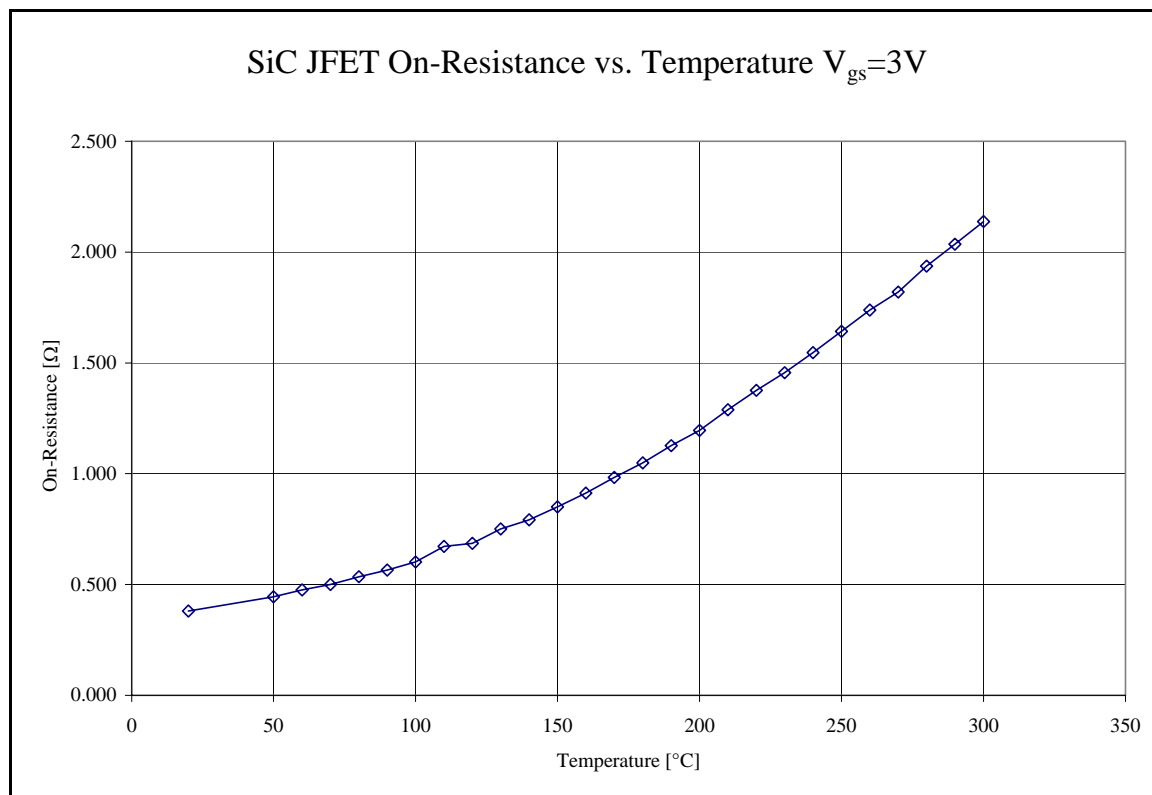
Figure 14. Temperature Dependence of Leakage Current of SiC Schottky Diode

Id [A] / T[°C]	20	50	60	70	80	90	100	110	120	130	140	150	160	170
0.1	0.007													
0.2	0.037	0.032	0.027	0.027	0.022	0.024	0.02	0.071	0.01	0.007				
0.5	0.134	0.149	0.159	0.159	0.139	0.154	0.178	0.33	0.178	0.168	0.188	0.188	0.193	0.198
1	0.3	0.339	0.374	0.369	0.371	0.393	0.437	0.755	0.452	0.481	0.496	0.52	0.54	0.574
2	0.64	0.725	0.799	0.799	0.808	0.857	0.955	1.336	1.009	1.077	1.121	1.184	1.248	1.331
5	1.683	1.941	2.151	2.154	2.186	2.317	2.581	2.85	2.747	2.95	3.079	3.27	3.455	3.7
10	3.538	4.11	4.388	4.667	4.838	5.111	5.385	5.814	6.049	6.496	6.784	7.216	7.663	8.164
12	4.369	5.048	5.411	5.69	5.983	6.359	6.72	7.214	7.636	8.205	8.537	9.116	9.7	10.38
14	5.25	6.073	6.498	6.84	7.265	7.7	8.178	8.799	9.263	10.09	10.57	11.36	12.09	12.97
16	6.171	7.211	7.714	8.139	8.7265	9.219	9.785	10.67	11.21	12.28	12.97	13.94	14.97	16.14
18	7.201	8.498	9.114	9.634	10.38	11.06	11.84	12.87	13.6	14.97	15.9	17.22	18.53	19.98
20	8.349	9.99	10.79	11.5	12.43	13.26	14.29	15.65	16.63	18.44	19.76	21.42	23.27	25.32
22	9.685	11.82	12.8	13.77	14.97	16.04	17.44	19.27	20.68	23.17	25.13			
24	11.33	14.09	15.41	16.73	18.22	19.8	21.78							
Ron [Ω]	0.381	0.444	0.476	0.500	0.535	0.565	0.601	0.672	0.686	0.751	0.792	0.851	0.912	0.983

Id [A] / T[°C]	180	190	200	210	220	230	240	250	260	270	280	290	300
0.1													
0.2													
0.5	0.198	0.22	0.212	0.212	0.215	0.217	0.21	0.222	0.22	0.212	0.208	0.208	0.203
1	0.593	0.628	0.657	0.676	0.711	0.74	0.764	0.789	0.813	0.828	0.862	0.886	0.916
2	1.385	1.465	1.546	1.609	1.702	1.785	1.858	1.932	2.015	2.073	2.171	2.256	2.352
5	3.875	4.125	4.364	4.584	4.872	5.126	5.37	5.624	5.902	6.107	6.454	6.747	7.065
10	8.657	9.214	9.717	10.38	11.04	11.65	12.28	12.92	13.55	14.09	14.92	15.6	16.34
12	11.06	11.79	12.48	13.36	14.19	14.97	15.85	16.7	17.66	18.34	19.46	20.39	21.37
14	13.85	14.82	15.7	16.87	17.95	18.97	20.12	21.32	22.49	23.57	25.03	26.25	27.57
16	17.24	18.53	19.66	21.22	22.69	24	25.52	27.13	28.74	30.11	32.06	33.72	35.43
18	21.61	23.17	24.79	27.03	28.84	30.79	32.8						
20	27.47	29.67											
22													
24													
Ron [Ω]	1.049	1.127	1.195	1.288	1.377	1.455	1.546	1.642	1.738	1.820	1.937	2.036	2.138

T [°C]	Id [μA]
20	0
140	0.03
150	0.2
165	0.1
180	0.05
200	0.3
210	0.7
215	1.2
220	2.6
225	3.8
230	6.2
240	9
245	10
250	8.2
260	5.4
270	3
280	1.9
290	1.4

Table 3. Measured Data for SiC JFET at Elevated Temperatures

**Figure 15. Measured Forward IV Temperature Curves of SiC JFET****Figure 16. Temperature Dependence of On-Resistance of SiC JFET**

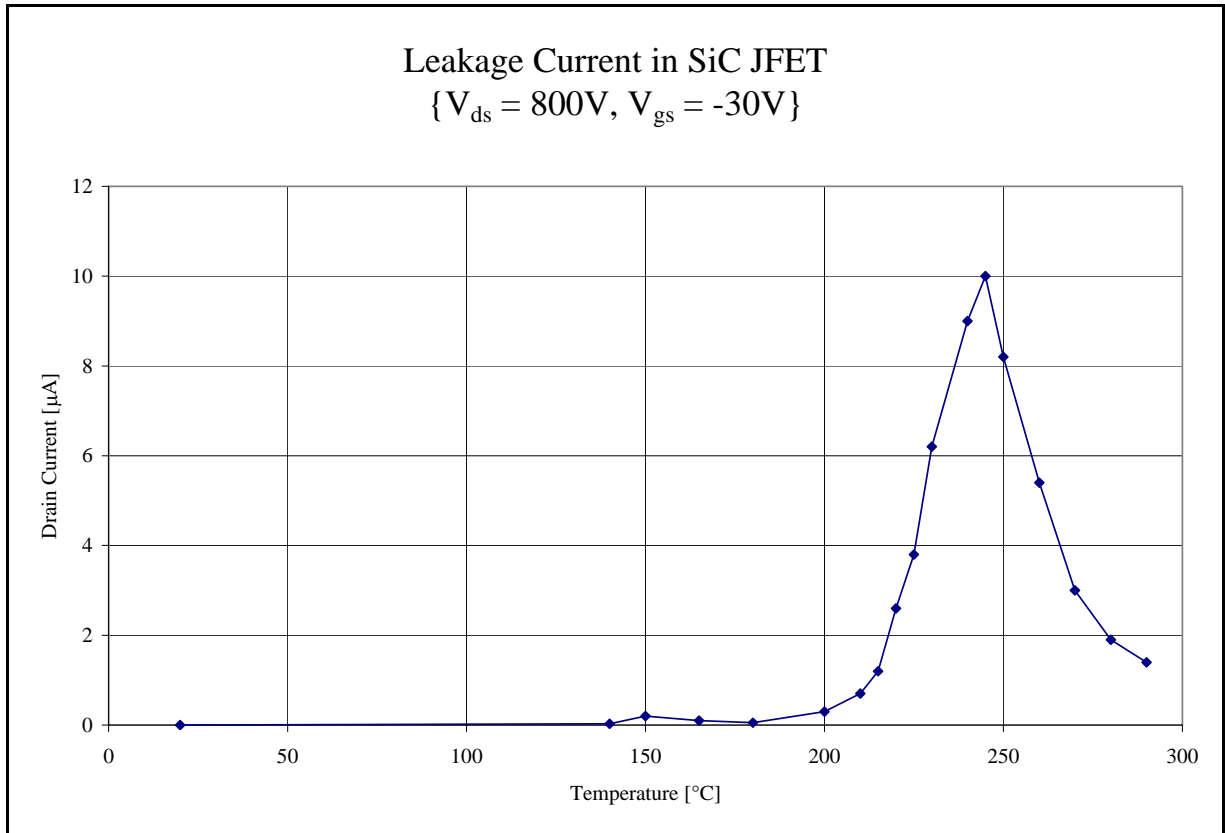


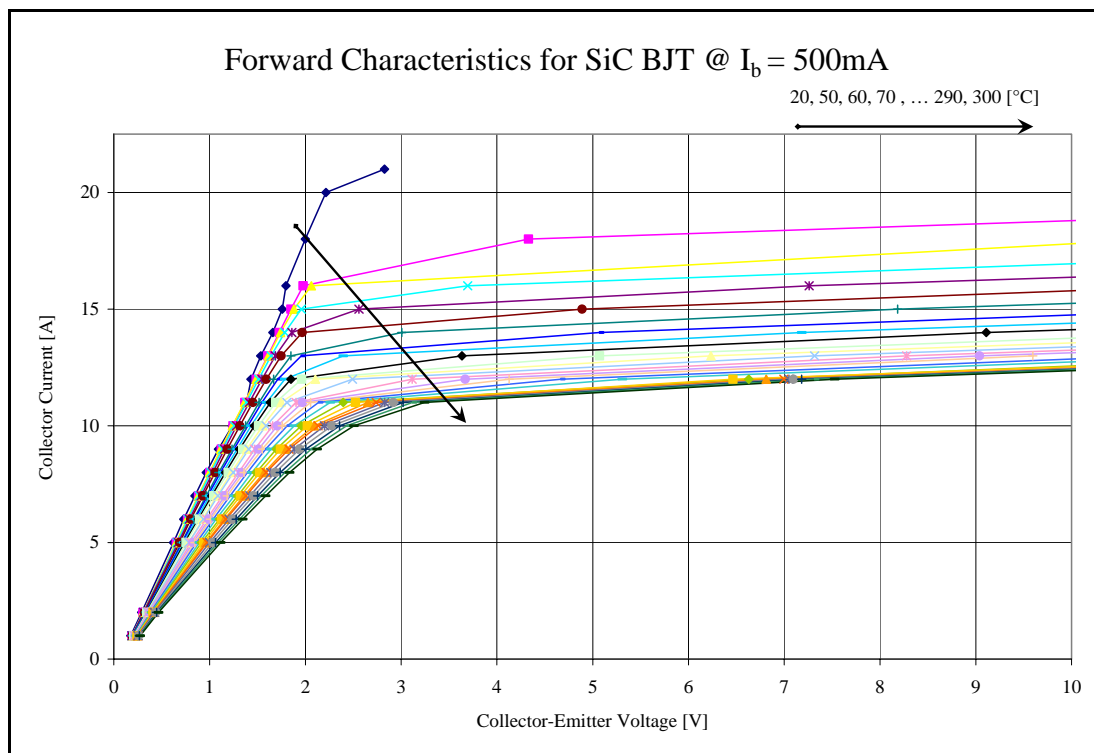
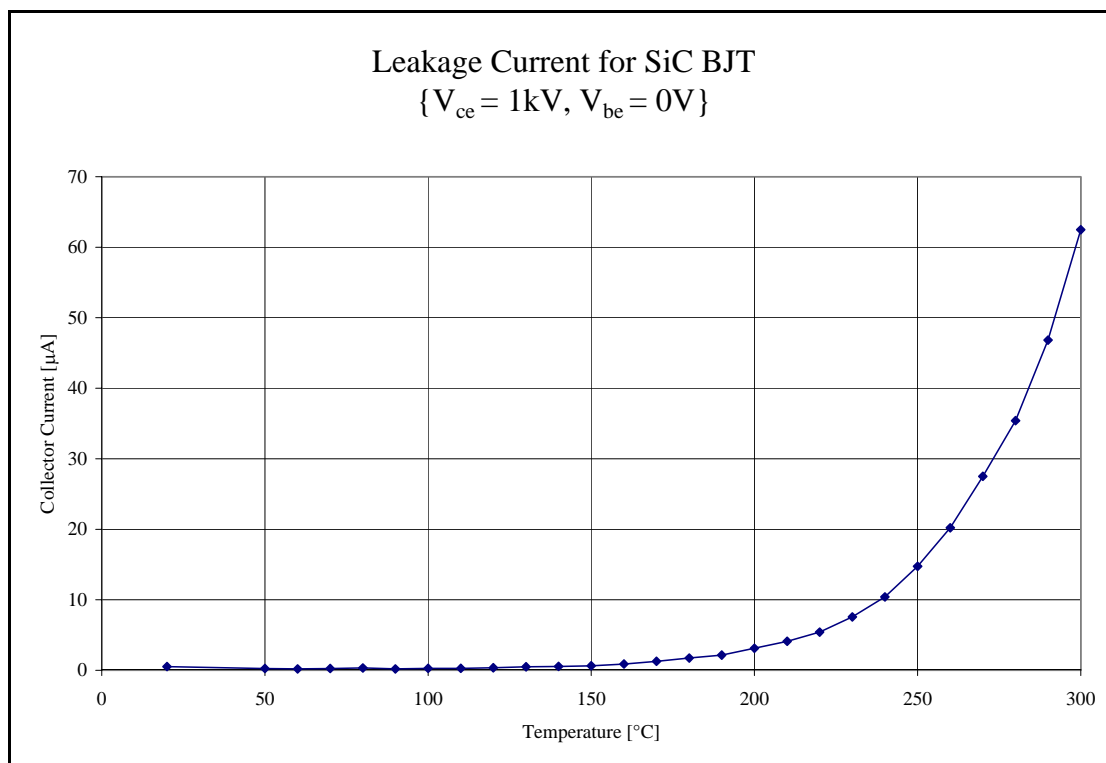
Figure 17. Temperature Dependence of Leakage Current of SiC JFET

The BJT showed diminishing forward conduction performance as temperatures were increased. Saturation voltages increased as the current carrying potential in the linear range decreased. The leakage current was indicated to be exponential with temperature. These effects were reversed once lower temperatures returned. The switching losses did not show consistent change over the temperature range we measured. Because of this observation, it was concluded that the switching losses of the BJT could be modeled as temperature independent. The highest measured values were chosen for both the turn-on and turn-off energies to be the constant switching energy loss for the converter model.

Temperature [C]	20	50	60	70	80	90	100	110	120	130	140	150	160	170
Vbe [V]	3.328	3.348	3.316	3.302	3.289	3.287	3.299	3.275	3.265	3.248	3.233	3.238	3.211	3.201
Ices [μ A]	0.5131	0.2398	0.2056	0.2471	0.3358	0.1956	0.2774	0.2872	0.3465	0.5001	0.548	0.6383	0.8882	1.263
VbeSat [V]	3.328	3.331	3.294	3.275	3.26	3.255	3.265	3.241	3.231	3.211	3.192	3.206	3.167	3.167
Ib=500mA														
1	0.176	0.188	0.188	0.188	0.188	0.193	0.193	0.198	0.203	0.208	0.208	0.212	0.212	0.217
2	0.291	0.305	0.305	0.31	0.31	0.32	0.33	0.33	0.339	0.339	0.344	0.354	0.354	0.364
5	0.623	0.652	0.65	0.659	0.672	0.686	0.706	0.716	0.73	0.74	0.755	0.781	0.784	0.808
6	0.73	0.769	0.764	0.774	0.789	0.803	0.833	0.842	0.862	0.882	0.896	0.926	0.938	0.969
7	0.847	0.886	0.882	0.891	0.911	0.93	0.965	0.979	0.999	1.021	1.043	1.074	1.087	1.136
8	0.965	1.001	0.999	1.013	1.033	1.057	1.096	1.114	1.14	1.165	1.194	1.228	1.248	1.302
9	1.092	1.121	1.116	1.136	1.155	1.184	1.233	1.253	1.287	1.311	1.346	1.385	1.409	1.473
10	1.238	1.243	1.238	1.258	1.282	1.316	1.375	1.399	1.433	1.468	1.512	1.556	1.59	1.658
11	1.385	1.368	1.363	1.385	1.414	1.453	1.516	1.546	1.595	1.634	1.69	1.746	1.807	1.902
12	1.433	1.487	1.487	1.512	1.546	1.592	1.668	1.712	1.785	1.849	1.961	2.105	2.491	3.114
13	1.534	1.609	1.614	1.643	1.687	1.746	1.849	1.956	2.396	3.636	5.072	6.234	7.316	8.278
14	1.661	1.726	1.741	1.785	1.858	1.966	3.006	5.072	7.182	9.109	11.6	13.02	14.31	15.41
15	1.758	1.849	1.88	1.956	2.559	4.889	8.183	11.65	14.29	16.58	18.68	20.1	21.42	22.59
16	1.797	1.976	2.063	3.695	7.26	11.4	15.56							
18	1.998	4.33	10.89	17.09	22.25	26.52	30.94							
20	2.215	18.68	26.69											
21	2.825													

Temperature [C]	180	190	200	210	220	230	240	250	260	270	280	290	300
Vbe [V]	3.201	3.184	3.17	3.167	3.167	3.148	3.143	3.131	3.121	3.116	3.118	3.111	3.109
Ices [μ A]	1.748	2.144	3.114	4.125	5.414	7.563	10.4	14.75	20.2	27.5	35.41	46.84	62.49
VbeSat [V]	3.158	3.14	3.123	3.118	3.114	3.084	3.074	3.05	3.04	3.021	3.011	2.987	2.967
Ib=500mA													
1	0.222	0.227	0.232	0.232	0.242	0.242	0.247	0.252	0.252	0.261	0.266	0.271	0.274
2	0.369	0.376	0.383	0.393	0.398	0.408	0.418	0.418	0.427	0.437	0.447	0.457	0.466
5	0.828	0.847	0.864	0.891	0.916	0.94	0.96	0.974	0.999	1.031	1.062	1.087	1.116
6	0.994	1.009	1.038	1.067	1.101	1.126	1.155	1.17	1.204	1.238	1.277	1.311	1.346
7	1.16	1.184	1.214	1.258	1.292	1.321	1.36	1.38	1.419	1.458	1.502	1.541	1.585
8	1.331	1.36	1.394	1.443	1.487	1.524	1.57	1.59	1.639	1.685	1.736	1.785	1.834
9	1.512	1.551	1.585	1.643	1.697	1.741	1.8	1.829	1.883	1.941	2.005	2.061	2.122
10	1.707	1.758	1.81	1.885	1.956	2.02	2.093	2.132	2.2	2.278	2.357	2.43	2.508
11	1.971	2.054	2.137	2.259	2.396	2.523	2.652	2.74	2.828	2.918	3.021	3.118	3.245
12	3.67	4.127	4.667	5.309	6.63	6.466	6.811	6.996	7.05	7.096	7.182	7.316	7.526
13	9.038	9.595	10.84	11.65	12.6	13.11	13.48	13.7	13.7	13.75	13.89	14.04	14.33
14	16.29												
15	23.42												

Table 4. Measured Data for SiC BJT at Elevated Temperatures

**Figure 18. Measured Forward IV Temperature Curves of SiC BJT****Figure 19. Temperature Dependence of Leakage Current of SiC BJT**

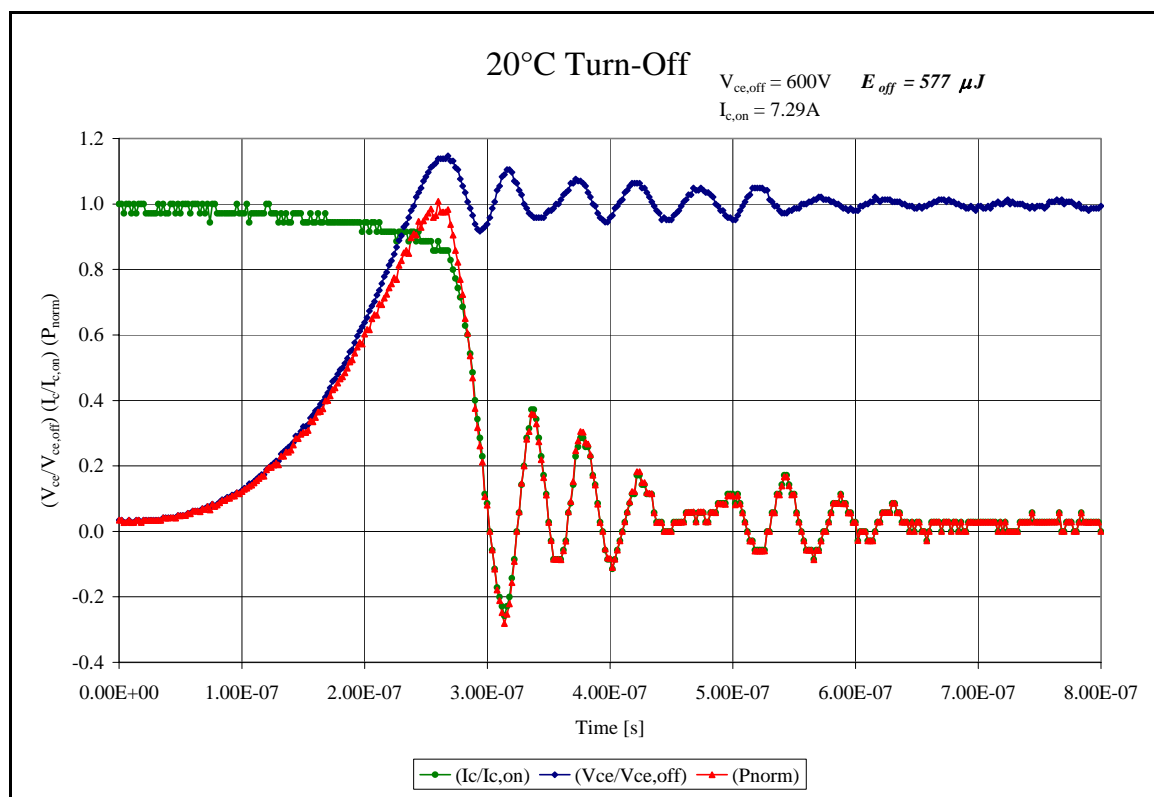


Figure 20. Normalized Turn-Off Characteristics of SiC BJT at 20°C

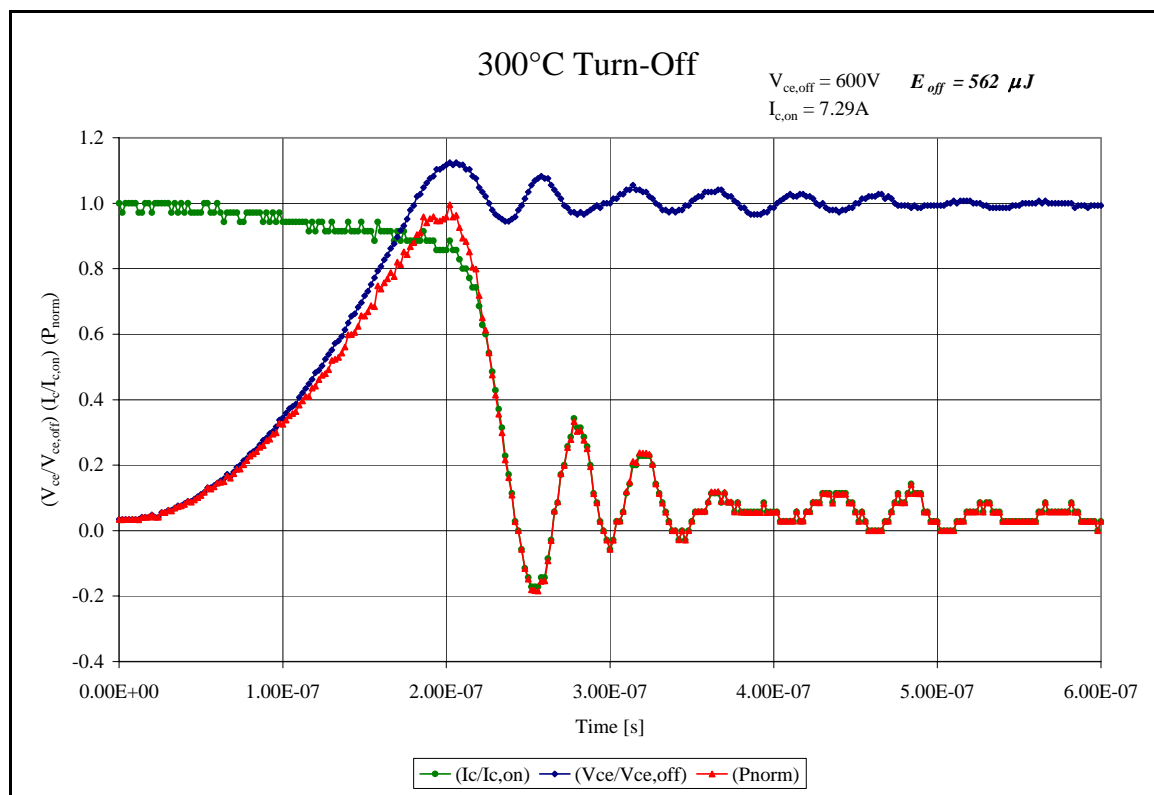


Figure 21. Normalized Turn-Off Characteristics of SiC BJT at 300°C

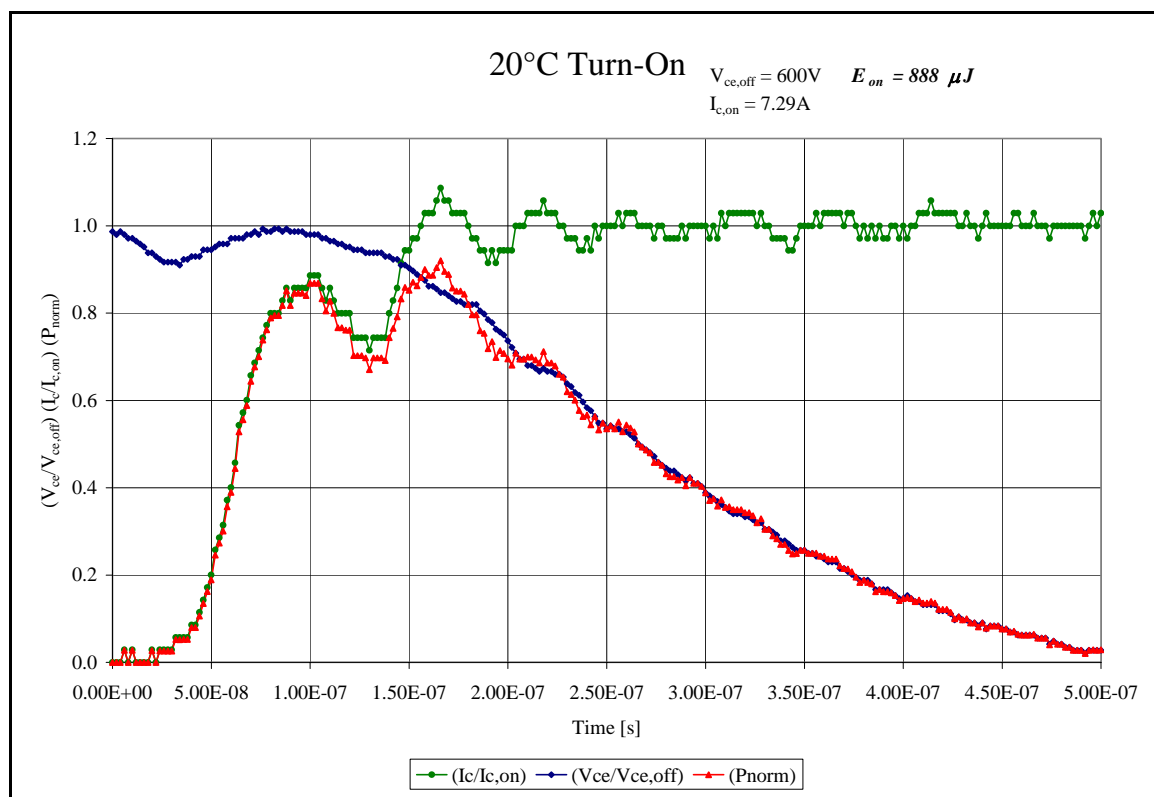


Figure 22. Normalized Turn-On Characteristics of SiC BJT at 20°C

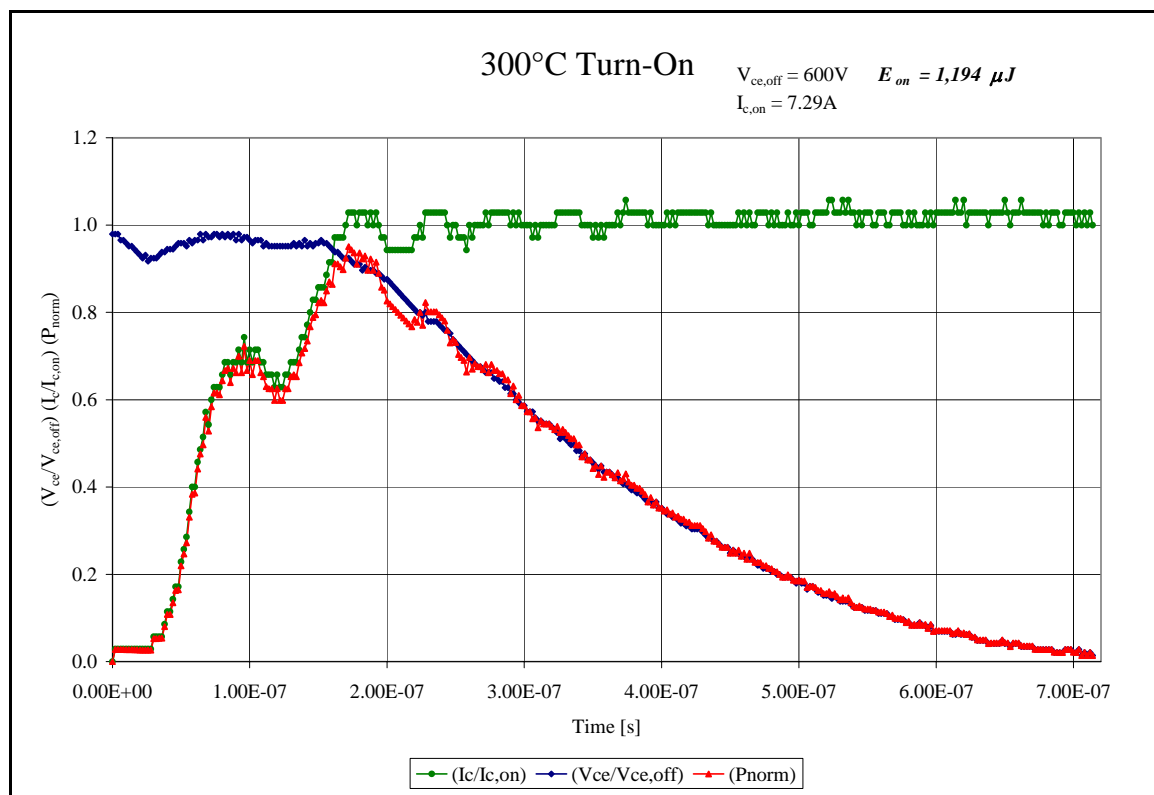


Figure 23. Normalized Turn-On Characteristics of SiC BJT at 300°C

The data collected was used to design 480Vrms inverter blocks using both SiC BJTs and JFETs with SiC Schottky diodes as the free wheeling diodes. The inverter was modeled at various switching frequencies and temperatures. This allowed the calculation of the losses of the inverter block and applies those to the design of specific heat sinks.

5.5 Application of the Measured Data to an Inverter Design

5.5.1 Inverter Modeling

To determine the losses in an inverter, one focuses on the performance of a single device as it operates throughout the various modes (current and voltage conditions) in the particular application. The energy losses in a device are the product of the current flowing through the device and the voltage across the device integrated over a convenient period of time, a 60Hz output cycle in this case. Portions of the current and voltage curves during the time period represent the conduction mode and portions represent the switching (turn-on and turn-off) mode. These modes are analyzed separately since they represent different types of physical events and the data necessary for their calculation are different. For the conduction mode, the static information (see the I-V curves given earlier) is used; for the switching mode, the dynamic information from the double-pulse tests is used.

The actual computations were carried out using a model in MATLAB script. The value of the current going through a switch was determined at an instant and multiplied by the voltage drop across the switch at that instant to get the energy loss for a short increment of time. The losses for all of the time increments over the 60Hz cycle were then summed up get the total conduction energy loss during one complete cycle. The total conduction energy is then averaged over that cycle to get the average conduction power loss. For the switching losses, the measured switching loss data is scaled according to the DC bus voltage and current in the switch, as found in the inverter during each switching event. The conduction loss for the freewheeling diode is done the same way as for the switch, but it is conducting at exactly the opposite time.

The measurements taken in characterizing the 1,200V BJT, JFET, and Schottky diodes were used to directly model 480V three-phase voltage-source inverter blocks. Also data measured by the University of Tennessee for a previous project with Peregrine was used to model a MOSFET inverter block at 480V. A comparison was made between the SiC-based inverter blocks and commercial silicon IGBT inverter from Semikron, SKiiP 342GDL120-4DU. Assumed conditions for the inverter were as follows: 100kVA rating, unity displacement power factor, unity modulation index, and a current density of 67A/cm² for each device. Table 5 below shows the total losses in watts per switch (and associated free-wheeling diode) in the inverter for different devices, temperatures, and switching frequencies. This data is plotted in Figure 24.

f _{pwm} [kHz]	Si IGBT	SiC BJT			SiC JFET			SiC MOSFET	
	125°C	125°C	200°C	275°C	125°C	200°C	275°C	125°C	175°C
1	101.4	79.7	93.3	115.1	125.6	193.7	307.7	100.3	110.7
5	237.2	140.3	153.9	175.7	140.0	208.1	322.1	122.4	132.8
10	406.9	216.0	229.7	251.5	158.1	226.1	340.1	150.0	160.4
20	746.4	367.6	381.2	403.0	194.2	262.2	376.2	205.3	215.7
50	1764.9	822.1	835.7	857.5	302.4	370.5	484.5	370.9	381.4

Table 5. Total Losses (watts) per Switch in 100kVA, 480V Inverter

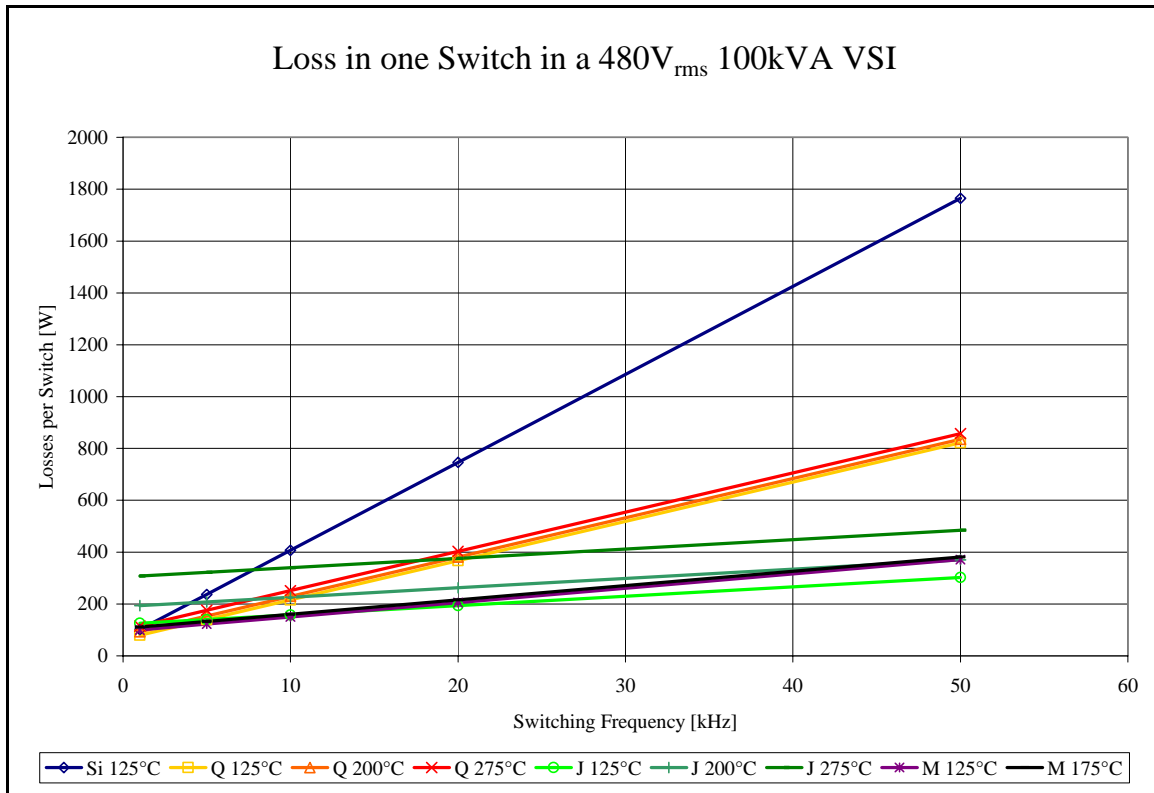


Figure 24. Total Losses (watts) per Switch in 100kVA, 480VAC Inverter

5.5.2 Losses in 480VAC Inverter Using 1,200V Devices

It is clear from Figure 24 that the improvement from using SiC devices, and the selection of the appropriate type of device, is a function of the application. That is, the results are a strong function of temperature and switching frequency. In general, SiC is more beneficial where high temperature and high frequency are required. Below 5 kHz switching frequency, the SiC BJT gives the lowest losses per switch in a three-phase voltage source inverter. From 5 to 20 kHz, the SiC MOSFET gives the lowest loss per switch in the inverter. Above 20 kHz, the SiC JFET has the lowest loss per switch. These losses are only for the inverter block with switches and freewheeling diodes; consideration would need to be given also to gate driving losses, particularly where the device is current gated (BJTs).

At low frequencies there is modest benefit to using SiC; however, once the switching frequency is increased to the 5 to 10 kHz range and above, the benefits of using SiC greatly increase. This shows that using a SiC MOSFET at a switching frequency of 5 to 20 kHz would be the best in a 480VAC inverter. With that, the junction temperature of the MOSFET can be elevated to the 175 to 200 °C range, giving a much more compact design without a great increase in losses.

Finally, it must be emphasized that any comparison of SiC devices at this early stage to silicon devices, which have undergone improvement and optimization over a 20-year period, is not necessarily appropriate. SiC devices will undoubtedly get better in all respects. The SiC MOSFET is a good example. As seen in Table 5, at 1 kHz, where the conduction losses are the primary loss mechanism, the SiC MOSFET had virtually the same total loss as a silicon IGBT which it may replace. But the SiC MOSFET has loss-producing regions other than the blocking layer which still dominate the overall device forward resistance. These will be minimized over the years ahead through better design and processing techniques. The bottom line is that SiC devices will get substantially better and outperform standard silicon by a wider margin in the future.

5.5.3 Losses in 4,160VAC Inverter Using 10,000V Devices

As indicated earlier, the objective of the overall project is to design and demonstrate an inverter that can operate at medium voltage (4,160VAC) using 10,000V SiC devices, rather than standard silicon IGBTs operating at 480VAC. This reduces dramatically the size of the power converter and associated filter, due to the 9-fold reduction in current, 10-fold increase in switching frequency and 2 or 3-fold increase in thermal gradient. This will also lead to a number of size and cost improvements for the overall energy system. The anticipated benefits are all enabled by SiC, which, as a wide band gap material, offers higher blocking voltage, shorter switching times and higher operating temperature compared to silicon.

There is absolutely no doubt that SiC devices will eventually deliver these benefits. SiC devices fabricated in prototype form have actually demonstrated the necessary voltage, switching frequency and temperature. And progress is being made toward better and better prototypes SiC devices under the sponsorship of DARPA, the Navy and others. The organizations developing the necessary high voltage devices include Cree, Northrop Grumman, Purdue University and United Silicon Carbide. This outcome is not a matter of "if", but rather "when".

However, the higher voltage devices were not available during the project for testing without a significant investment that is not possible in a Phase I SBIR project. Therefore, the characterization of, say, 10,000V devices was not possible. Peregrine had intended to estimate the benefits of SiC in medium voltage inverters by (1) extrapolating from data the team measured with 1,200V devices and (2) by evaluating data available from the literature and suppliers. After considerable effort to derive quantitative loss information for a SiC-based inverter at medium voltage, the team has elected not to present it. It is not believed to be sufficiently reliable to publish.

As for extrapolation from the measured data for the 1,200V devices, the team could find no clear theoretical relationships to enable this. There are a variety of relationships given in the literature, but it is not clear they fit the circumstances and the published data for real high voltage prototype SiC devices is not consistent with any theoretical extrapolations. An extrapolation from 1,200V to 10,000V is just too far. In addition, scientists in the field were not encouraging in the team's attempt to carry out such extrapolations.

As for the use of published data alone for high voltage devices, there is too wide of a spread among the data to give any comfort that the data represents a proper baseline. In fact, given the numerous variables involved – device structures, doping levels, and so on – it would be incredible if the published information for a variety of prototypes from different suppliers did follow a systematic relationship.

The result is that the team must fall back on basic theory and the fact that the fundamental physics are simply better for SiC than for silicon in this application. The physics of silicon is such that today, after decades on the market, there is still no silicon device that can be used in a simple, 6-device, three-phase VSI inverter that operates at 4,160VAC. Special power topologies are needed, such as (1) cascaded inverter blocks with many more IGBTs, (2) multi-level inverter with series IGBTs, or (3) current source inverters with series GTOs. All of these have much lower switching speeds than SiC devices and none can be operated above 125°C. The reduction in overall losses in a 4,160VAC inverter could not be less than a factor of two or three with mature SiC devices, compared to silicon devices.

Is the basic premise - that the necessary SiC devices will be available in the near future - true? A year prior to this writing, Cree supplied 4,500V SiC GTOs to Kansai Electric Company for a 300°C inverter. These are sufficient for an inverter that operates at 2,300VAC, one of the three standard medium voltage levels used in industry (the others are 4,160VAC and 6,500VAC). In addition, DARPA currently is funding three organizations to develop 10,000V MOSFETs for a high frequency transformation system for use on future aircraft carriers: Cree, Northrop Grumman and Purdue University. The PI has visited all three of those organizations and discussed the DARPA program manager, Ms Sharon Beerman-Curtin. The Cree and Northrop Grumman devices have been fabricated in prototype form and the Cree devices are expected to be available to the DARPA project during the next several months of this writing. Thus, it

seems to be a certainty that medium voltage, SiC-based inverters could be available to the energy business during the next several years, if DOE would support this effort.

5.6 Thermal & Packaging

5.6.1 Need for High Temperature Packaging

In general, power electronic devices made from SiC have two basic advantages over their silicon counterparts that lead to higher converter efficiency and lower cost. These advantages are (1) lower losses due to lower specific on-resistance and faster switching, and (2) higher operating temperature. The first advantage gives lower total losses. The second advantage increases the die-to-ambient temperature difference which drives the heat from the device. If the temperature difference is higher, less heat transfer surface is required, reducing the quantity of material in the heat sink and airflow requirement. Taking advantage of SiC's ability to operate at higher temperatures to reduce the amount of cooling material (and cost) is the focus of this section and the next.

The key boundary conditions in the thermal problem are the maximum permissible temperature of the device (125°C for a standard, silicon IGBT) and the temperature of the ambient air at about 50°C. Although detailed thermal calculations must be done for specific designs, one can rough out certain relationships using just the boundary condition information. As just noted, the maximum overall temperature difference for driving the heat from the device is about 75°C. If the designer increases the permissible die temperature to 200, 275 and 350°C, he increases the overall temperature difference by factors of two, three and four. A competent designer can translate those into reductions in heat removal material by similar factors. Again, this is not a precise analysis, but the relationship is as dominant as this gross analysis would suggest. When combined with lower losses from the SiC devices, the overall size reduction can be dramatic.

Today, all power electronics designers are pushing the limits of air cooling, which is far and away the lowest cost and most reliable method for cooling power semiconductors. Air cooling also leads to the smallest size if the entire cooling system is considered, including the secondary cooling system and all auxiliary components. Note that even a liquid system may still ultimately require air cooling hardware. Thermal designers already have developed heat sinks with clever fin geometries to maximize effective fin area and they know all about maximizing surface convection coefficients through turbulence and high air mass flow rates. The designer can also put exotic materials with high thermal conductivities in the thermal path between the die and the fins. But the heat flux achieved in the thermal management system will still be limited at the air interface by the fin area, convection coefficient and temperature difference, all of which have hit their maximums with standard silicon devices. If, on the other hand, if the device temperature is allowed to increase substantially by using SiC, the surface gradient can be increased by factors of two, three and four, thus enhancing and re-vitalizing the potential of air cooling.

Early in its work on SiC applications, Peregrine mistakenly believed that at least the major power semiconductor suppliers, who design and fabricate silicon devices today, would be working hard to get ready for the introduction of SiC or other wide band gap devices. They would then have or be nearing design solutions for high temperature operation. However, all prior work was found to be lacking or highly fragmented. Peregrine needed to take on the role of an integrator by pulling together the technologies of others and filling in any missing pieces with its own original work.

Micro processors for computers, games and other applications are limited in their clock speeds by cooling techniques also. While there are some differences in the thermal management problem, the packaging solutions do overlap to some extent. Therefore, Peregrine has looked into some of the thermal solutions in the IC industry, whose design problems have not traditionally overlapped those in power electronics.

Finally, by way of introduction, considerable effort has been expended by some to develop SiC packaging at 500°C and even 600°C, primarily for sensors that are used in or near various types of engines – jets, rockets and reciprocating engines. Those applications push the frontiers of materials and processes to the limit. However, those temperatures do not seem necessary for most power electronics applications,

certainly not for distributed and renewable energy. A much more feasible and practical limit is 300°C, which is adequate to achieve the objectives of this project.

5.6.2 Semiconductor Packaging Today

The basic connections and substrates in a state-of-the-art power semiconductor package are shown in Figure 25. Starting at the top of the stack, the current flows to the source through wires bonded to the top of the die. Generally the wires are made of aluminum and sonically welded to the top of the die, which have small metal pads to provide connection points. Multiple wires will generally be used not only to distribute the current more evenly over the die area, but also to reduce stray inductance. Most undesirable voltage perturbations are the result of the interaction of inductance and capacitance. The layering within a semiconductor design makes it impossible to eliminate capacitance, but the inductance can be minimized. It can easily be shown mathematically that the spreading of the current over multiple paths reduces the stray inductance. The gate drive circuit will be connected to the gate access points on the top of the die by its own wires and wire bonds in a similar way.

The surfaces of the die, as delivered by the fabricator of the die, are metallized to facilitate bonding. Bonding techniques and materials are a key ingredient to device packaging. The die is soldered to the next substrate, which must be electrically conducting in order to provide a current path out to the external electric circuit, that is, the load. This material will generally be a metal, such as copper. That substrate is then soldered to another substrate which is generally not electrically conducting, so that the electrical portions of the package are isolated from the outer non-electric portions. In most device packages (e.g. IGBTs) the outer materials of the package are not energized electrically, but in some others (e.g., SCRs) they might be. The non-electrically conducting material might be a ceramic, such as aluminum oxide (Al_2O_3) or aluminum nitride (AlN).

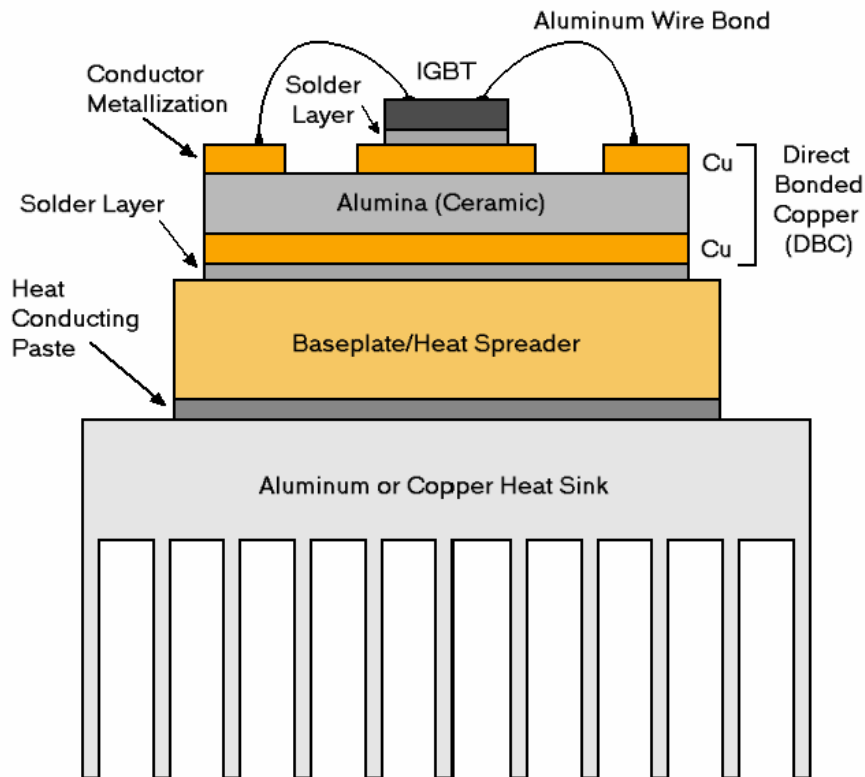


Figure 25. Typical Semiconductor Packaging Today

The next and final required substrate of the device package can be made of any material with high thermal conductivity – usually copper or aluminum. This provides a durable surface on the bottom and acts as the base plate which is attached to the heat sink.

The entire stack is then generally surrounded by a plastic enclosure with appropriate electrical leads protruding out for connection to the external circuit, and the semiconductors themselves are potted in a gel-like silicon substance to protect them from environmental exposure. That completes the overall semiconductor package, which is now a tightly integrated unit. It can be used by the converter designer or fabricator in this form.

When installed in a converter, the integrated unit will be attached to a heat sink made of a material with high thermal conductivity, most often aluminum or copper. This attachment usually involves wiping a heat conducting paste over the area of attachment and bolting the semiconductor package to the heat sink. The bolts will be spaced appropriately to distribute the bonding pressure uniformly over the attachment area and then torqued down to a specified pressure which minimizes the thickness of the paste (as it has relatively low conductivity), but still fills in all anomalies in the two surfaces so as to form a heat path filled completely with solid material.

All of the substrate and bonding materials were selected with several characteristics in mind: high thermal conductivity, matching coefficients of thermal expansion (CTE), and the capability of being bonded in high volume fabrication processes. Unfortunately, not all of these characteristics are present in one material so compromises are necessary. In a mature power semiconductor package, the dominant mechanisms for failure are de-lamination of substrates and detachment of wire bonds, both caused by thermal cycling. Due to the mismatch in CTEs of the die and the next substrate (often copper), an intermediate layer with an intermediate CTE might be inserted. The thermal cycling problem is accentuated if the die temperature oscillates through a very wide range, as will be the case with SiC devices.

The upper temperature limits on key components, such as the solder and plastic enclosure, might only be 200°C or so in a standard package, since with the 125°C limit of a silicon die there is no reason to use higher temperature materials. In addition, the equipment necessary to fabricate semiconductor packages often has operating temperature limits which preclude fabrication much above 200°C. Figure 26 is a photograph of fully assembled IGBT packages ready for use in assembling a converter.



Figure 26. Typical Power Semiconductor Packages

5.6.3 Direct Bonded Copper

Special attention should be given to direct bonded copper, commonly known as “DBC”, because it has become the most commonly used substrate material in high power semiconductor packages. DBC is a sandwich with layers of copper (or aluminum) on both sides of a layer of ceramic; usually alumina (Al_2O_3) or aluminum nitride (AlN). The bonding between the copper and the ceramic involves a direct bond process without solder or brazing material, and is well understood and extremely effective. There are at least one-half dozen suppliers of DBC, including Curamic (Germany), Toshiba (Japan) and IXYS (U.S.). Prices are competitive and reasonable.

Because of the unique construction of DBC, this material can be used as both the conductor trace metallization and the ceramic isolation layer, as shown in Figures 25. The copper on one side can be etched in a process similar to the fabrication of an ordinary printed circuit board. That is, a designer, using one of the many available CAD tools, can lay out circuit traces on one of the copper sides, which will then be masked. The balance of the copper in that layer will be chemically etched away leaving only the desired copper traces to which components can be soldered. DBC is also thin, so it has reasonably high composite thermal conductivity, regardless of the type of ceramic used. The composite CTE of the overall sandwich is dominated by the ceramic, which is close to that of the device die, so DBC is effective in improving reliability by providing a reasonably good CTE match with the die.

In the context of high temperature packaging, DBC offers higher temperature capability than some other approaches because of the high mechanical strength of the direct bond between the copper and the ceramic. The DBC can withstand temperatures over 500°C before the copper layer starts separating from the ceramic. This makes DBC a prime candidate for use in a high temperature, high power electronics package.

Figures 27 and 28 show a six-device inverter module known as a SKiiP, a product of Semikron of Germany. This particular module is used in a power electronics product developed by an engineering team of the PI in a prior project. In addition to the power devices, it also contains gate drive circuits with diagnostics and protection, and a heat sink with fans. DBC is used in the module in the manner described above. The bottom copper layer of the DBC here is attached to an aluminum heat sink with heat conducting paste and bolts, also as described. This modular concept is precisely the approach being followed in this project, although the materials and processes used at 300°C are entirely different.

5.6.4 Elements of High Temperature Device Packaging

5.6.4.1 Introduction

High temperature packaging for electronics has become an active area for worldwide R & D. Major applications include consumer products with higher microprocessor clock speeds, automobiles, civilian and military aircraft, and deep-well petrochemical drilling. There has been an explosion in the development of new materials, geometries and processes which can contribute to this R & D under the monikers of micro or nano technology. The disciplines here are as complex as those pertaining to semiconductors and SiC. Again, the research is highly fragmented and is often being carried out for purposes entirely different than the packaging of power semiconductors. Peregrine has had to integrate several different technologies in developing high temperature device package concepts that are feasible.

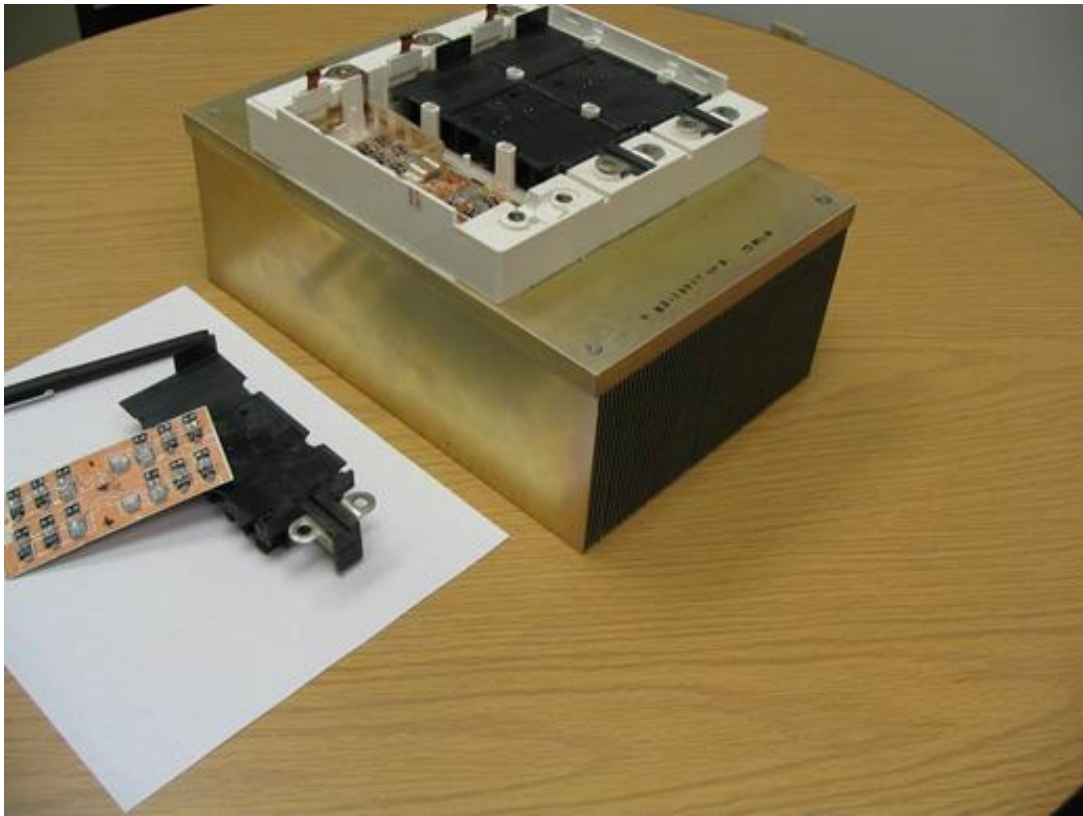


Figure 27. Semikron SkiP Inverter Module (Six Pack) Using DBC Substrates

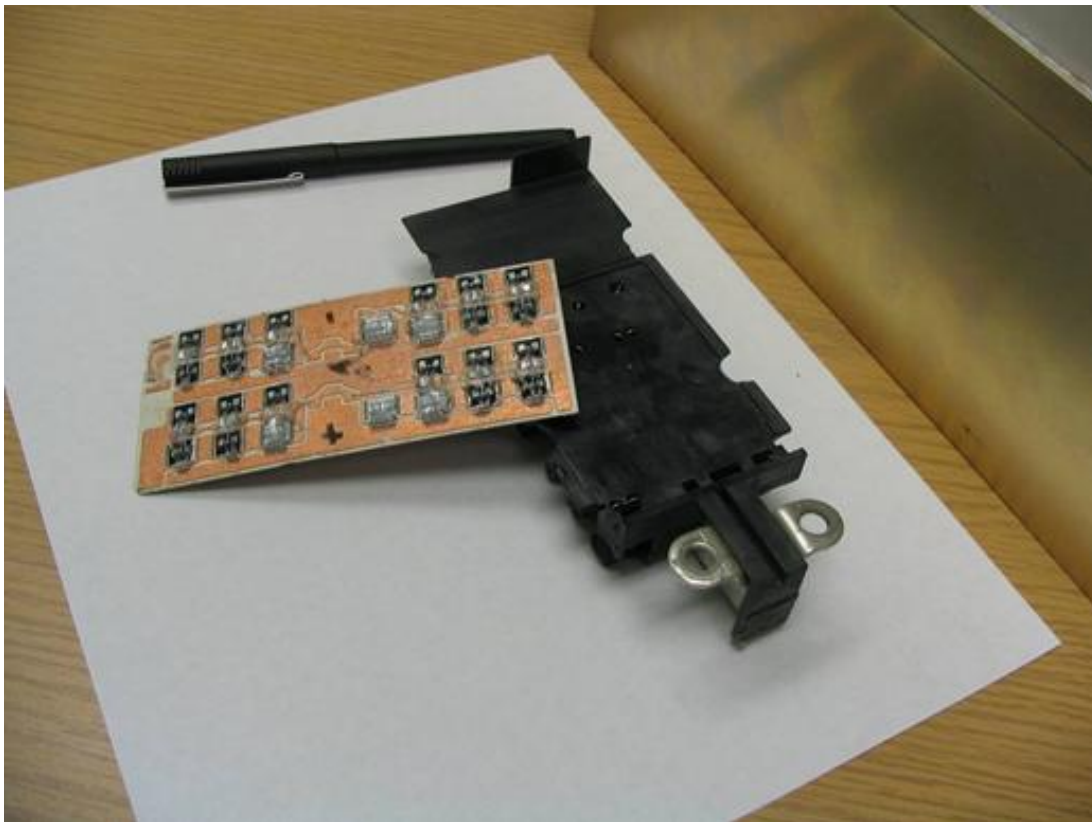


Figure 28. Semikron SkiP Inverter Module (Six Pack) Using DBC Substrates

As the designer increases the temperature of the device package from current levels, various temperature limits for its components are exceeded. One can systematically replace each limiting component with a higher temperature version as he increases the temperature; by the time he gets to 250°C or so all of the materials and processes will have been replaced. It would be straight-forward to design a package that can operate once or a few times at 300°C, but to withstand frequency thermal cycling between the highest and lowest temperatures associated with SiC is another matter. Achieving a close CTE match is even more critical than before, but adjacent materials must also have appropriate elasticity so as to absorb some differential movement without cracking.

A 300°C device package must be completely redesigned from scratch rather than merely changing out some of its components. The designer may integrate not just the device and adjacent substrates, but also a heat sink with a better CTE. This integrated unit can be extremely small and tailored specifically to wide band gap devices. A desirable feature would be the replacement of wire bonds with another substrate on top of the die to eliminate completely the bond wire de-attachment problem and to permit two-sided cooling. All of this is believed to be feasible in time, based on discussions with knowledgeable people.

5.6.4.2 Materials

Tables 6, 7, 8 and 9 summarize the properties of important materials to be considered in developing high temperature semiconductor packaging. These include materials which are currently used in state-of-the-art semiconductor package designs, but also additional materials, some of which are quite new. It is not likely that all potential candidate materials have been identified - too much is happening in materials research in the scientific community. With the development of composites, materials can actually be designed to meet specific objectives, such as matching CTEs. Note that the reported properties of most materials vary by a surprising amount due to differences in material structure (e.g. single crystal versus multi-crystal), manufacturing techniques and other factors.

Table 6 shows conductivity, which the designer naturally wants to maximize in a thermal package. The standout material is CVD (chemical vapor deposition) diamond, but this material is expensive and not shapable. It is usable only in thin layers for specialized purposes. SiC-C (diamond) and Al-C (diamond) composites are promising candidates from strictly a conductivity point of view. SiC itself has high conductivity, which suggests it might be used in the device package in ways other than as a semiconductor. SiC is actually straight-forward to make and the basic ingredients are extraordinarily common. SiC has been used for decades due to its hardness and luster (carborundum blades and jewelry). BeO has been eliminated from most designer's list of candidates, because BeO dust is highly toxic. Essentially all suppliers of civilian power semiconductors have ceased using BeO over the last ten years. The old standbys of copper and aluminum are still viable candidates in a high temperature package in places where CTE matching is not important.

Table 7 shows the CTEs for the same materials. CTE of a SiC die is about 3.7 ppm/K, which becomes the target for all other materials. Aluminum and copper are the standouts from a cost and conductivity standpoint, but they are among the worst possible materials from a CTE standpoint. In fact, virtually all power semiconductor problems today in CTE matching occur because aluminum or copper is being used somewhere in the package. This problem occurs with essentially all pure metals, so the larger temperature swings experienced with SiC devices motivate the designer to look harder look at ceramics, which in general have much lower CTEs. Composites show promise too.

The importance of CTE matching should be qualified. The objective is really to avoid excessive stress, which involves **strain** matching more than simple CTE matching. When a large temperature gradient is present, the designer might actually elect to have specified differences in CTEs in adjacent materials to match strain. In addition, elasticity is desirable to allow strain differences to be absorbed without inducing cracks. Solders and other bonding materials particularly should have significant elasticity. The interaction of all of the important material properties requires sophisticated thermal stress modeling.

Table 8 covers density, which is not a driver in all applications, but it is for some that Peregrine is currently working on, such as Army mobile power, where reducing weight is of some concern. It is also a major driver in aerospace applications for the same reason. One generally associates high density with high conductivity, but some of the ceramics and composites have surprisingly high conductivities without high densities.

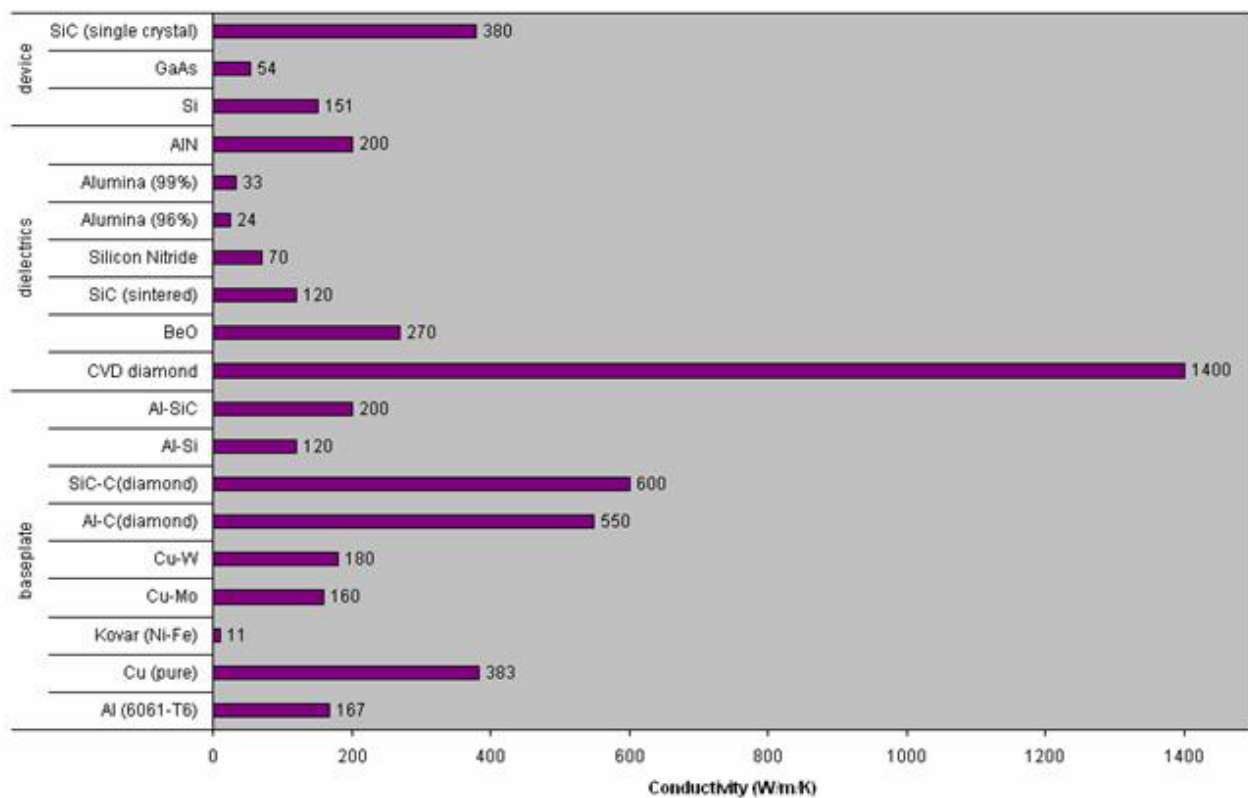


Table 6. Conductivity of Materials

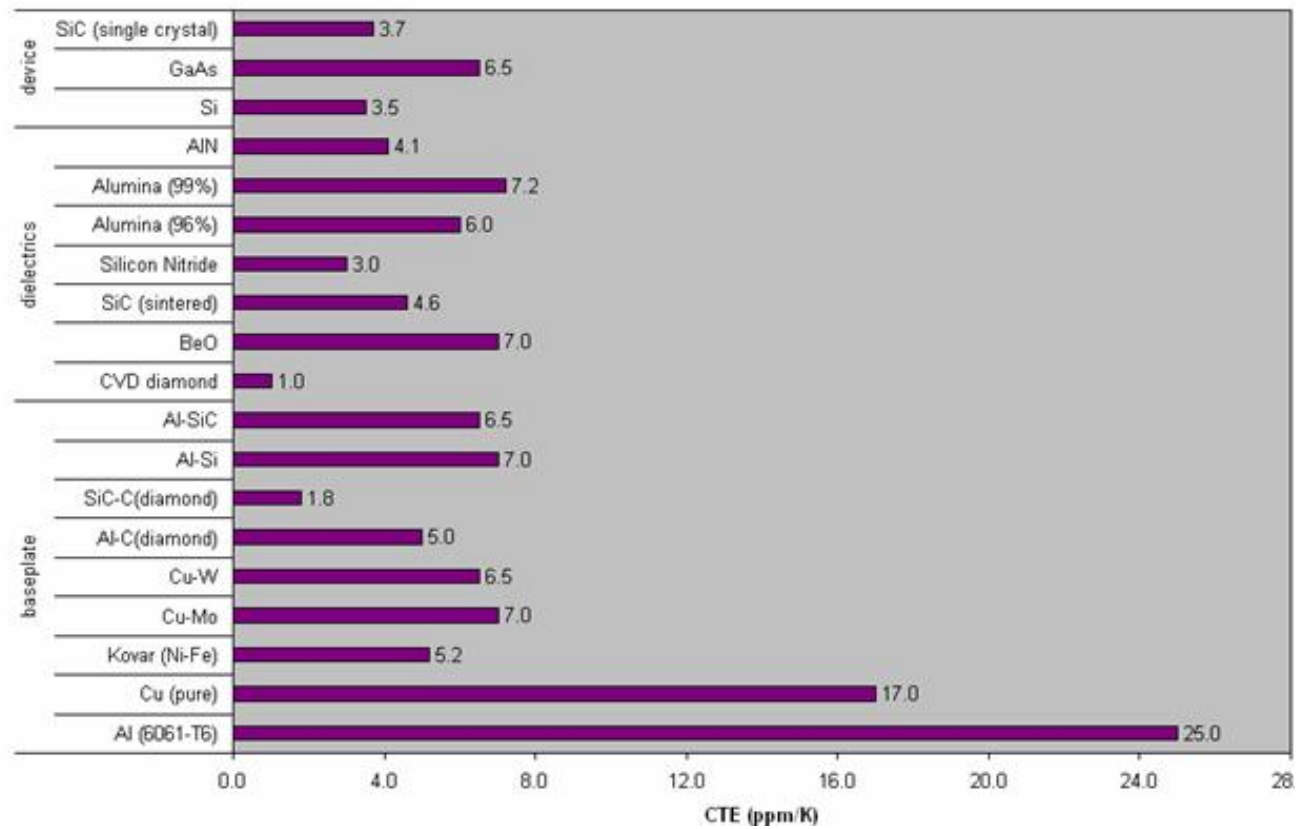


Table 7. CTE of Materials

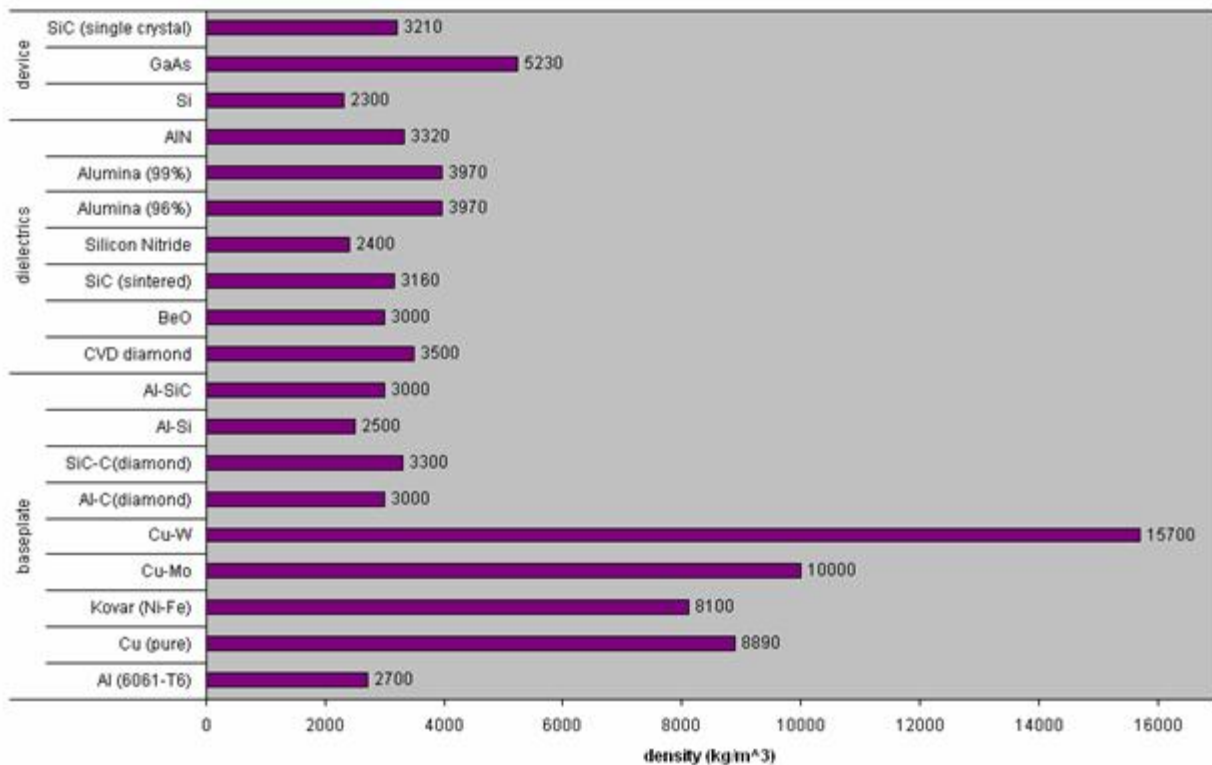


Table 8. Density of Materials

Material	Density <u>g/cm³</u>	Cost <u>\$/Kg</u>	Cost <u>\$/cm³</u>
Copper	8.9	18	0.16
Aluminum	2.7	2	0.06
Boron nitride	2.25	132-176	0.30-0.40
SiC particles	3.2	5.5	0.02
Disc C Fiber	2.2	15-100	0.07-0.48
Diamond particles	3.52	350-5,000	1.20-17.60
HOPG	2.53	1320-1760	3.30-4.50

Source: Presentation Materials from Carl Zweben (March 13, 2005)

Table 9. Cost of Selected Materials

Table 9 addresses cost to the extent information is available. This table is a reprint from a recent conference in high temperature electronics packaging attended by a member of the Peregrine team. The table is highly incomplete as it contains only those materials which are actually produced in volume and have a recognized price. Some of the important materials in the previous tables do not fall in this class and are not listed since they cannot be priced. Nor can the processes which would be used in fabricating device packages with these materials be priced. Still, with this incomplete information, some conclusions can be drawn. The primary reason for the widespread use of aluminum is obviously low cost. When ease of fabrication, physical toughness and reasonably high conductivity are coupled with low material cost, its use is no surprise. But the table also reveals the low cost of SiC particles which can be mixed with other materials as a composite. In fact, it can be mixed with aluminum to form AlSiC, a process that is 20 years old and has a reasonable existing production infrastructure. The AlSiC composite might have a lower bulk cost than even copper when used in a heat sink and its CTE is much more favorable.

After candidate materials are identified, a trade-off analysis must be carried out to select final materials. That is, an appropriate balance between conductivity, CTE, cost and manufacturability must be struck. The results of the trade-offs for this project are apparent from the packaging concepts discussed later. Why each material was selected will be discussed there.

One of the important conclusions from the thermal modeling in this project is that while high thermal conductivity is a plus, it is less important to the designer when the device can operate at 300°C than when it can operate at only 125°C, the case for standard silicon. A few degrees more or less in the stack of substrates have little impact on a final design. The total temperature differential across all material in the thermal path up to and including the material in the fins of the heat sink is small in most cases – only around 25°C - whereas the temperature differential at the surface to drive surface convection is about 225°C. The designer would happily give up thermal conductivity for a better CTE match or lower cost. If the absolute minimization of size is the only criteria, then the tradeoff might come out quite differently.

A composite can be viewed as a “designer” material. Here the designer can simply select different mixtures of materials to meet different objectives. If the designer prefers to tradeoff conductivity for CTE, he can do it. The CTE of the AlSiC composite can be reduced to approximately 6 while for AlC (diamond) it can be reduced to approximately 5. Obviously the resulting composite must still be manufacturable in volume, as it is for AlSiC.

5.6.4.3 Die Attach

Bonding and attachments represent a complex discipline that involve materials, processes and specialized machinery. They generally are developed in direct response to a specific application. The bonding and attachments for a state-of-the-art power semiconductor using silicon were covered above. The techniques employed now are well developed and highly competitive, but they must be reviewed again since they will be changed greatly in a high temperature package. Not only must they be able to withstand much higher temperature but they must be capable of bonding the new materials. Indeed, otherwise promising materials must be eliminated from further consideration if bonding is not possible. With some of the innovative materials, it is not at clear if effective and reliable bonding is possible in a semiconductor package. While thermal and stress modeling has been carried out in this project for several packaging concepts (discussed later), ultimately substantial experimentation would have to be carried out too.

The available types of bonding include diffusion bonding, diffusion welding, thermal-compression bonding, direct copper bonding (DBC), brazing, soldering and epoxy bonding. These will not be covered in any detail here, other than to give a few remarks about soldering, the current method for joining the die and substrates. Power semiconductors typically use solders which keep their integrity up to temperatures in the 200 to 225°C range, which has been acceptable to date since the device itself has been limited to 125°C. The most common solder, lead-tin eutectic, as well as the common leadless solders formulated to replace lead-tin fall in this range. Common hard solders, such as gold-tin and lead-silver-tin, have reflow temperatures up to 280 to 309°C, but even those are not adequate for a package with dies at 300°C. However, several, less commonly used hard solders are available which can be used at temperatures over 300°C. Two candidates meeting the temperature requirement are the gold-silicon eutectic, which has a reflow temperature of 363°C, and the gold-germanium eutectic, which has a reflow temperature of 356°C.

The large suppliers of solder, such as Indium Corporation of America, sell dozens of types of solder, including the two just named. Most of these suppliers will formulate a solder to specifications supplied by the customer. The gold-silicon eutectic is one of the solders recommended by Indium for high temperature packages in this project (Indium product designated #184) and is made up of 96.76 percent gold and 3.24 percent silicon. Gold sounds expensive, but it used throughout the electronics world where corrosion might be a problem. It is common to use gold in printed circuit boards. It does not lead to exorbitant cost, primarily because it is used in very thin layers, although the cost of a printed circuit board using gold is somewhat higher than for a printed circuit card with only copper.

One of the characteristics of high temperature solders is that they are harder and more inclined to crack under stress. This tendency needs to be taken into account when evaluating thermal and stress models of a packaging concept. More details will be given below when Peregrine’s recommended packaging concepts and associated thermal/stress models are described.

There are also a few other die attach materials which are not used traditionally with power semiconductors, but show some promise at high temperature. These include silver filled glass, which has a lower CTE and modulus of elasticity than gold-silicon solder, and sintered silver paste, which has been demonstrated. These were ruled out here because they are still in the research phase of development.

5.6.4.4 Topside Device Connections

There are several methods for achieving the topside connections to the power semiconductor device, however, the most common and most reliable at the moment is still the wirebond, which retains its place

as the state-of-the-art in industrial power semiconductor packaging. For high temperature packaging, the best option for the topside device connection is still the wirebond, but because of the extreme environment, more care must be taken to match materials to avoid failure by thermal stresses.

The state of the art for 125°C packages is to use aluminum for the wire material, bonding to aluminum pads on the device and bonding to copper, gold, or aluminum pads on the conductor substrate. The wirebond is ultrasonically bonded to these pads using a wedge bonder. There are several reliability problems on the topside of the device associated with bonding aluminum pads to aluminum wire. One of these problems is the erosion of the aluminum metallization layer on the device underneath the wire at the bond. This erosion is caused by the migration of the aluminum material (called electromigration) of the bond pad under the stress of high electrical current flowing through a small area. In pushing the semiconductor device to higher and higher temperatures, this problem will only accelerate.

There are other material combinations which mitigate this problem. One way is to use gold as the bond pad and wire material, instead of aluminum. Gold does not have an electromigration problem, but has the disadvantage of requiring lower current density as well as being more expensive than aluminum.

Another way to mitigate electromigration is to use ribbon instead of wire as the topside connection. The ribbon material is still ultrasonically bonded to the bond pad, but it has some key differences. First, because the ribbon is rectangular instead of round in cross section, a single ribbon can be used to carry current to the device instead of using multiple conductors. The rectangular cross section limits the stray inductance coming from the wire. The second advantage is that the perimeter of the bond is longer making the current density in the bond pad decrease and so decreasing the effect of electromigration.

Ultimately, the best combination is to have both bond pads and the wire be the same metal. Multi-metal combinations, such as aluminum bond pads with gold wire, can result in the formation of intermetallics which can decrease the reliability of the connection. Gold is better than aluminum because it does not have the problems with electromigration that aluminum has. Ribbon is probably the better choice over wire, but industry experience with wire is much more extensive.

5.6.4.5 Balance of Package

Besides the power circuit and associated electrical and mechanical connections, the balance of the package consists of the case, isolation mechanism, and thermal interface material, which are required to attach the package to a heat sink. Currently, most of this balance of package is made of organic material such as plastics which have a maximum temperature for use of less than 300°C.

The case in a 125°C package is usually made up of a thermoset plastic, sealed with epoxy. Plastic makes for an almost perfect case material for a non-hermetic package because it can serve as a structural material for supporting the conducting leads, but at the same time, is naturally electrically non-conductive, making separate, insulating feed-throughs unnecessary. For temperatures higher than around 250°C, the use of plastic as a case material becomes restricted by the maximum useable temperature of the plastic and epoxy.

The use of plastic in the case also drives the method of environmental isolation used for the package. By far, the most effective and least costly method of environmental isolation at 125°C is to pot the semiconductor array in a jelly-like silicon material. The use of potting material makes the infiltration of water and oxygen impossible, which reduces the likelihood of failure by corrosion. However, if the maximum temperature of the package is greater than about 250°C, the use of plastics, and hence, potting, becomes difficult or impossible.

The alternative to potting is to hermetically seal the package, that is, make the package airtight either by making the interior of the package a vacuum environment or, more likely, filling the interior with nitrogen or some other non-reactive gas. Hermetic packages are useful up to the highest temperatures which any semiconductor material can reach. The case material for a hermetic package will most likely be a metal alloy of low CTE, such as Kovar or Invar which are both alloys of iron. Metal matrix composites such as

AlSiC may also be used in applications where a light weight or heat dissipation through the case is required. The leads to the electrical circuit are usually electrically isolated from the case using glass feed-throughs. The package is then evacuated and a lid is brazed or soldered into place. It is likely that the 200°C package can be designed using a plastic case and isolated from the environment using a silicon based potting compound. The 300°C package, on the other hand, will probably have to be hermetically sealed using a metal case.

The final consideration for the balance of package is the thermal interface material used between the package module and the heat sink. For 125°C packages, a silicon-based paste is used as the thermal interface material. The paste is spread onto the bottom of the baseplate, and the fasteners are torqued down to evenly distribute the paste across the contact area with the heat sink. Like the silicon based potting compound, silicon-based thermal interface material paste is only useful to temperatures around 250°C. At temperatures above 250°C, the only thermal interface material which is practical to use is a graphite sheet material. This material is a commercial product and is made in various forms by several companies. One of these companies is eGraf, which sells the material specifically for use as a high temperature, thermal interface material.

5.7 Specific High Temperature Packaging Concepts

5.7.1 Analytical Methods

5.7.1.1 Material Selection

Obviously the methods selected must assist in answering the key questions. In this project, there are two primary areas of concern with the high temperature package, as enabled by SiC: (1) stresses from thermal gradients which would cause the package to fail and (2) overall thermal dissipation and the resulting size reduction from increasing the device temperature of the semiconductor power blocks. The materials which make up the semiconductor package impact both of these areas of concern.

The selection of materials for a high temperature package with air cooling is based on a combination of material properties: conductivity, CTE, modulus of elasticity, cost, manufacturability and maturity. Strictly from a stress standpoint, CTE is the most important, followed by modulus of elasticity. As noted above, conductivity is relatively less important with air cooling at the higher temperatures being considered since the surface temperature differential will be about 225°C in any case, while the temperature drop across the material in the substrate stack and heat sink will be only 25°C or so. The relative insensitivity in the problem to material conductivity is caused by the dramatic increase in overall temperature differential from the use of SiC. The advantage here is that the designer can select from a longer list of materials with CTEs that more closely match the CTE of SiC and can compromise the conductivity more than he would with a temperature cap of only 125°C and maximum overall differential of 75°C.

Where materials have similar advantages, their selection will be based on price and maturity. There are a significant number of innovative materials being developed in the scientific community, particularly composites. Their properties are unconfirmed in some cases and their practicality in a cost sensitive world has not been evaluated. Peregrine has taken a hardnosed, conservative position on materials, but nevertheless believes that significant improvement in materials will occur during the five years.

5.7.1.2 Package Evaluation

Potential package designs were evaluated for tensile stress in the substrate layers using two dimensional FEA simulations. The two dimensional models are extremely simplified to isolate only the thermal stress contributions of the die and the solder and substrate layers directly underneath the die. The baseline stress analysis is for a 125°C package made from alumina-based DBC, which is the current state-of-the-art among semiconductor packaging companies such as Semikron and Powerex. This baseline stress profile is compared to a variety of materials in both 200°C and 300°C package designs. Suitable packages are ones with stress patterns similar in magnitude and pattern to the baseline model.

Since the most common package failure is the de-bonding of various layers in the package, the tensile stress is thought to be a good predictor of package failure. There is no good way to quantitatively predict package reliability through either S-N (stress vs. number of cycles to failure) curves or through physics of failure models. The S-N curve is the traditional way to predict mechanical fatigue lifetime. Unfortunately, the semiconductor package includes many different materials and alloys which do not have published S-N curves. Solder alloys are notorious for following non-linear failure patterns, as well as having failure rates dictated by the vagaries of imperfections in the bond layer for individual packages. Even seemingly straight-forward parts of the package, such as the substrate and metallization layers have this problem. DBC involves a copper oxide layer in the bond joint between the copper layer and the ceramic core. This copper oxide layer is not well defined for modeling, nor is there published data on fatigue failure, but at the same time, it probably plays some role in the delamination tendencies of the substrate at elevated temperature.

The best that can be done is to make a qualitative analysis of the stress patterns in the solder layer by comparing different material stackups to a baseline stress pattern. This will serve as a starting point for experimental analysis of failure and fatigue in the solder layer and the packaging as a whole.

5.7.1.3 Modeling

The general design strategy is to choose a set of materials which appears to work by looking at the material properties, and then developing a package which puts these properties to best use. For thermal calculations, the semiconductor package is simplified to include only the power semiconductors and the free-wheeling diodes which make up an inverter bridge, along with the substrate materials underneath the devices which will transfer the heat out of the devices and into the heat sink. After being drawn up physically with the SolidWorks CAD system, this simplified version of the semiconductor package is then modeled for its thermal and mechanical performance using a finite element analysis (FEA) program. The FEA program which is used for the analysis is CosmosWorks, also a product of SolidWorks Corp. (a Dessault Systemes company). Using two CAD products from the same company assures compatibility.

The thermal stress modeling is done on a two-dimensional model and focuses on obtaining the tensile (first principle) stress in the solder layer underneath the device. To verify that the stress patterns in the two dimensional models are relevant to the three-dimensional models, the two-dimensional stress patterns are compared to the stress patterns from a three-dimensional 1/8th model at the corner of the die. Both the magnitude and the stress pattern are similar when looking at the tensile stress (principle stress) developed in the various layers of the package. Because of the similarity between the stress magnitude and pattern, the two-dimensional models are used to obtain better mesh resolution.

5.7.1.4 Two-Dimensional (2D) Design Evaluation

The 2D models used for analysis are highly simplified and used primarily for stress comparisons between materials. A standard power semiconductor package does not have any obvious lines of symmetry (internally) which are useful, so the package is reduced to a single die, insulated on the top, with a material stack underneath which forms the heat path from the die to the air. The heat sink is simplified as a simple heat transfer coefficient, coupled with the bulk air temperature, to form the thermal boundary on the underside of the material stack.

Evaluations of the 2D model stress patterns are then made by comparing the stress patterns obtained from the proposed 200 and 300°C packages to those stress patterns obtained from a standard 125°C package. Those proposed package designs with stress patterns similar to the 125°C package baseline are deemed to be reliable for the purpose of obtaining a starting point for experimental thermal testing, to be done in Phase II of this project.

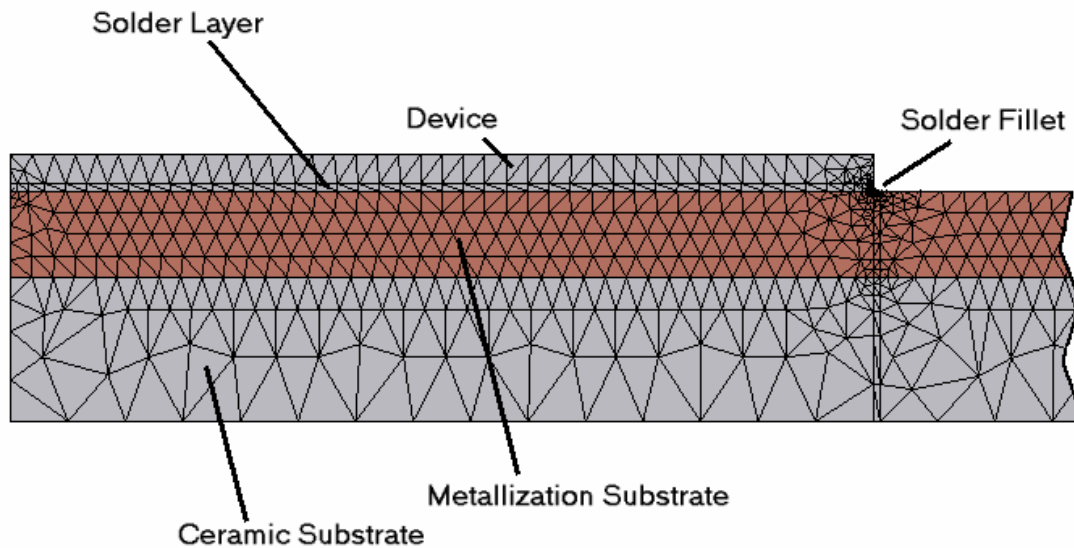
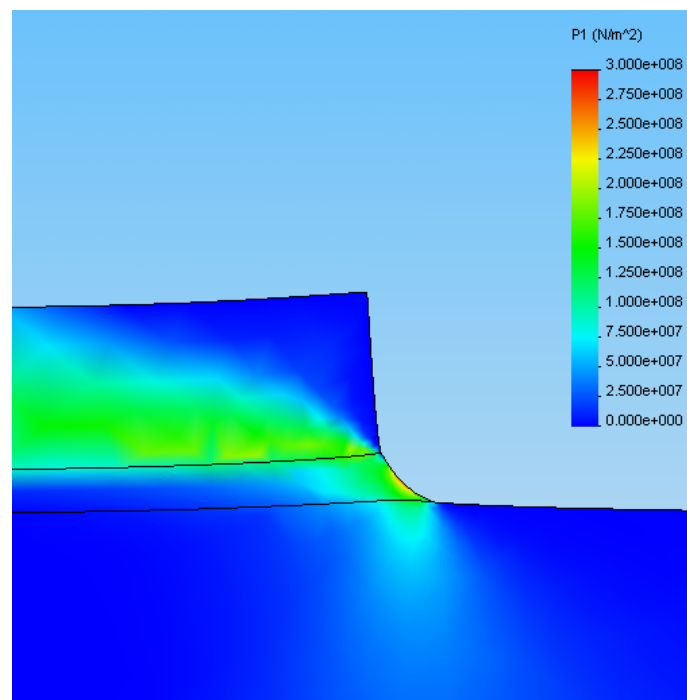


Figure 29. 2D Thermal Stress Model Showing Mesh



**Figure 30. Stress Levels at Solder Fillet
Baseline 125°C Package Using Alumina-Based DBC**

5.7.1.5 Three-Dimensional (3D) Design Evaluation

Once the design has been evaluated from a 2D perspective, a 3D model of the design is constructed and analyzed. The model is simplified to consist only of the six switches and six diodes forming the three-phase inverter bridge, and the material stack forming the thermal path from the devices to the heat sink. The heat sink model includes fins to determine the extent of the heat spreading within the fin. Data from

the static and dynamic device testing is then put into a converter model and the losses in the converter, along with the 3D thermal model, are used to size the heat sink, emphasizing a small form factor.

5.7.1.6 Local Environment versus Full Inverter

The analysis pertaining to thermal packaging has two primary parts: stress determinations around the device and overall sizing for gross heat removal. The first part involves, as indicated above, the use of two CAD tools for the thermal and stress computations. This part can be abstracted from a total inverter block with devices, substrates and heat sink. That is, it can be carried out by focusing just on the device and immediate substrates with everything else represented in the form of boundary conditions. When done this way, there is great latitude in how the models are set up. The power level, for example, does not need to match the specifications for a given application. All that is important is that the local conditions simulate the conditions in the given application. The models and assumptions must produce the temperature gradients and differential movement of adjacent materials that will be found in the real device stack.

5.7.2 Proposed 200°C Package

5.7.2.1 Design Methodology

A 200°C package is analyzed here because it is likely the upper limit in temperature for a SiC power MOSFET. The MOSFET is the most mature of the SiC devices currently in development and will probably be the first to be commercialized, perhaps as soon as this year by Cree. The 200°C package will deliver most of the size reduction from using SiC at elevated temperature, but at the same time entails less risk than attempting to achieve 300°C immediately. The materials which will enable an adequate 200°C package are already on the commercial market and being used in power semiconductor packaging. Modest changes will be required.

For 200°C, DBC is the natural choice because it is so prevalent. DBC with an alumina core is commonly used in standard power semiconductor packaging with maximum temperatures up to 125°C. Alumina performs adequately for a 125°C package and is inexpensive. For the 200°C package, because the thermal stress levels are expected to be higher, it makes sense to try DBC based on an aluminum nitride core. An FEA analysis comparing (1) stress levels in a 125°C package using copper and alumina, and (2) the stress levels in a 200°C package made from AlN based DBC indicates that the AlN-based DBC is perfectly adequate for temperatures up to 200°C. AlN-based DBC is reasonably inexpensive and is a commercially available substrate material sold by Curamix in Germany and IXYS in the US.

5.7.2.2 Package Concept

The stress levels between Figures 30 and 31 show that it should be fairly straight-forward to move from a 125°C operating temperature to a 200°C operating temperature. Because of this, a more detailed design concept can be attempted.

The baseplate of the package should be made of a low CTE material such as AlSiC or CuW (copper tungsten alloy). A substrate of aluminum nitride based direct bonded copper should be soldered to this baseplate using gold-tin solder. The SiC die should be attached to DBC substrate using a solder with a lower eutectic melting temperature than gold-tin solder, such as tin-silver (95% tin-5% silver) which has a melting temperature of 240°C and can be used at operating temperatures of 200°C. Having two solders with distinctly different melting temperatures is essential for processing reasons. Which solder joint has the higher melting temperature solder (the substrate attach or the die attach) depends on how the package is assembled. Using the higher temperature solder to attach the substrate to the baseplate assumes that the baseplate/substrate subassembly is assembled before the devices are placed on the substrate.

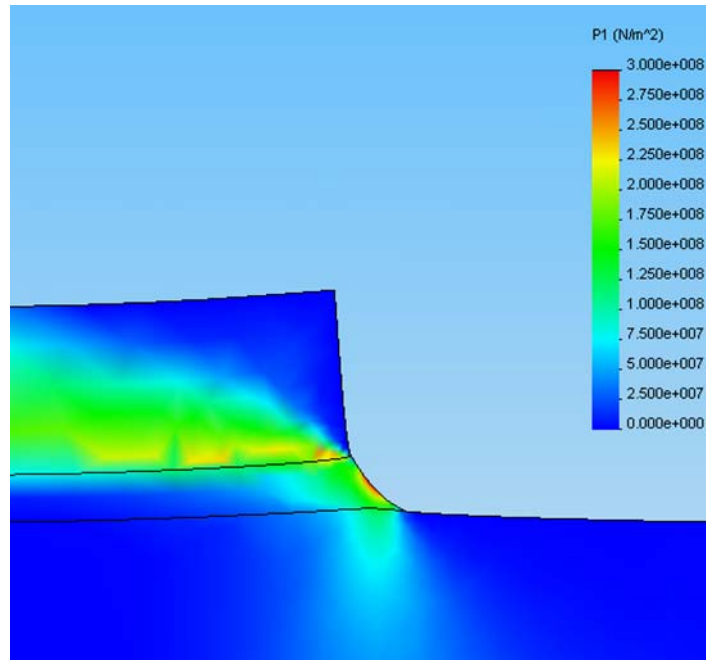


Figure 31. Stress in AlN-Based DBC in 200°C Package

Once the device is bonded to the DBC substrate, wirebonds are attached. Because the temperature is not so extreme as to warrant the extra cost and technical difficulties of using large diameter gold wire, aluminum wire will be used here. For the case, there are various plastics and epoxies which can survive temperatures up to 200°C, and potting compound can be found for this temperature range as well. Figure 32 shows the proposed package construction, neglecting the wirebonds and the package leads.

5.7.3 Proposed 300°C Package

The 300°C package is the logical extension of the 200°C package. At 300°C, the temperature difference between the device and the environment will be raised to over three times that found when the die temperature is limited to only 125°C, causing an additional size reduction. A 300°C package is also worth studying because 300°C represents a new circumstance where traditional packaging techniques are impractical or impossible.

There are several different combinations of materials which seem, from preliminary FEA studies, to perform adequately at 300°C. The performance evaluation is based on comparisons of the stress levels in the package under study as compared to a 125°C rated alumina-based DBC package. All the packages proposed here use gold-based hard solder to obtain the 300°C rating; the variables between the packaging concepts shown here are in the substrate and metallization compositions.

One of the most promising technologies for 300°C power electronics packaging is direct bonding of the metallization in foil form to a ceramic substrate as in DBC, which was discussed earlier. Unfortunately, the current compositions of direct bonded substrates are unsuitable for reliable use at 300°C because the coefficient of thermal expansion (CTE) of the composite substrate is too high, even when using an aluminum nitride core. However, there are other formulations of direct bonded metal foil substrates which are technically feasible and provide better thermal stress characteristics than current direct bonded metallization substrates.

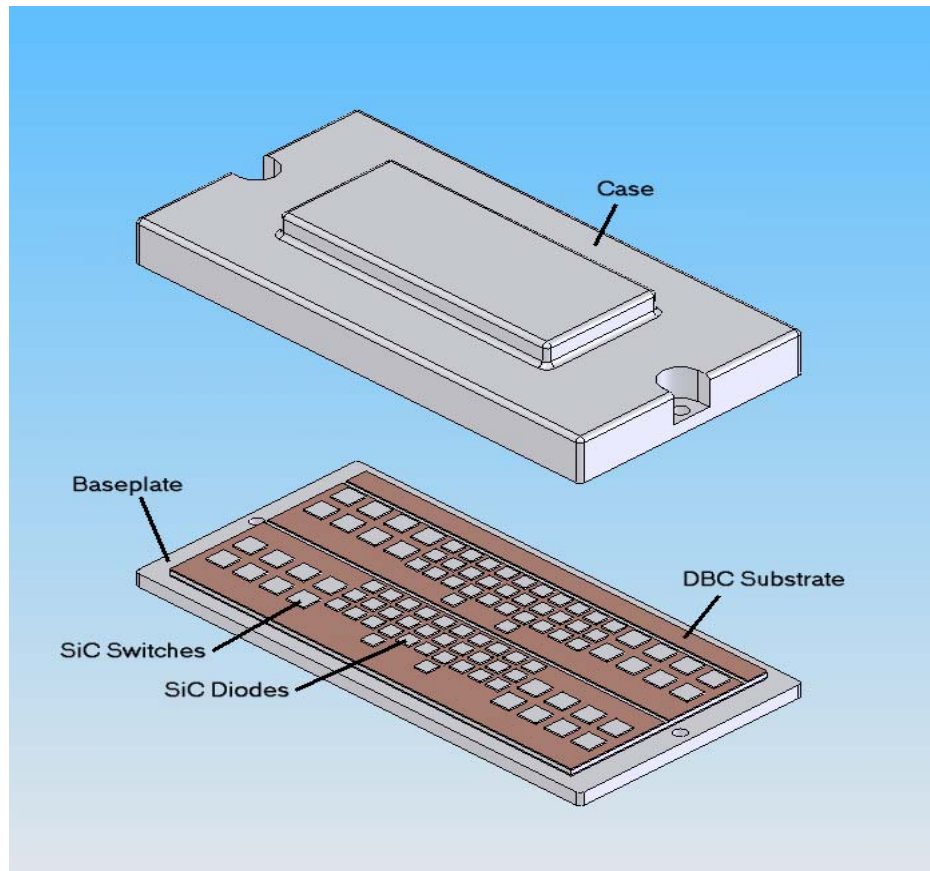


Figure 32. Proposed 200°C Package for 100 kW Inverter

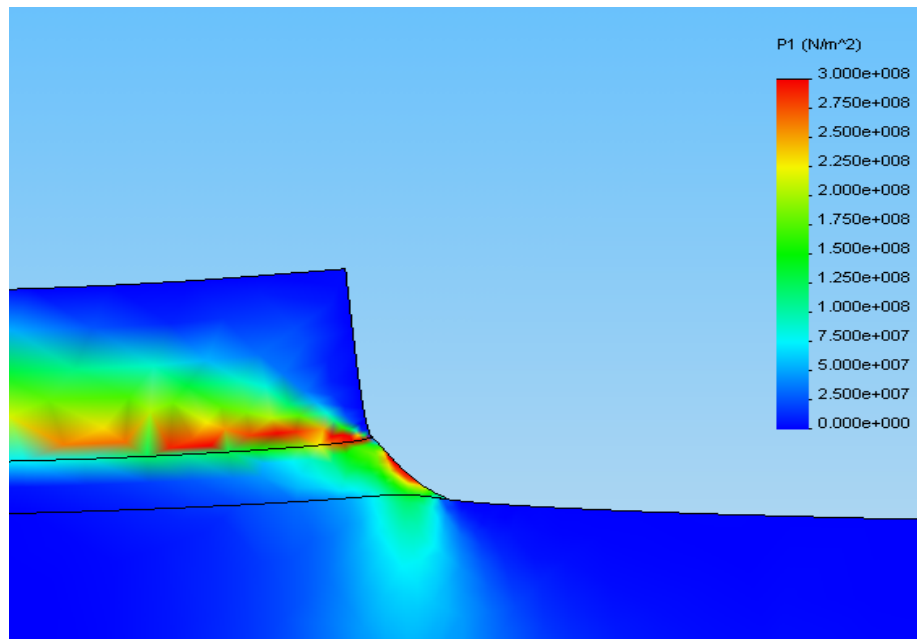


Figure 33. Stress Profile for 300C Package Using Al/AlN/Al Direct Aluminum Bond

5.7.3.1 Aluminum Nitride Based Direct Bonded Aluminum

Discussions with a representative from a DBC supplier indicate that, while this material is not in production, it is technically possible to produce. IXYS has already introduced a similar substrate material called DAB, which uses aluminum for the metallization and alumina for the ceramic.

FEA analysis indicates that the performance of a 300°C package made with this material will be less reliable than the baseline alumina based DBC package, but the stresses in the 300°C package are shown to be not much worse than the baseline. Experimentation will be necessary to determine exactly how much worse this package performs.

The advantage of this package is that all the material is available and the processes are technically feasible. Some work will have to be done to develop this particular substrate/metallization combination, probably with IXYS, a DBC supplier. Of the three substrate combinations given in this section, the aluminum nitride direct bond aluminum substrate is the worse performing from a thermal stress standpoint, but is probably the most feasible due to the known bonding process and the current carrying capabilities of aluminum metallization.

5.7.3.2 Silicon Nitride Based Direct Bonded Aluminum

This combination represents the best that direct bond technology can possibly offer, in terms of stress in the solder layer of the die attach and current carrying capabilities. This material combination has not been attempted before, but it is probably feasible through processes similar to the IXYS DAB product using alumina, which is a commercial product. Like aluminum nitride based direct bonded aluminum, the silicon nitride based direct bonded aluminum will have high current carrying capabilities due to the relatively large thickness of the aluminum conductor layer. This is very important if the package is going to be used in high power products where the current levels are in the 200A or larger range.

Figure 34 shows that the stress levels are on the same order as the alumina based DBC which is currently used in modern power semiconductor packages. This indicates that the reliability of a package based on silicon nitride and used at a 300°C operating temperature will be similar.

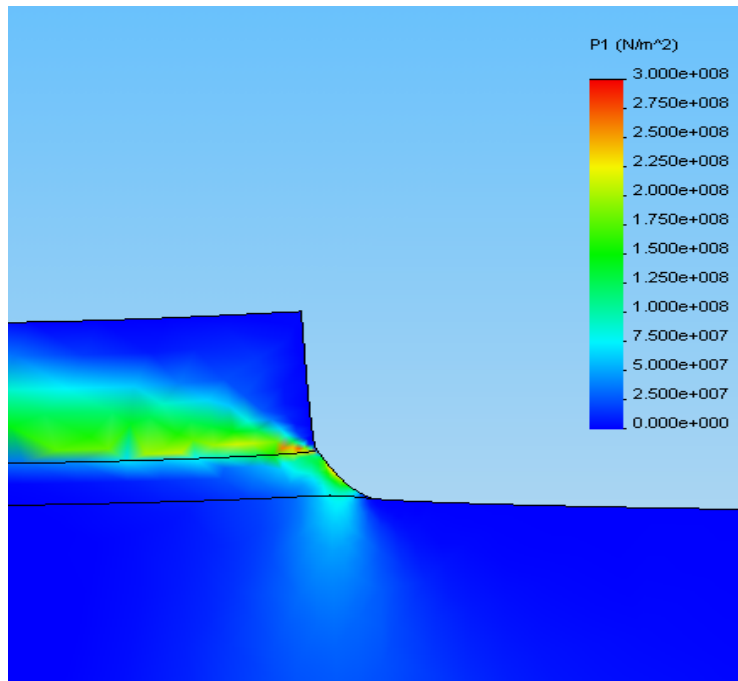


Figure 34. Stress Profile for 300°C Package Using Al/Si₃N₄/Al Direct Aluminum Bond

The largest difficulty with a package made from these materials is that, not only has the direct bond process not been tried before, but silicon nitride is only just starting to become a useful material for a semiconductor package. In place of silicon nitride, commercial silicon carbide ceramic might also be used for this package, with similar results in the stress levels at the die attach. Commercial silicon carbide has very different bulk properties than the silicon carbide used in semiconductors because it is a multi-crystalline aggregate instead of being a single crystal monolith. In practical terms, this means it is much cheaper, but its bulk thermal conductivity is lower and its coefficient of thermal expansion is larger. There seems to be no clear reason why aggregate silicon carbide is not more often used in semiconductor packages. Cost might be an issue in that silicon packages can get away with using alumina, which is less expensive.

5.7.3.3 Gold Thick Film on AlN

Gold thick film is a promising candidate and performs the best from a stress level standpoint. However, the problems with using gold thick film are numerous. While gold offers good stress relief on the solder joint because of its elasticity, it does not provide sufficient current carrying capacity to compete directly with aluminum or copper. Building up adequate conductor thickness using thick film technology will require many layers of thick film metallization, each with its own interface and possible failure modes. The current state-of-the-art in thick film technology is just barely adequate to provide for sufficient current carrying capacity for power semiconductors and would not likely be sufficient for the high power applications in this project.

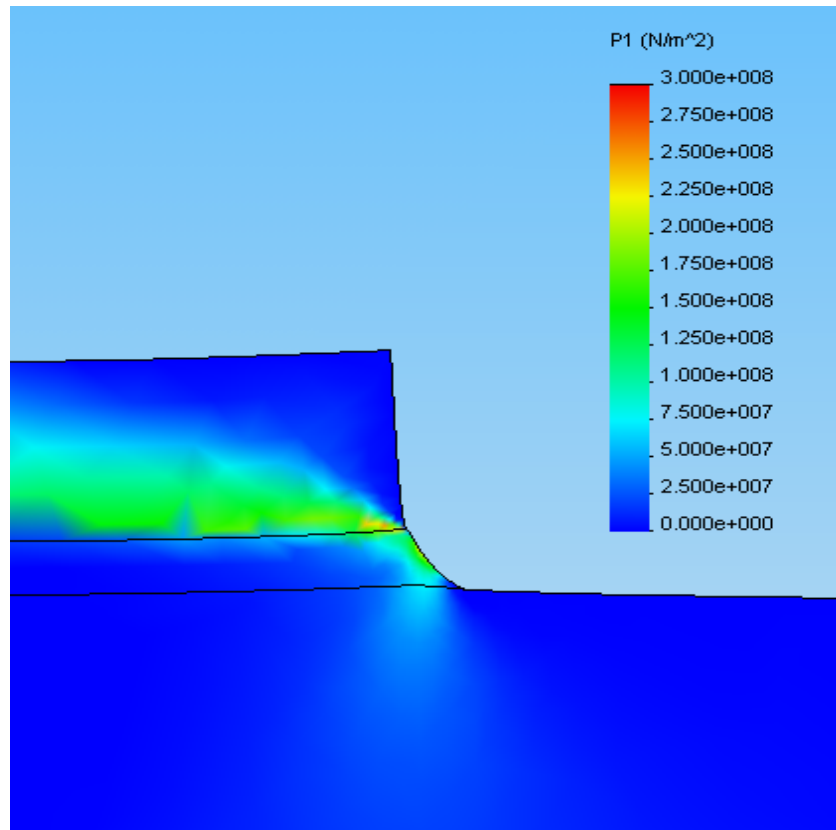


Figure 35. Stress Profile for 300°C Package Using Au/AlN Thick Film Gold Metallization.

For low current, high temperature applications, gold-based thick film is clearly the best from a thermal stress standpoint. For higher currents, either one of the above solutions have to be used, or the current needs to be divided up in such a way as to keep the current density through any one set of conductors low. One way of doing this is to provide each device with its own isolated, metallized pad, which carries only the current exposed to the particular device. Once the current travels through the device, the divided current can then be recombined at a bus bar made of DBC. If the inverter is made up of individually packaged discretes, the conductor pad inside the discrete package can be gold thick film on AlN, while the bus bar connecting each discrete to the others can be made up of copper. In this way, the gold thick film metallization will only have to carry a small portion of the current. This is viewed as a stop-gap until a better solution is found.

A combination of metallization materials might also be useful. A thick film gold layer atop a copper metallization layer may work, since it is the stiffness (modulus of elasticity) of the metallization material which produces most of the stress at the solder layer. Generally, the ceramic layer contributes to the stress level via the CTE mismatch with the die, and the metallization layer, since it is relatively thin, contributes to the stress level via the material's modulus of elasticity (E).

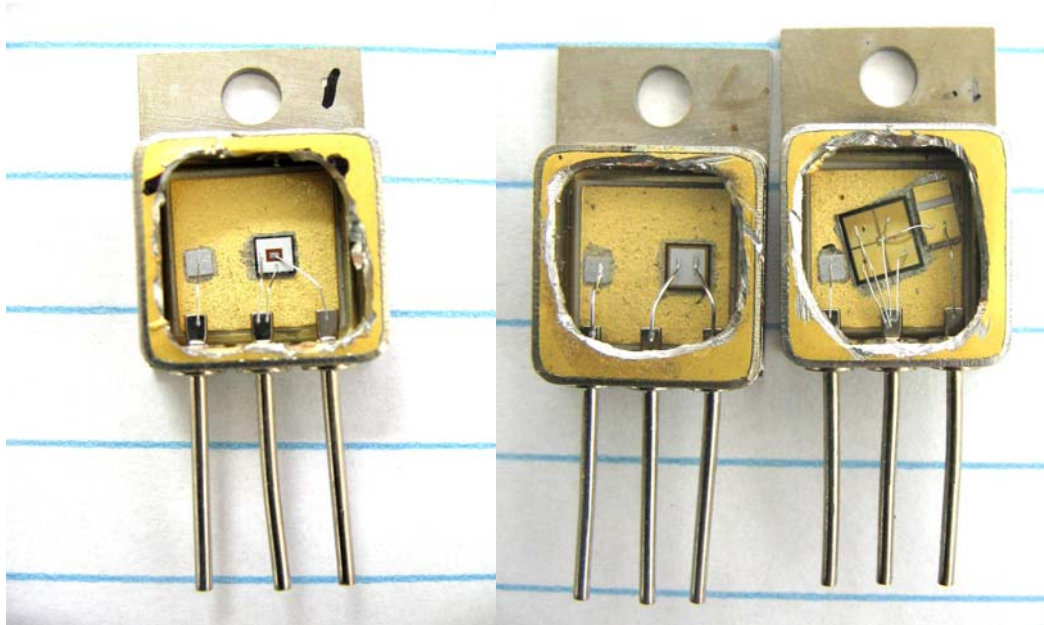


Figure 36. From left to right, SiC JFET, Schottky Diode, and BJT Packages

5.7.4 SSDI Packaging for High Temperature Device Characterization

In carrying out SiC device characterization at elevated temperatures in Phase I, the devices obviously had to be mounted in a manner that would allow them to be operated at up to 300°C. Long-term thermal reliability was not the requirement, just the ability to run them sufficiently to collect the data – on the order of minutes with little thermal cycling. The high temperature mounting was carried out by Solid State Devices Inc (SSDI) of Los Angeles.

The packages which SSDI used are in the footprint of a TO-254 and hermetically sealed. The substrate directly underneath the device is DBC (8mil Cu/25mil AlN/8mil Cu) which is nickel underplated and gold plated to facilitate wirebonding. The device is soldered to the substrate using gold-tin solder and the substrate is attached to the tab using gold germanium solder. The tab of the package is made of copper tungsten. The case is made of copper with a Kovar lid. Wirebonding is accomplished using aluminum wires.

These packages were successfully taken up to temperatures exceeding 300°C without loss of operation. Because the die attach is gold-tin, which has a eutectic melting point just short of 300°C, the solder probably came close to reflowing at the highest testing temperatures. This should have no effect on the electrical testing; however, the package cannot be cycled repeatedly to 300°C with any reliability. In one test, the package withstood temperatures up to 425°C without explicitly failing as a discrete device; however, upon opening the package, signs of melted solder were found, indicating that the solder reflowed as it was operated above its eutectic point. Further investigation as to the lifetime expectancy of the package when cycling between room temperature and 200°C, and room temperature and 275°C, will take place in the near future in some of Peregrine's other work.

5.8 Effect of Operating Temperature on Heat Sink Size

5.8.1 Losses and Operating Temperature vs. Heat Sink Baseplate Area

When referring to the “size” of the inverter, the largest contributor to the size is the heat sink and fan assembly. The heat sink and fans can make up over 80% of the total inverter size. With this in mind, the size of the heat sink has been computed for various operating temperatures and presented in Figure 37.

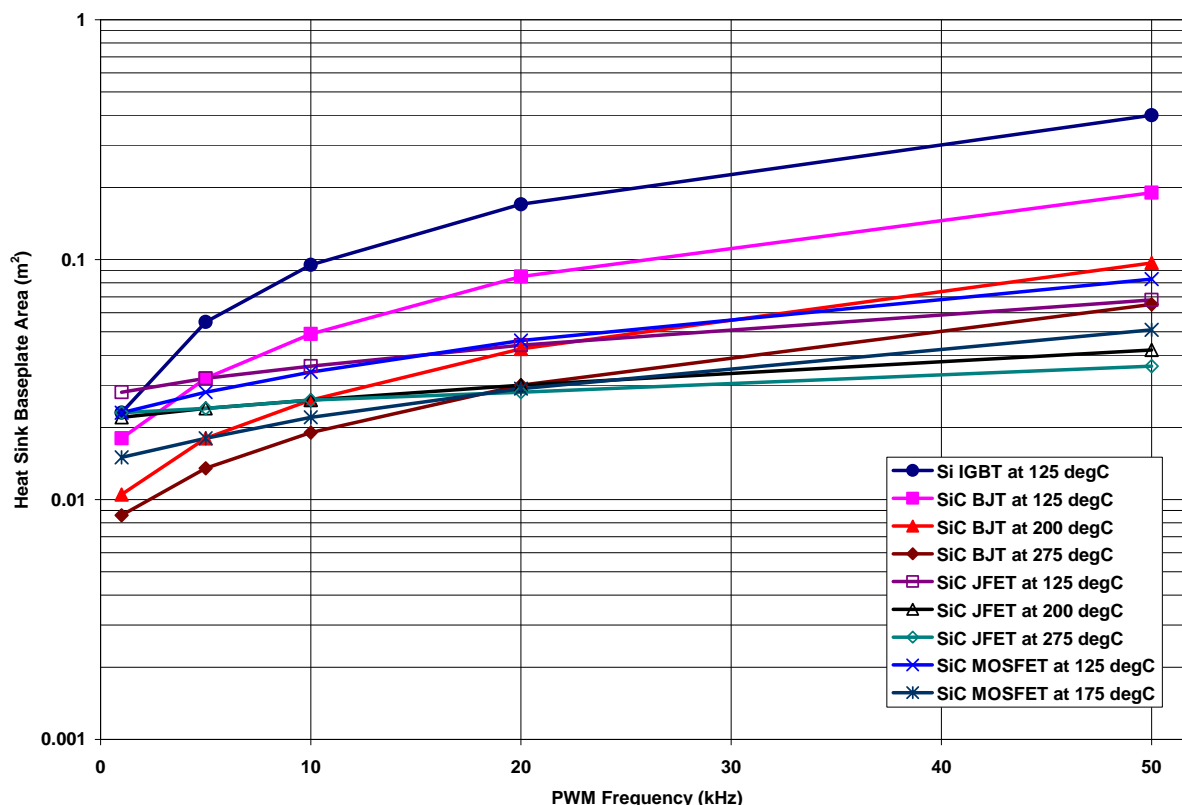


Figure 37. Total Converter Baseplate Area (Proportional to Losses) with Changing Switching Frequency and Temperature

In increasing the operating temperature of the devices, the conventional wisdom is that the size of the heat sink should decrease. Opposing this effect is a potential increase in losses in the devices resulting from the fundamental degradation of performance of some types of devices at elevated temperature. If the losses increase by the same ratio that the die-to-ambient temperature difference increases, then the heat sink will not change in size. A major activity at Peregrine in Phase I was to test SiC JFETs and BJTs at temperatures from room temperature to 300°C for both switching and conduction losses to determine precisely how large this offset is as temperature is increased. In general, it was found that the conduction losses become worse at elevated temperature, while the switching losses do not.

Figure 37 shows the change in heat sink volume as a function of temperature and switching frequency, based on the conduction and switching loss data obtained from testing Cree SiC BJTs. The size calculations were obtained using convection heat transfer correlations corresponding to a fan (or fans) delivering 55 cubic feet per minute ($Re_D = 4007$) through a straight-fin heat sink; a common design for cooling power semiconductor blocks. The major conclusion coming from Figure 37 for SiC devices is that while the losses increase in these devices as the temperature increases the losses are more than offset by the benefits of the greater heat transfer rate as the operating temperature of the device is increased.

The lowest increase in conduction losses occurs with the SiC BJTs and the greatest increase in conduction losses occurs with the SiC JFETs. In fact, if an application is dominated by conduction losses, as opposed to switching losses, the JFETs are not highly benefited by higher temperature; that is, the value of a higher thermal gradient is almost entirely offset by the increase in losses. If the application is dominated by switching losses, say, in a low power, high frequency power supply, then higher temperature is highly beneficial to the JFET. As emphasized elsewhere, the benefits of elevated temperature is application specific. For the high power applications of this project, the conduction losses dominate, leading to the use of BJTs or GTOs (not tested, but some published data exists). Higher temperature does make sense for this since the increase in conduction losses does not offset the increase in thermal gradient. Further details of Peregrine's tests and results are discussed elsewhere.

5.8.2 Practical Cooling System Design

From Figure 37 above, a design point is chosen to design a cooling system around. The design point includes two comparative devices, a silicon IGBT at 125°C and a SiC BJT at 275°C, both switching at 20 kHz, which is appropriate for minimizing the size of the passive filter elements in a power generation application. A heat sink design is based on the baseplate area shown in Figure 37, and a fan and plenum system designed around the requirements for the respective heat sinks.

While the baseplate area for the heat sink is directly proportional to the power dissipation of the devices, the design of the fins cannot be strictly held constant in a real world design because of restrictions on the specifications of the fan that blows air through the fin array. As the power dissipation and thus the heat sink baseplate area becomes larger, the flow rate and pressure drop across the heat sink change in a non-linear fashion. This means, in practical terms, that the fan requirements increase faster than the baseplate area as the dissipated power is increased.

The heat sink and fan system were designed around a 50°C operating environment. The fan and plenum system were specified using the product line of NMB, a company which manufactures electronics cooling fans, amongst other things. In both designs for the silicon IGBT and SiC BJT heat sinks, the fans were specified to deliver a convection cooling coefficient of 50 W/m²/K. To keep with the spirit of a direct "apples to apples" comparison, both heat sinks are modeled as aluminum extrusions.

5.8.2.1 Thermal Modeling

Figures 38 and 39 show the temperature distributions of the IGBT and the BJT respectively. Because all the other components make only slight differences in the temperature distribution, only the heat sink and the baseplates of the individual device packages are modeled. Heat power

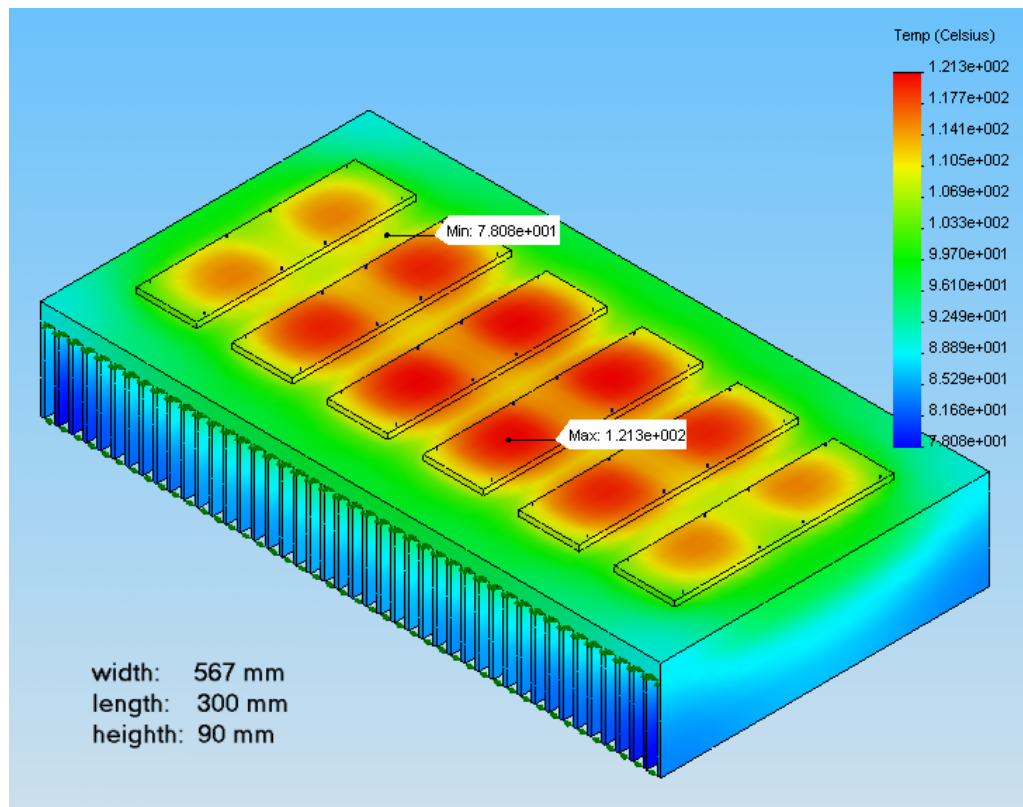


Figure 38. Si IGBT Heat Sink Temperature Distribution in 50°C Environment

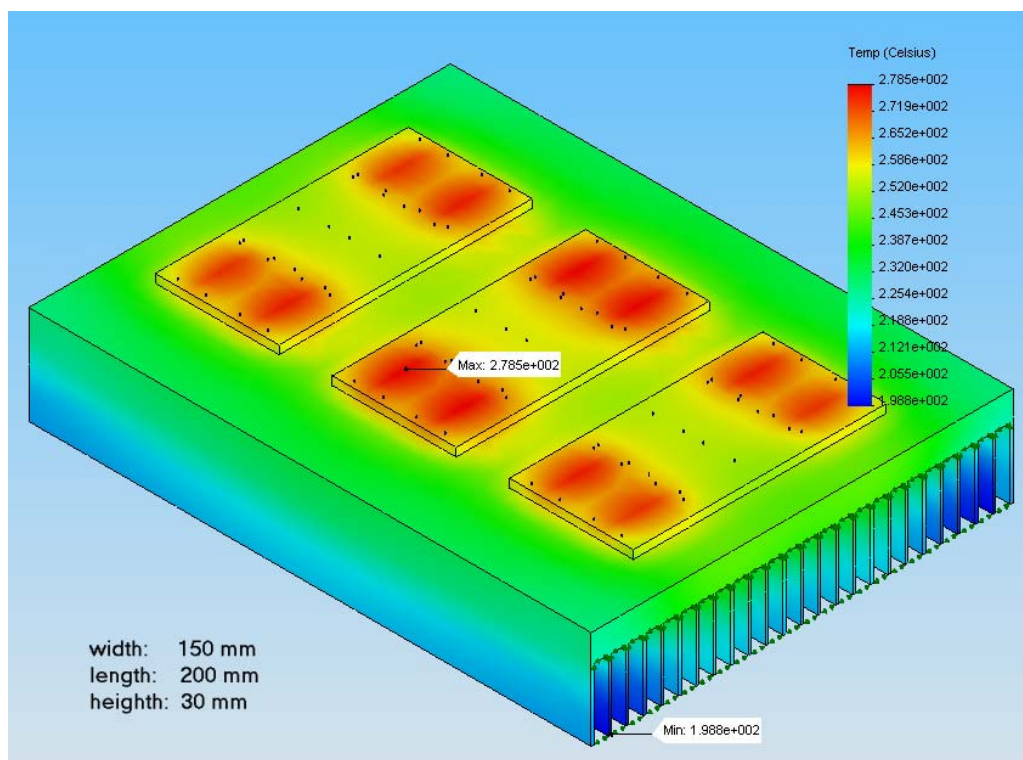


Figure 39. SiC BJT Heat Sink Temperature Distribution in 50°C Environment

boundary conditions are applied to various regions of the device package baseplates, and convection heat transfer boundary conditions are applied to all the surfaces of the fins.

Because the SiC inverter is roughly 2x more efficient than the Si IGBT inverter switching at 20 kHz and because the temperature differential between the device and the ambient temperature of 50°C is 3x higher for the SiC BJT inverter compared to the IGBT inverter, the baseplate of the BJT inverter heat sink is roughly 1/6th the size of the IGBT heat sink baseplate. As discussed before, the design of the fins between the two inverters cannot be easily related back to the losses from the inverter because the relation between air flow rate and pressure drop, the two variables which control fan selection, to cooling load is non-linear. Here, empirical convection correlations were used to design the length, thickness, and spacing of the heat sink fins.

5.8.2.2 Comparison of Cooling Requirements between Si and SiC

Figures 40 and 41 show the full inverter plus cooling system for both the Si IGBT based inverter and the SiC BJT based inverter. It is quite clear that the system as a whole becomes much smaller when moving from Si devices at 125°C to SiC devices at 275°C.

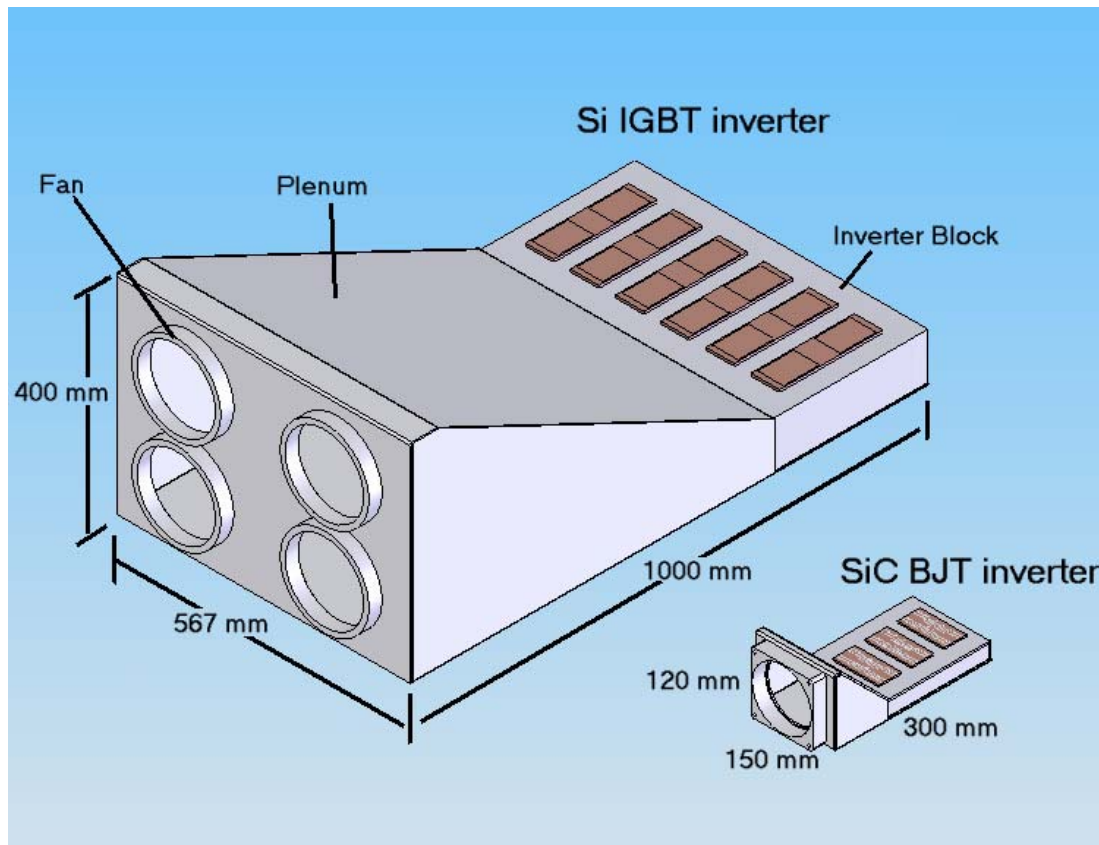


Figure 40. Comparison (To Scale) of Si IGBT Inverter at 125°C to SiC BJT Inverter at 275°C, Including Cooling Equipment

The fans were selected using curves from a commercial catalogue. The plenum is required to direct the air flow through the fins of the heat sink and is constructed from sheet metal. Fans running in parallel, as in the case of the Si IGBT inverter, increase the flow rate of air through the heat sink in low pressure drop situations. Because of the non-linear relationships between air flow and pressure drop to heat transfer rate, the IGBT inverter requires nearly 10x the airflow of the SiC based inverter.

5.9 Filter Design

5.9.1 Proposed Filter and Its Functionality

Figure 42 shows the output filter array proposed for development in this project. The output filter carries out two distinct functions. The first is to remove the carrier frequency of the pulse width modulation (PWM) used in the inverter bridge. The voltage on the DC bus that feeds the inverter is chopped by the solid-state switches of the inverter into a string of pulses, where each pulse has a calculated width. With smoothing, the voltage or current will assume an average which is directly related to the duty cycle of the pulses. PWM frequencies used in power electronics are often as low as several kHz and may exceed 100 kHz. For the high power applications addressed in this project switching frequencies of the order of 1 kHz or lower would be typical. SiC will allow higher frequencies to be used at up to 20 kHz or even more. For the remainder of this section, it will be assumed that the switching frequency for silicon devices is 1 kHz and for SiC devices could be 10, 20, or 50 kHz. It is not clear that 50 kHz in a multi-MW application is feasible or even advisable, but its inclusion in the analysis allows all realistic cases to be bracketed.

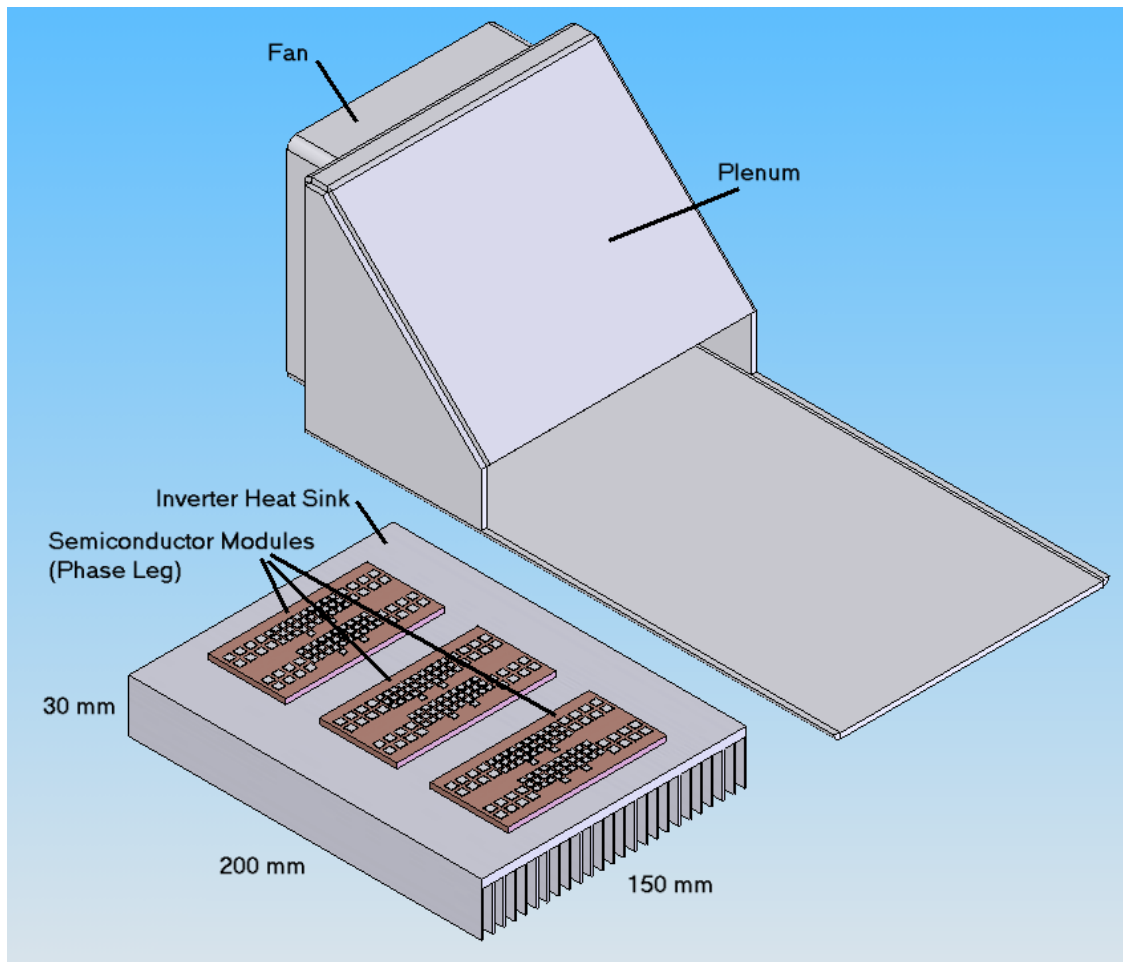


Figure 41. Exploded View of SiC BJT Inverter at 275°C, with Cooling Equipment

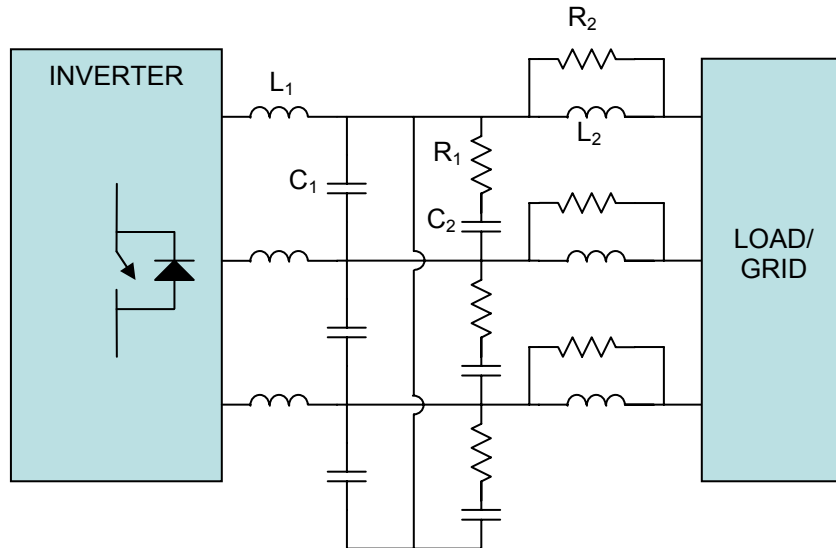


Figure 42. Output Filter Topology

If no filter element were placed between the load and the inverter switches, the load would see the high frequency train of pulses directly. In this situation, the load would experience extraordinarily poor power quality and a dead short might occur with any load that has another voltage source (grid or genset). Interposing an inductor will tend to reduce the PWM distortion in (smooth) the current, plus eliminate the possibility of the dead short. Thus, the inductor represents the minimal filtering that would be necessary. A variable speed drive (largest market for power electronics in the world) uses the inductance of the motor being controlled for this purpose and does not generally need a supplemental inductor. Any inverter used for general purposes, however, needs at least the inductor. To remove the PWM distortion in the voltage, capacitance must be inserted also. These L-C filter elements (see L1 and C1 in Figure 42) can be repeated to give an L-C-L or L-C-L-C array which smooths the current and voltage even further.

The second function of the output filter elements is to minimize the linkage of (decouple) any elements which might cause system instability in the form a resonance. Resonance is caused by the presence of Ls and Cs, along with an exciting force tuned to their natural frequency. Since both Ls and Cs must be present in the overall power conversion system, the risk of resonance is present. The elements other than L1 and C1, as shown in Figure 42, de-couple any passive elements in the load from those in the inverter or filter. L2 is particularly important in this function. R1 and R2 assure that any resonances are convergent and quickly dampened.

The filter topology shown in Figure 42 is used only for comparative purposes. The actual filter used would differ, depending upon the application. For grid connection of fuel cells or wind turbines, there would probably be a step-up transformer at the output of the inverter to increase the voltage to the distribution or transmission level. The step-up transformer would provide significant impedance, approximately 5% of the system base impedance, leading to lower filtering requirements. Capacitance might also be necessary to smooth voltage to bring it within the tolerances specified by IEEE519, the North American standard on harmonic distortion.

If the application requires the output of the inverter to be connected directly to the load (no grid interconnection), the filter design might have all of the elements shown in Figure 42. Other applications might require other variations.

In addition, the filter topology might differ with the switching frequency. With a switching frequency of 20kHz the filter topology might be simplified from that shown, but at 1 kHz where it is much closer to the desired 60Hz output, a tuned filter might be called for since the risk of interaction between passive

elements is greater. However, for the comparison presented here, the same filter topology is used for all frequencies and a three-phase resistive load is assumed.

5.9.2 Filter Modeling and Design Criteria

Simple filters are susceptible to analytical solutions, but the normal technique today is to simply simulate the filter with a CAD tool. Values can then be easily changed, allowing families of designs to be developed which the designer can use to optimize the circuit to meet specific objectives. There are several excellent CAD tools available for the simulation of circuits. For the results presented here, Peregrine used PSpice (product of Cadence), perhaps the best known and most popular of such tools. The upper limit on voltage and current ripple at the output of the filter was 5 percent total harmonic distortion (THD), the upper level specified by IEEE519. The THD level can be readily reduced or increased by changing the component values in the simulation.

5.9.3 Resulting Filter Component Values

Table 10 shows the filter component values for required for different switching frequencies for a 480VAC system with a DC bus of 680V operating at a total power output of 100kW.

Device Type	Switching Frequency	L1 [μH]	L2 [μH]	C1 [μF]	C2 [μF]	R1 [Ω]	R2 [Ω]
Silicon	1k	4160	690	10	10	150	7.5
SiC	10k	280	46	1.5	1.5	50	0.47
SiC	20k	140	23	2.2	2.2	50	0.47
SiC	50k	56	9.2	1.0	1.0	50	0.47

Table 10. Filter Design at 100kW, 480VAC with Different Switching Frequencies

Inductors L1 and L2 dominate the filter size and weight. Thus, the size and weight for only these two components is presented here. For 1 kHz, L1 and L2 were designed with 0.5 mm thick E-I laminations made of silicon steel. For the other frequencies commercially available powdered iron E-cores were utilized. The approximate dimensions, volume, and weight of these components are given in Table 11. All of the component values for L1 and L2 are inversely proportional to switching frequency. This obviously has a dramatic impact in reducing size and weight as the frequency is increased.

Freq [kHz]	Value	L1 Size [LxWxH] (in)	Weight [lbs]	Value	L2 Size [LxWxH] (in)	Weight [lbs]
1	4.2mH	9 x 11 x 8	160	690uH	3 x 4.4 x 2.5	8
10	280uH	6.1 x 9.1 x 6.1	46	46uH	4.5 x 2.6 x 3.6	6.3
20	140uH	6.1 x 7.1 x 6.1	36	23uH	4.5 x 2.7 x 3.6	5
50	56uH	6.1 x 5.3 x 6.1	26	9.2uH	3.1 x 1.7 x 3.1	2.5

Table 11. Size and Weight of Dominant Filter Elements

5.9.4 Filter Design for 4,160VAC, 1MW System

Increase in switching frequency in medium voltage systems would lead to similar reduction in filter requirements. However, the increased voltage level will lead to significantly higher value of the inductors required. Cores for these inductors are not commercially available and would have to be custom made using appropriate high frequency core material -- powdered iron or ferrite, or a hybrid structure of a tape wound core with powdered iron material used for realizing the gap. Further, the increase in voltage will lead to higher stray capacitive effects in the inductors which will become more pronounced at higher switching frequencies. Stray capacitance in inductors will reduce the effectiveness of the filter and also add to the switch current stress during turn-on. Thus, special winding techniques would be required to minimize the stray capacitance.

The actual design and fabrication of the necessary high frequency inductors for use at 4,160VAC is an entire R&D project in itself. No one in the world makes such inductors, to the knowledge of the Peregrine team. This is not because it cannot be done, but because there simply has been no need. The high frequencies enabled by SiC devices in high voltage circuits have never before been possible. Note that Peregrine is associated with many consultants with specialties in areas pertinent to power electronics. Several of these are experts in magnetics. The design and fabrication of these inductors has been discussed with one of these, who concluded that, while there will be design issues due to the novel application, none of these will be obstacles that stand in the way of actually realizing the dramatic size reduction suggested by this analysis.

The ultimate prices of the high frequency inductors should also decrease to reflect the substantial reduction in material with increased frequency. This would not be apparent if one or a few inductors were fabricated today, but it will be as the market and manufacturing infrastructure for high frequency, high power magnetics develop. An indication of this eventual result is the fact that the cost of magnetics in power supplies has definitely decreased as frequencies have increased.

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