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Upgrading the Digital Electronics of the PEP-II Bunch Current Monitors at the Stanford Linear Accelerator Center

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ABSTRACT

Upgrading the Digital Electronics of the PEP-II Bunch Current Monitors at the Stanford Linear Accelerator Center. JOSH KLINE (Sacramento State University, Sacramento, CA) ALAN FISHER (Accelerator Department, Stanford Linear Accelerator Center, Stanford, CA 94025)

The testing of the upgrade prototype for the bunch current monitors (BCMs) in the PEP-II storage rings at the Stanford Linear Accelerator Center (SLAC) is the topic of this paper. Bunch current monitors are used to measure the charge in the electron/positron bunches traveling in particle storage rings. The BCMs in the PEP-II storage rings need to be upgraded because components of the current system have failed and are known to be failure prone with age, and several of the integrated chips are no longer produced making repairs difficult if not impossible. The main upgrade is replacing twelve old (1995) field programmable gate arrays (FPGAs) with a single Virtex II FPGA. The prototype was tested using computer synthesis tools, a commercial signal generator, and a fast pulse generator.

INTRODUCTION

PEP-II is a pair of 2.2 km circumference synchrotron storage rings for electrons and positrons with a standard operating current on the order of two amps located at the Stanford linear accelerator center (SLAC). Charged particles are injected into the ring from the linear accelerator at a frequency of up to 60 Hz; actual injection is controlled using data from the BCM. The ring traps charged particles using bend magnets to steer particles around the ring and quadrapole magnets to focus the beam. The energy radiated due to acceleration of the stored particles must be replaced. PEP-II replaces the lost energy by using cavities filled with 476 MHz microwave radiation to produce a stable orbit in the ring. Positrons and electrons are propagated in separate rings in opposite directions. The two rings are stacked on top of each other and intersect at a single interaction point.

PEP-II has 3492 buckets per ring for charge bunches to travel in. A bucket is a phase of the 476 MHz microwave where charged particles can be pulled around the ring without decaying to the center or being propelled out of the ring. Particles that are out of synchronous phase will either relax into phase or be completely ejected from the beam. This self correcting effect is a result of the stability of the bucket position. If a particle is out of synchronous phase it will not receive the proper amount energy from the microwave to achieve synchronous orbit.

If a particle is too late compared to the synchronous phase; it will gain less than the energy required to replace the radiated energy, this results in a net loss of energy. The less energetic particle will be bent by the bend magnets slightly more than during the previous turn. The lower energy particle will take a shorter path around the ring and arrive earlier than the previous turn, since the particles are propagated at approximately the speed of light. Thus the high energy(late) particle arrives earlier and earlier with each turn and are relaxed toward the synchronous phase. The result is an oscillation between too early in phase(low energy) and too late in phase(high energy). This oscillation is a product of the

relaxation of the high/low energy particles and is a stable of form particle propagation inside a synchrotron.

Every other bucket position is occupied with a charge bunch, where a charge bunch is group of charged particles moving around the ring in the same bucket. Every other bucket is left empty in an effort to minimize parasitic collisions between the positron and electron beams. A parasitic collision is when an electron bunch nearly collides with a positron bunch, resulting in a beam deflection at the interaction point. The last forty buckets are left empty in case the beam has to be terminated unexpectedly. The beam is terminated by turning on a magnet that bends the beam off course into a beam dump. The magnet field requires a finite amount time to reach the critical bend value. The forty bucket space is large enough so that the magnetic field can reach the critical strength to completely bend the beams into the beam dumps. If the magnetic field does not reach the critical value, the beam will oscillate, making a potentially bad situation worse.

Bunch current monitoring is a useful technique for fast measure and respond scenarios with semi-periodic subjects specifically in synchrotrons. BCMs are used to monitor the electron bunches and positron bunches traveling in the PEP-II particle storage rings at SLAC. In PEP-II charge bunches pass by the detector every 4.2 ns. Synchronous phase change from bunch to bunch occurs because the microwave cavities fill up with slightly more energy during the forty bucket gap, and so bunches just after the gap are slightly late compared to the synchronous phase, while bunches at the end of the bunch train are slightly early. In order to gather useful data the system must gather and respond to data very quickly. Particles are injected from the linear accelerator to ensure optimum charge density per bunch, and injection timing is determined by the charge information gathered from the BCM.

The BCM detector outputs a signal dependent on the electric field of the particle beam. The electrons/positrons are highly relativistic so the electric field detected results in a very fast bipolar pulse. The output of the detector is from four electric field sensors, and the

outputs are fed to a comb filter that combines the fast pulses (100 ps) into a single two period sinusoid of 1428 MHz. The sinusoid is then mixed with a 1428 MHz reference signal that is stepped through four ninety degree phases. The signal is fed through a low pass filter, and then is digitized by the on board digitizer. The four phase technique allows extraction of the bunch current value. The bunch current value is found by taking the sum of the squares of the difference between two signal values out of phase by 180 degrees. The average value is then computed over many turns to smooth out noise in the measurement. The mathematics is as follows.

The output of the comb filter is

$$s(t) = s_0 \cos(\omega t + \phi_{beam}), \tag{1}$$

where s_0 is the bunch current. The output of the mixer is

$$\mathrm{DC} + s_0 V_0 \cos(\omega t) \cos(\omega t + \phi_{beam} + \phi_{step}), \tag{2}$$

where V_0 is the reference amplitude. If we add the trigonometric identities

$$\cos(2\omega t + \phi) = \cos(\omega t) \cos(\omega t + \phi) - \sin(\omega t) \sin(\omega t + \phi), \tag{3}$$

and

$$\cos(\phi) = \cos(\omega t) \cos(\omega t + \phi) + \sin(\omega t) \sin(\omega t + \phi), \tag{4}$$

we can rewrite the output of the mixer as

$$\mathrm{DC} + \frac{s_0 V_0}{2} \cos(\phi_{beam} + \phi_{step})(\cos(2\omega t) + 1). \tag{5}$$

If we pass this output through a low pass filter, the signal becomes

$$\frac{s_0 V_0}{2}\cos(\phi_{beam}+\phi_{step})+\mathrm{DC}. \tag{6}$$

The step phase ϕ_{step} can assume four discrete values, $0, \pi/2, \pi$ and $\frac{3\pi}{2}$. If we superpose the 4 values of the signal, evaluated for the four different values of ϕ_{step}, we get

$$s_0 V_0 = \sqrt{\left(\frac{s_0 V_0}{2}\cos(\phi_{beam})+\frac{s_0 V_0}{2}\cos(\phi_{beam})\right)^2+\left(-\frac{s_0 V_0}{2}\sin(\phi_{beam})-\frac{s_0 V_0}{2}\sin(\phi_{beam})\right)^2} \tag{7}$$

A field programmable gate array (FPGA) chip is an array of thousands to millions of logic cells integrated on to a single chip driven by an external clock. The logic cells are controlled by semiconductor switches. The switch states are defined on an onboard PROM (programmable read only memory). The switch states control how the cells are linked, and how they function. The PROM is programmed using a hardware description language. The current FPGAs (1995) are too slow to handle the required 476 MHz processing rate, significant signal conditioning is required before data can be gathered. The signal from the BCM detector is connected to a VXI crate with two digitizers and two decimation boards. A VXI crate is a chassis in which other electronics can be implemented; the crate used has a built in CPU and power supply. The even buckets are digitized by one of the two digitizers and the odd buckets are digitized by the other. The digitizer sends the digitized signal to one decimation board with six FPGAs. The data stream to the FPGAs is decimated by eight; i.e., by sampling one out of every eight passes a charge bunch made so that 7/8 of the data is lost. The proposed system does not require such decimation and can gather all of the data using two boards; one board with a digitizer and an FPGA, a second board with a CPU running Linux, a digitizer, a power supply, a hard disk, a USB interface, and dual port RAM. For further information on the current system please read[1].

MATERIALS AND METHODS

The proposed upgrade plan replaces the VXI crate in each ring with the the new digitization board and the Linux computer board. In short the VXI crates contain twelve FPGAs from 1995 and the new system contains one modern FPGA (Virtex II). The new FPGA will be programmed using Verilog Hardware Description Language (HDL) in the Xilinx synthesis environment.

Verilog HDL is the language used to program the Virtex-II FPGA component of the BCM in the PEP-II storage rings at SLAC. Verilog HDL is a structure for constructing routines that can be implemented onto programmable hardware. The Xilinx ISE 8.1i synthesis environment has an implementation tool that writes the Verilog routines to the switches on the FPGA PROM. ModelSim XE III 6.0d is the program used to simulate how the Verilog routines will be implemented on the FPGA and how the FPGA will operate once programmed.

FPGAs represent a fast and inexpensive method of prototyping and implementing design. Programming is easier and less expensive to alter than a soldered circuit board. The reprogrammable nature of the FPGA also improves the cost effectiveness of the chip. One FPGA can be used in several applications by implementing different HDL routines. FPGAs can be programmed into sections that act independently of each other. The Virtex-II FPGA is replacing twelve older FPGAs by programming the FPGA into six different sections. Each section is programmed as a single small FPGA and runs in parallel with the other sections. The new FPGA will total up the signal from many turns, the computer will use that sum to calculate the value of equation [7].

DISCUSSION AND CONCLUSIONS

The prototype was tested with various computerized test benches and signal generators. The prototype showed that the proposed system is feasible and can be implemented, however

further devlopment is required before the system is ready for application. The proposed system is a Linux computer operating all of the required components to collect and process data from the BCM detector. The Linux computer will be directly interfaced with the SLAC network. Figure 1 compares the proposed system to the current system.

REFERENCES

[1] M.J Chin, J.A. Hinkson, PEP-II Bunch-by-Bunch Current Monitor, Particle Accelerator Conference, Vancouver B.C. , Canada, May 12-14 1997, pg 2235-2237

FIGURES

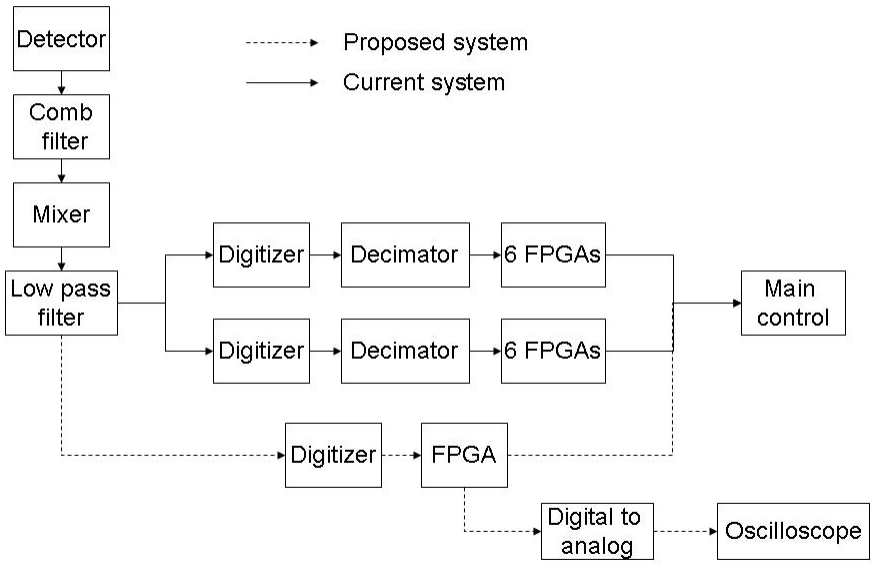

Figure 1: A diagram comparing the old system to the proposed system. The proposed system replaces 6 FPGAs with one and does not need a decimator.