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Analysis of High Power IGBT Short Circuit Failures

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***Abstract*—The Next Linear Collider (NLC) accelerator proposal at SLAC requires a highly efficient and reliable, low cost, pulsed-power modulator to drive the klystrons. A solid-state induction modulator has been developed at SLAC to power the klystrons; this modulator uses commercial high voltage and high current Insulated Gate Bipolar Transistor (IGBT) modules. Testing of these IGBT modules under pulsed conditions was very successful; however, the IGBTs failed when tests were performed into a low inductance short circuit. The internal electrical connections of a commercial IGBT module have been analyzed to extract self and mutual partial inductances for the main current paths as well as for the gate structure. The IGBT module, together with the partial inductances, has been modeled using PSpice. Predictions for electrical paths that carry the highest current correlate with the sites of failed die under short circuit tests. A similar analysis has been carried out for a SLAC proposal for an IGBT module layout. This paper discusses the mathematical model of the IGBT module geometry and presents simulation results.**

***Index Terms*—Current density, High-speed electronics, Insulated gate bipolar transistors, Inductance, Linear accelerators, Power semiconductor devices, Power semiconductor switches, Pulse power system switches.**

I. Introduction

The NLC accelerator proposal at SLAC has selected the solid-state induction modulator approach for its X band klystrons because of its high efficiency, high reliability, and low cost [1]. The topology selected for the modulator consists of 80 off single turn magnetic cores, each driven by its own solid-state switch. The secondary of the modulator has three turns: the total leakage inductance referred to the secondary is low (<20 μH) [1]. To drive the core without using a matched PFN requires a switch that can turn on and off fast at high power levels [1].

The solid-state induction modulator uses high voltage (3.3 kV) high current (4 kA pulses for 10 μs, at 15 V gate-emitter voltage (Vge)) IGBT modules from manufacturer "A" [2]. These IGBTs were developed for traction applications and, although not specifically designed for ultra-high speed pulsed power use, were used successfully in a prototype induction modulator.

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II. Testing of IGBTs

The prototype solid-state induction modulator has been designed, built and tested at SLAC [2]. The manufacturer "A" IGBT modules in the modulator worked reliably during normal operation but many failed during an arc on the secondary. Measurements have shown that peak current through an IGBT module can exceed 15 kA during an arc, with a rate of rise greater than 10 kA/μs [2]. An IGBT test circuit was set up to simulate short-circuit faults on the secondary of the modulator.

Two types of short circuit test have been carried out at SLAC: 'soft' and 'hard' short circuit. A 'hard' short circuit is defined to occur when there is a short circuit present when the IGBT is switched on, whereas a 'soft' short circuit is one that occurs after the IGBT has been turned on. Under ideal conditions, an IGBT facing a soft short-circuit would experience a rise in collector current (Ic) until the IGBT comes out of saturation, at which point the collector voltage would rise and the current would be safely limited by the transconductance of the switch. Ideally, with a gate-emitter drive of +15 V applied, the IGBT die in the manufacturer "A" module would come out of saturation and self limit the module fault current to somewhere around 5 kA.

SLAC performed soft short circuit tests by using the IGBT module to discharge a capacitor through a saturable inductor. Initially the current would rise slowly at a rate limited by the inductance of the circuit. As soon as the core saturated it no longer impeded the current flow and a soft short was represented. Measurements made during the soft circuit test, with an initial collector-emitter voltage of 2.2 kV, are shown in Fig. 1. Unpredicted current and gate waveforms, and IGBT failures, occurred when tests were performed into extremely low inductance (<50 nH) short circuits. A number of failed IGBT modules were carefully dissected and analyzed, in order to determine the mechanisms of failure [2].

III. Overview of IGBT Failure

The design of the IGBT module from manufacturer "A"

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employs a total of 16 IGBT die and 8 anti-parallel diodes. Internally the IGBT module has four identical rafts. Each raft has four IGBT die and 2 anti-parallel diodes as shown in Fig. 2. Emitter and collector busbars (shown in Fig. 3) connect to each raft. The two die closest to the collector busbar are referred to as 'IGBT A', while the two closest to the emitter busbar are referred to as 'IGBT B'.

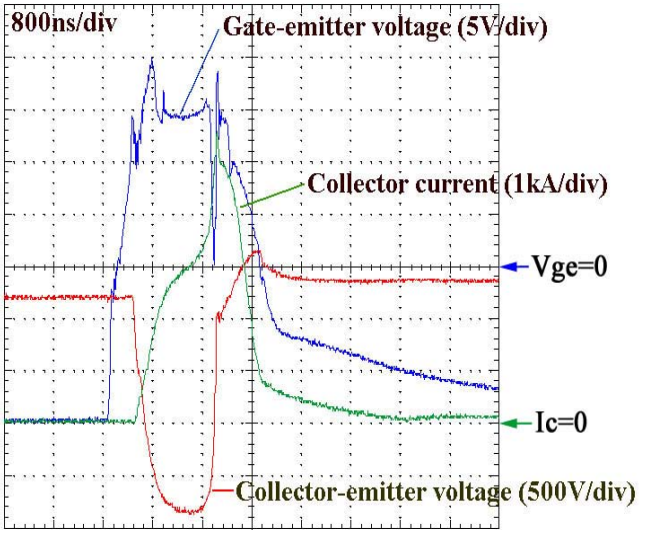

Fig. 1. Measured soft short-circuit waveforms for a manufacturer "A" IGBT module.

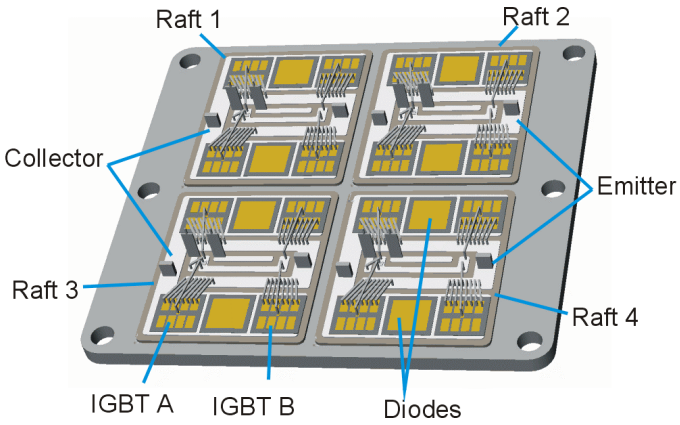

Fig. 2. Internal layout of manufacturer "A" IGBT module.

SLAC opened up 13 failed IGBT modules to determine the position of failure (see Table I). The observed failures all occurred on one of the IGBT die closest to the emitter busbar. Inspection of damaged IGBT modules suggested that asymmetry in the internal layout of the IGBT die was causing a current imbalance which led to IGBT B taking considerably more stress than IGBT A.

TABLE I
LOCATION OF FAILED IGBT DIE ON RAFTS

Raft	Die Position on Raft	Number of Failures
1	IGBT B, top	5
2	IGBT B, top	4
3	IGBT B, bottom	2
4	IGBT B, top	2

IV. IGBT FAILURE INVESTIGATIONS

A. SLAC

In order to understand these IGBT failures, SLAC and TRIUMF undertook parallel investigations; both investigated the assumption that an imbalance in inductances between the electrical paths was to blame. At SLAC various simulations of an IGBT module were performed:

- Circuit analysis using PSpice [3]. The simulation included inductance, calculated using Maxwell3D [4], for the emitter of IGBT A and IGBT B: mutual coupling was not modeled in the PSpice simulation. The simulation predicted a large current spike when the emitter inductances were unmatched (10 nH for IGBT A and 0.01 nH for IGBT B), but showed normal behaviour when these emitter inductances were equal [1];
- Electromagnetic analysis using Maxwell3D: busbars, collector and emitter traces, wire bonds and IGBT die were all modeled as being copper. Hence the IGBT die, in the Maxwell3D simulation, do not have gain or Miller capacitance. A simulated rate of rise of current of between 7.5 kA/µs and 9.4 kA/µs was applied to the IGBT module. The simulations showed that the current density was greatest in IGBT B [2].

B. TRIUMF

At TRIUMF, current sharing between the IGBT die was investigated using the circuit analysis code PSpice. The model included calculated values for self and mutual inductances of the electrical paths, as well as realistic electrical characteristics of the IGBT die.

1) Inductance Model

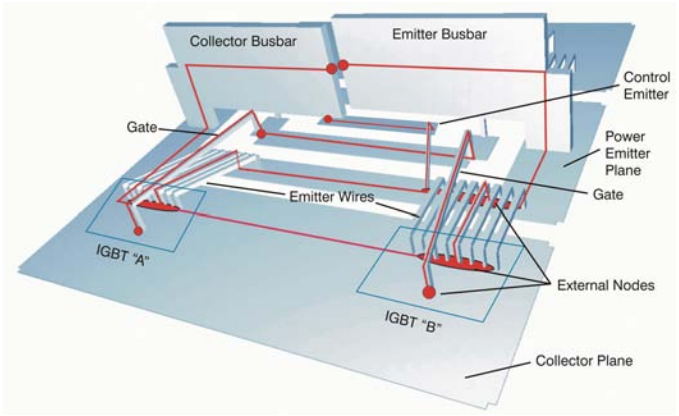

Fig. 3. Raft from a manufacturer "A" IGBT module.

Fig. 3 shows a diagram of a raft from a manufacturer "A" IGBT module. In Fig. 3, the placement of nodes in an equivalent circuit of the IGBT raft are indicated by the dots, and the effective circuit linking these nodes is traced out with lines. The main power connections to the IGBT die are via:

- Collector busbar, to a wide and flat collector plane, to the collector of IGBT A and then to the collector of

IGBT B;

- Emitter busbar, to a power emitter plane:
  - Bond wires connect from the power emitter plane to the emitter of IGBT B.
  - The power emitter continues past IGBT B towards IGBT A: wire bonds connect from the power emitter to the emitter of IGBT A.

The gate drive to the IGBT die is applied via external gate and control emitter terminals.

- The gate connection to IGBT A runs a relatively short distance through a gate trace and then connects to the die via a wire bond. The control emitter connection to IGBT A is through a control emitter trace, then via a wire bond to the power emitter plane, along the power emitter plane, and finally through the wire bonds which connect the power emitter plane to the emitter of IGBT A.
- The gate connection to IGBT B runs through a gate trace and then connects to the die via a wire bond. The control emitter connection to IGBT B is through a control emitter trace, then via a wire bond to the power emitter plane, and finally through the wire bonds which connect the power emitter plane to the emitter of IGBT B.

Fig. 4 identifies the main components of the inductance model derived for two IGBT die: due to symmetry between the upper and lower halves of the raft (Fig. 2), and the pattern of the failures, it was deemed sufficient to model only two of the four IGBT die using PSpice [5].

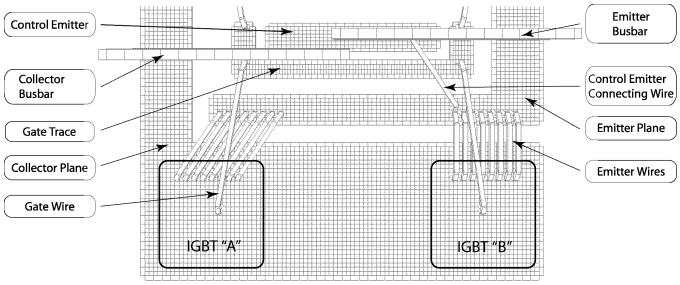

Fig. 4. Basis of circuit model for half a raft from a manufacturer “A” IGBT module.

Fig. 5 shows an image of the lower half of an IGBT raft with an equivalent circuit superimposed to show the location of the inductances to be modeled. The dot adjacent to each inductor indicates the first node of the inductor in the PSpice model, as per “dot” convention, and indicates the positive direction of mutual coupling. There are 8 wire bonds joining each IGBT die to the emitter plane; these are modeled as going straight up, over, and down rather than following a curved trajectory. In Fig. 5:

- LCollectorB represents the inductance out of the collector of IGBT B;
- LCollectorAB represents the inductance out of the collector plane shared by both IGBT A and IGBT B;
- LEmitterA represents the inductance of both the emitter wire bonds and power emitter plane of IGBT A;
- LemitterB represents the inductance of the emitter wire bonds of IGBT B;
- LEmitterAB represents the inductance of the power emitter plane shared by both IGBT A and IGBT B;
- LgateA represents the inductance of the gate wire bond of IGBT A;
- LgateB represents the inductance of both the gate wire bond and gate trace of IGBT B;
- LcontrolEmitter represents the inductance of the control emitter trace and wire bond to the power emitter plane.

Each emitter wire bond touches the collector plane in a different location. However, the circuit model lumps all these wires as one inductance attached to the IGBT die at one node. For this first order inductance model, variations of current density between the eight-emitter wire bonds are ignored and all emitter wires are treated as emanating from a common node.

Fig. 5 shows straight segment conductors as regular inductors. However, inductance is only defined for closed loops, and the inductance depends critically on the chosen return path. A circuit can be treated as being made up of ‘partial inductances’, but this is only valid when a complete loop is considered and all the mutual terms between the partial inductances are considered [6].

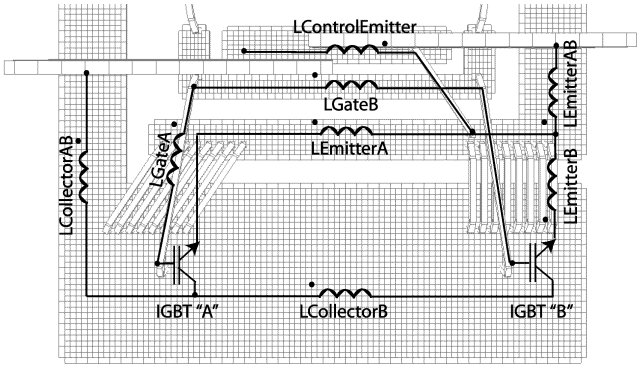

Fig. 5. Equivalent circuit for half a raft from a manufacturer “A” IGBT module.

Codes such as FastHenry [7], Amperes [8] and Faraday [8] are capable of calculating partial inductance. FastHenry, a public domain inductance extractor, was used to calculate the partial inductance matrix for an IGBT raft. FastHenry is a three-dimensional inductance extraction program that computes the frequency dependent resistances and self and mutual inductances between conductors of complex shape. FastHenry simulates the geometry of an object as a collection of rectilinear conductors, and calculates the electrical impedance of the object between various node points.

FastHenry treats the model as a ‘n’ port network. The output of a simulation is a text file impedance matrix showing the direct and trans-impedances across each port at a specific frequency. The result is as if an AC current was applied to one port on the network, and the induced voltage on all ports was

TABLE II
SELF INDUCTANCE (MAIN DIAGONAL) AND MUTUAL COUPLING COEFFICIENTS FOR EQUIVALENT CIRCUIT SHOWN IN FIGURES 5 & 6.

	LCollectorAB	LCollectorB	LEmitterA	LEmitterB	LEmitterAB	LGateA	LGateB	LControlEmitter
LCollectorAB	12.59nH	–0.158	–0.200	–0.086	0.035	0.163	–0.027	0.061
LCollectorB	–0.158	6.45nH	0.353	–0.021	–0.167	–0.034	0.179	–0.196
LEmitterA	–0.200	0.353	11.05nH	0.063	–0.118	–0.219	0.156	–0.173
LEmitterB	–0.086	–0.021	0.063	2.18nH	0.104	–0.101	–0.315	0.047
LEmitterAB	0.035	–0.167	–0.118	0.104	10.63nH	–0.052	–0.192	0.225
LGateA	0.163	–0.034	–0.219	–0.101	–0.052	16.45nH	0.114	–0.054
LGateB	–0.027	0.179	0.156	–0.315	–0.192	0.114	27.96nH	–0.296
LControlEmitter	0.061	–0.196	–0.173	0.047	0.225	–0.054	–0.296	13.80nH

measured. The real and imaginary impedance components give the resistance and inductance values, respectively, seen through the port. The imaginary impedance component on the main diagonal of the output matrix gives the self-inductance; whereas the off diagonal terms of the imaginary impedance component give the mutual inductance. For the PSpice model the mutual inductance term is expressed as a coupling coefficient. Table II shows the calculated self and mutual inductances for the inductors shown in Figs. 5 & 6: the self-inductance terms are on the main diagonal. The off-diagonal terms in Table II are the mutual inductance coupling coefficients.

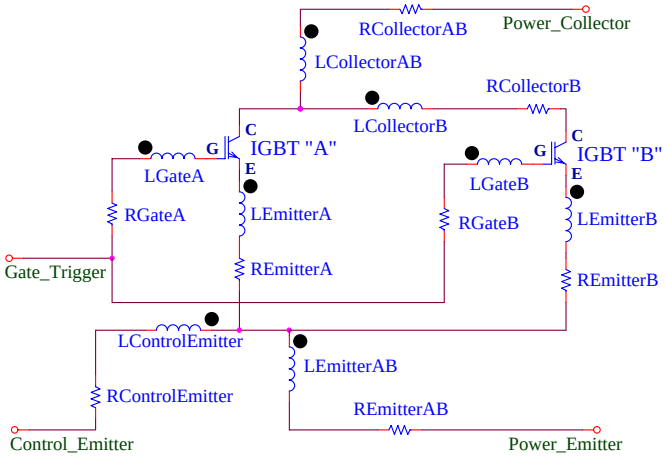

Fig. 6. PSPICE model for half an IGBT raft from manufacturer "A".

2) *PSpice Model of IGBT*

Manufacturer "A" does not supply SPICE models for many of their products. Therefore the PSpice model for an IGBT die was based on an International Rectifier (IR) IRG4PH50U [9] IGBT SPICE model: this IGBT is a single die device. The IR IGBT die model was "tuned" as follows:

- The model parameters were adjusted to give a good representation of the manufacturer "A" data sheet DC transfer characteristics, scaled for one die, at 25°C, with a collector emitter voltage of 20 V;
- Measurements of capacitance of manufacturer "A" IGBT die were carried out. The parameters of an IR IGBT die model were adjusted to give good correlation with the measured voltage dependent capacitances. Fig. 7 shows the measured Miller capacitance (Cgc) and Collector-Emitter capacitance (Cce) for one IGBT die, as a function of voltage: the measurements were carried out for Vce up to 350 V DC. The gate-emitter capacitance simulated is approximately 14.7 nF.

Other modeling considerations were:

- Diodes (Fig. 2) were not modeled since, during turn-on conditions being examined, they are not conducting;
- Only the wire bonds emerging from each IGBT die were modeled. A second set of wire bonds, which daisy chain the two halves of a die, were not simulated.

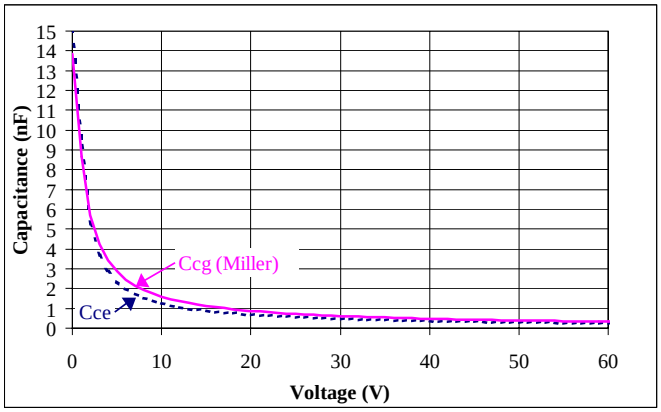

Fig. 7. Measured Miller capacitance (Cgc) and Collector-Emitter capacitance (Cce), for one IGBT die, versus voltage.

The PSpice circuit shown in Fig. 6 closely follows the layout shown in Fig. 5. The self-inductance values are read in from an external file that also contains the mutual coupling terms. The PSpice model represents 1/8th of the 16 IGBT die in the manufacturer "A" IGBT module.

In order to simulate realistic waveforms inside the IGBT module it is necessary to create waveforms, in a circuit external to that of Fig. 6, which are similar to those measured. The PSpice external circuit may not exactly represent the test hardware used. The simulated gate-emitter drive voltage traverses between –15 V and +14 V. The gate drive is applied outside the IGBT module, between "Gate_Trigger" and "Control_Emitter" (Fig. 6); therefore Vge on an individual IGBT die can be different to the externally applied drive. Predictions presented for Vge are between the gate and emitter of the IR IGBT model.

3) *Simulation Results – Normal Operation*

The predicted currents for normal operation are shown in Fig. 8: the maximum current is almost 3 kA per IGBT module

(average of 180 A per each of 16 IGBT die). IGBT B conducts only slightly more current than IGBT A. Assuming uniform current distribution in each IGBT die and that each die has an effective cross-sectional area, for the collector-emitter current, of 80 mm^2 the maximum current density in the silicon is approximately 2.3 A/mm^2.

The current imbalance during the period of rising current is a result of Vge of IGBT A being decreased during this period.

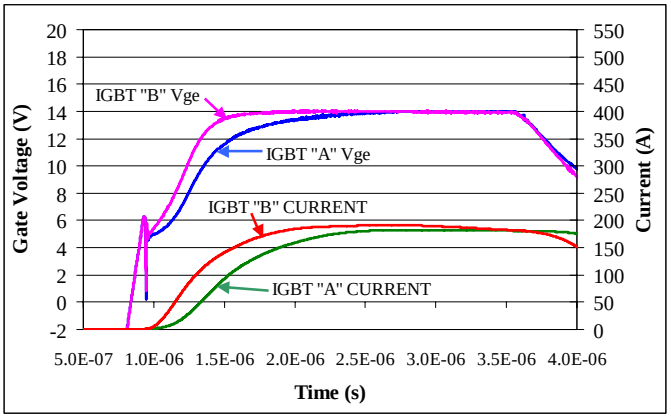

Fig. 8. Predictions for normal operation for two IGBT die in a manufacturer "A" module.

4) Simulation Results – Hard Short Circuit

The simulated gate-emitter drive voltage, for operation with a hard short circuit, has a flattop duration of 800 ns. The maximum current is approximately 5.9 kA per IGBT module (average of 370 A per each of 16 IGBT die). The predicted currents are shown in Fig. 9: not only is the current imbalance significant, the current traces are diverging during the rising edge of the current waveform. This divergence is a result of Vge of IGBT A being decreased by several volts during the period of rising current. IGBT B conducts a maximum current 20% greater than 1/16th of the module maximum current.

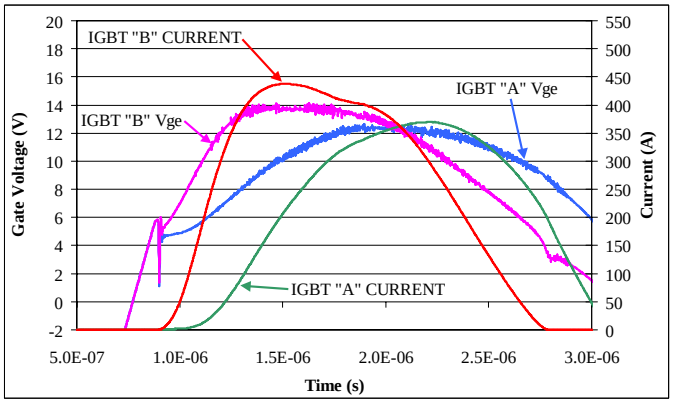

Fig. 9. Predictions for hard short circuit for two IGBT die in a manufacturer "A" module.

5) Simulation Results – Soft Short Circuit

The simulated gate-emitter drive voltage, for operation with a soft short circuit, has a flattop duration of 1.2 µs. The maximum current is 6 kA per IGBT module (average of 375 A per die). The predicted currents are shown in Fig. 10: the maximum current through IGBT B (490 A) is approximately 30% greater than 1/16th of the module maximum current and is a result of Vge of IGBT B being increased by approximately 2.5 V during the period of rapidly rising current. The maximum current through IGBT A is less than 1/16th of the module maximum current and is a consequence of Vge of IGBT A being decreased by approximately 3 V, during the period of rapidly rising current.

Assuming uniform current distribution in each IGBT die and that each die has an effective cross-sectional area, for the collector-emitter current, of 80 mm^2 the maximum current density in the silicon of IGBT B is approximately 6.1 A/mm^2.

Since the soft short circuit leads to IGBT failure, this prediction is further analyzed to understand the reasons for the current imbalance between the die IGBT A and IGBT B.

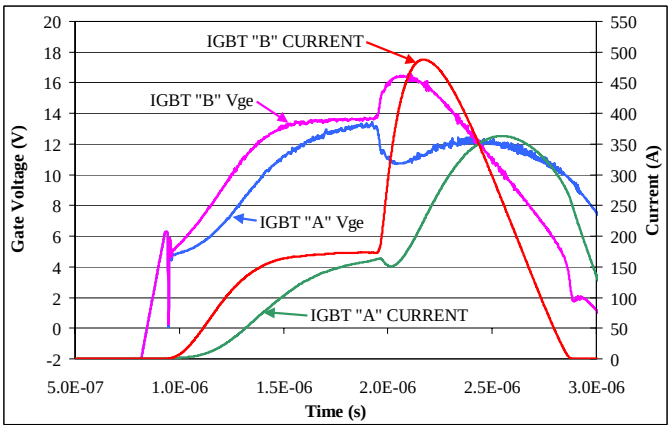

Fig. 10. Predictions for soft short circuit for two IGBT die in a manufacturer "A" module.

V. Analysis of Predictions

IGBT B conducts significantly more current than IGBT A under both hard and soft short circuit conditions (Figs. 9 and 10). However IGBT B fails only under soft short circuit conditions (Table I). Theories were formulated, and tested, for the increase in Vge on IGBT B and the reduction in Vge on IGBT A during soft short circuit conditions:

- Mutual coupling between inductances in the main current paths and connections to the gates (LGateA and LGateB in Fig. 6) – see Table II;
- Mutual coupling between inductances in the main current paths and the control emitter (LControlEmitter in Fig. 6) – see Table II;
- Rising voltage across the collector-emitter of the IGBT die, together with Miller capacitance between collector and gate, causing an increase in gate voltage.
- The presence of a resistor in the gate circuit of each IGBT raft.

A. Effect of Mutual Coupling to Gate Traces

During a soft short circuit Vge for IGBT B rises by almost 2.5 V and the maximum current through IGBT B is 490 A (Fig. 10). To determine the effect of the mutual couplings to the gate traces and gate wire bonds these couplings were set to zero. Without mutual coupling to the gates, the Vge of both

die IGBT A and IGBT B fall by about 3 V upon application of the soft short circuit, and the predicted currents through IGBT A and IGBT B are limited to 320 A and 350 A (Fig. 11), respectively. Hence inductive coupling from the main current paths to the gate traces significantly contributes to current imbalance between the IGBT die. Table II shows that the high current path LemitterB is most strongly coupled to LgateB; however the couplings from the high current paths LemitterAB, LcollectorB and LemitterA to LgateB are significant too.

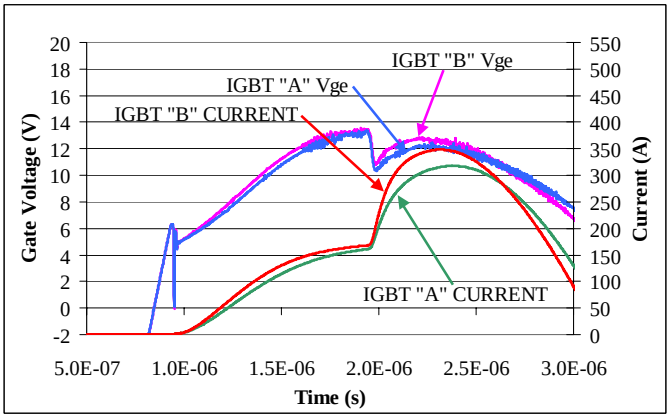

Fig. 11. Predictions for soft short circuit without mutual couplings to the gate traces and gate wire bonds, for two IGBT die in a manufacturer "A" module.

B. *Effect of Mutual Coupling to Control-Emitter*

To determine the effect of the mutual couplings to the control emitter these couplings were set to zero. Without mutual coupling to the control emitter, the Vge of IGBT B rises by about 5 V when the soft short circuit occurs (Fig. 12). As a result the maximum fault current through IGBT B increases from 490 A to 520 A when the mutual couplings to the control emitter are set to zero. Similarly the maximum fault current through IGBT A increases from 360 A to 395 A.

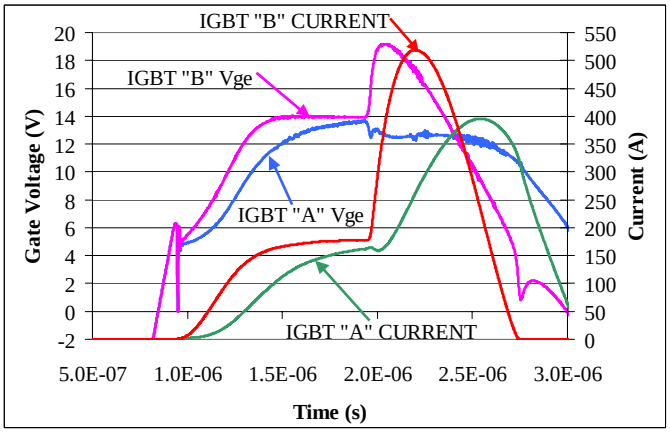

Fig. 12. Predictions for soft short circuit without mutual couplings to the control-emitter, for two IGBT die in a manufacturer "A" module.

Inductive coupling from the main current paths to the control emitter trace helps to limit the maximum current through the IGBT die. Table II shows that the high current path LEmitterAB is most strongly coupled to LcontrolEmitter; however the couplings from the high current paths LCollectorB and LEmitterA to LControlEmitter are significant too.

The control-emitter trace runs parallel to the segment of gate trace that controls IGBT B (Figs. 3 and 5): these traces are physically close, and have a similar geometry. The coupling coefficients from the high current paths LCollectorB, LEmitterA and LEmitterAB, to both LGateB and LControlEmitter are similar in magnitude and therefore the induced voltages tend to have a relatively small effect on Vge of IGBT B. However the coupling coefficient from LEmitterB to LGateB is significantly larger than from LEmitterB to LContolEmitter: hence a rapidly rising current in the emitter of IGBT B couples strongly to its own gate, increasing Vge (see section V.A.).

C. *Effect of Miller Capacitance*

To determine the effect of the Miller capacitance upon the magnitude of current in the IGBT die an additional, non-linear, capacitance was modeled between the gate and collector of each die. Fig. 7 shows the measured Miller capacitance for an IGBT die: the value of this voltage dependent capacitance is approximately given by equation 1.

$$Ccg \approx \frac{20nF}{|Vcg|+1.4} + 28\,pF \qquad (1)$$

Adding a non-linear capacitor per die, whose value is given by equation 1, increases the maximum fault current from 490 A to 500 A, for IGBT B, and from 360 A to 380 A for IGBT A (Fig. 13).

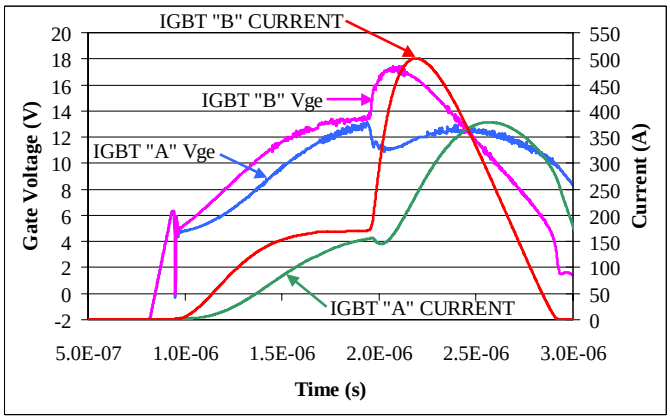

Fig. 13. Predictions for soft short circuit with an additional capacitance per die, between gate and collector, whose value is given by equation 1. Predictions are for two IGBT die in a manufacturer "A" module.

D. *Effect of Gate Resistor*

The PSpice predictions detailed above simulated a resistance of 4 Ω in series with the gate drive for the 2 die: this models the presence of a 2 Ω resistor in the gate circuit of each IGBT raft (IGBT raft consists of 4 die). To determine the effect of the gate resistor, simulations were performed as follows:

- 2 Ω in series with the gate drive for the 2 die;
- 1 Ω in series with the gate drive for the 2 die;

- 0.1 Ω in series with the gate drive for the 2 die.

Halving the gate resistance, to 2 Ω per half raft, decreases the maximum fault current from 490 A to 470 A, for IGBT B, and from 360 A to 340 A for IGBT A (Fig. 14): the maximum current is reduced from 6 kA to 5.6 kA per IGBT module. The reduction in current through IGBT B is a result of a decrease in the peak value of Vge of IGBT B from 16.6 V to 15.8 V.

Further reducing the gate resistance to 1 Ω per half raft decreases the maximum fault current to 450 A, for IGBT B, and to 330 A for IGBT A (Fig. 15): the maximum current is reduced to 5.4 kA per IGBT module.

A gate resistance of 0.1 Ω per half raft decreases the maximum fault current to 425 A, for IGBT B, and to 320 A for IGBT A (Fig. 16): the maximum current is reduced to 5.1 kA per IGBT module. However the PSpice simulations show that, with a gate resistance of less than approximately 0.6 Ω her half raft (0.3 Ω per raft of 4 die) the gate current can start to oscillate, which also results in large transient values of Vge (Fig. 16).

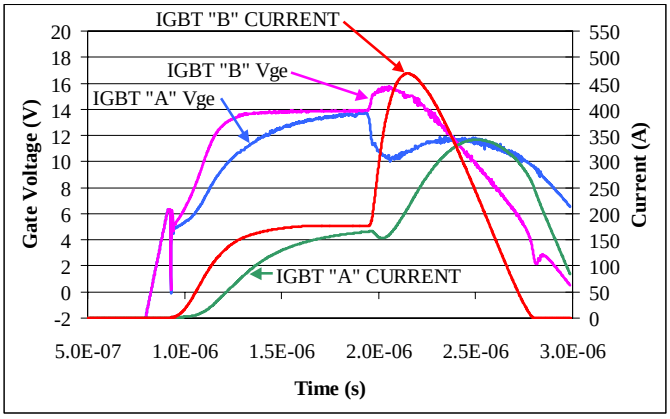

Fig. 14. Predictions for soft short circuit, with 2 Ω gate resistance per half raft, for two IGBT die in a manufacturer “A” module.

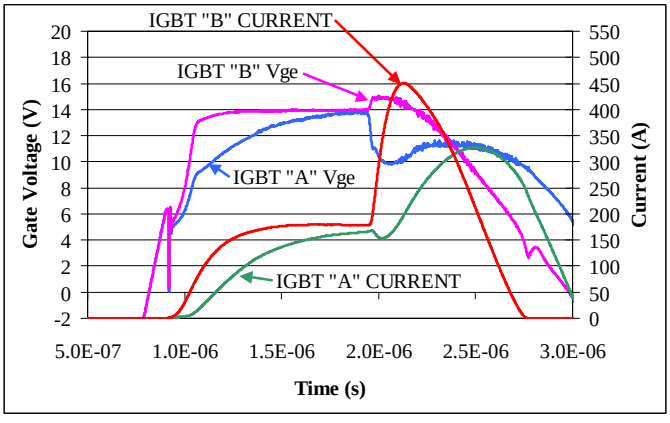

Fig. 15. Predictions for soft short circuit, with 1 Ω gate resistance per half raft, for two IGBT die in a manufacturer “A” module.

The value of the gate resistance significantly affects the magnitude of the fault current, under soft short circuit conditions. Although a lower value of gate resistance results in lower fault currents, and Vge more closely follows the externally applied gate-emitter voltage, the absolute value of current imbalance between IGBT die is not significantly affected.

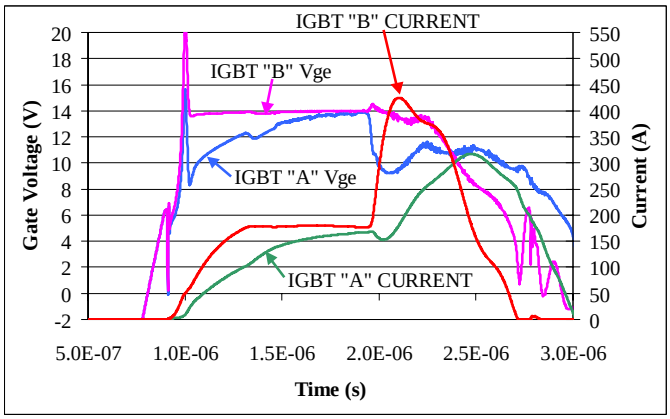

Fig. 16. Predictions for soft short circuit, with 0.1 Ω gate resistance per half raft, for two IGBT die in a manufacturer “A” module.

VI. Analysis of SLAC IGBT

SLAC considered several layouts of IGBT modules to mitigate the current imbalance between die [2]. A modified rectilinear design, consisting of 4 rafts of die, was proposed and built (Fig. 17). The design of the SLAC rectilinear IGBT module is similar to the IGBT module from manufacturer ‘A’ in that it features four identical "rafts" of four IGBT die each, but differs in the geometry of both these rafts and their surrounding casing.

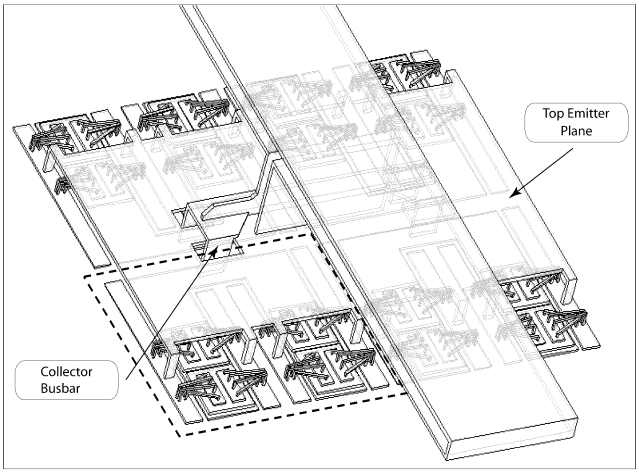

Fig. 17. Isometric view of the SLAC rectilinear 5.0 module. An IGBT raft is shown with a dashed box around it.

Fig. 18 shows a detailed view of one raft of the SLAC rectilinear IGBT module. A preliminary model of this IGBT module, with a gate resistance of 2 Ω per IGBT raft, has been simulated at TRIUMF under soft short circuit conditions: predictions show that this particular layout significantly reduces the current imbalance between IGBT die (Fig. 19). The current imbalance between IGBT die is reduced because the layout reduces induced voltages in the gate-emitter circuits (Fig. 20).

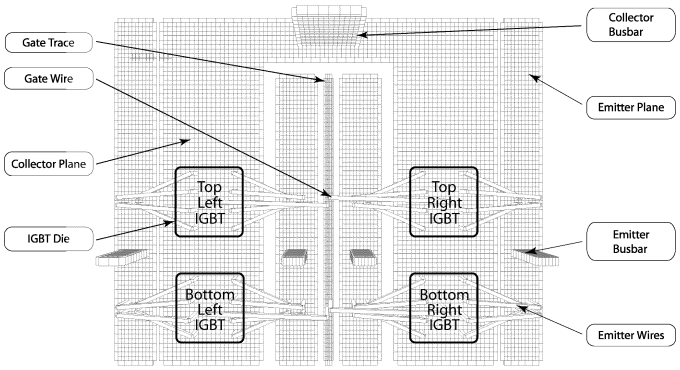

Fig. 18. SLAC rectilinear 5.0 IGBT layout of one raft: the top emitter plane is omitted for clarity.

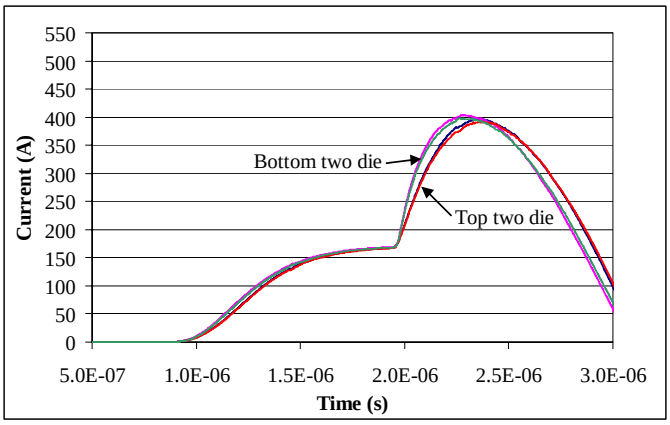

Fig. 19. Predicted current for soft short circuit for one raft of four IGBT die, for the SLAC rectilinear IGBT layout, with 2 Ω gate resistance per raft.

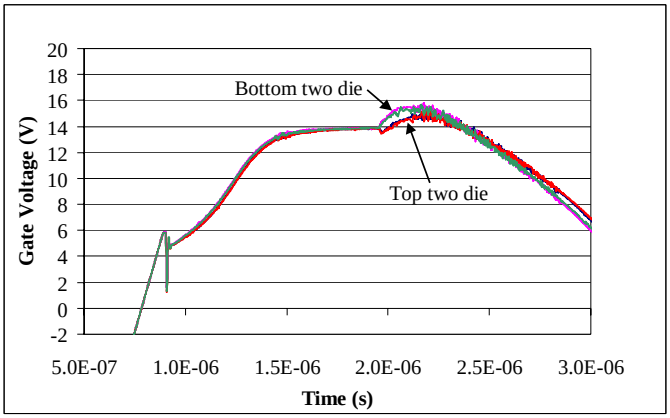

Fig. 20. Predicted gate-emitter voltages for soft short circuit for one raft of four IGBT die, for the SLAC rectilinear IGBT layout, with 2 Ω gate resistance per raft.

Reducing the gate resistance to 0.5 Ω per IGBT raft reduces the maximum current by approximately 25 A per IGBT die.

An additional non-linear capacitor per die, whose value is given by equation 1, to simulate the effect of increased Miller capacitance, increases the maximum current by approximately 12 A per IGBT die.

VII. Conclusion

The research has identified inductive coupling from the power traces to both the gate traces and gate wire bonds as the primary cause of current imbalance between the die in the IGBT module from manufacturer "A". The coupling to the gate circuits can boost the Vge of die above the externally applied gate voltage, and therefore potentially increase the fault current. Hence IGBT module designs intended for high di/dt applications need to pay particular attention to the internal layout relative to the main power paths.

A value of gate resistance of less than 2 Ω, per IGBT raft, results in reduced fault currents, however the absolute value of current imbalance between IGBT die is not significantly affected. A gate resistance of less than approximately 0.3 Ω per raft (of 4 IGBT die) is not recommended as it results in oscillatory gate current.

Preliminary simulations of the SLAC rectilinear IGBT module show that the current sharing between die, under soft short circuit conditions, is good.

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