

Final Report

Pulse Capacitors for Next Generation Linear Colliders

DOE SBIR Phase I Contract DE-FG 03-99ER82840

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March 4, 2000



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Table of Contents

Executive Summary.....	2
I Introduction.....	3
1.1 Applications of High-Voltage Pulse Capacitors.....	3
1.2 Rationale for Nanostructured Capacitors.....	5
2 Experimental Procedure.....	6
2.1 Materials Procurement and Characterization.....	6
2.2 Powder Doping*.....	6
2.3 Fabrication of Multilayer Chip Capacitors (MLCC's)*.....	7
2.4 Electrical Characterization.....	9
2.4.1 Capacitance and Temperature Coefficient of Capacitance (TCC) Measurements.....	9
2.4.2 Insulation Resistance.....	9
2.4.3 Dielectric Breakdown Testing.....	10
2.4.4 Capacitance versus Voltage Measurements.....	10
2.5 Comparison to Commercially Available Devices.....	11
3 Experimental Results and Discussion.....	12
3.1 Properties of BaTiO ₃ Nanopowders.....	12
3.2 Sintering of 1206-Style Chip Capacitors.....	12
3.3 Sintering of 3632-Style Chip Capacitors.....	16
3.4 Properties of Commercial-Off-The-Shelf Components.....	19
3.5 Comparison of Nanostructured Capacitors to State-of-the-Art Devices.....	20
4 Commercial Relevance and Opportunities.....	21
5 Summary of Phase I Results.....	22
6 Literature Cited.....	23

Executive Summary

The objective of this Phase I program was to demonstrate high-voltage multilayer ceramic capacitors (MLCC's) based on nanomaterials technology. To meet this goal, barium titanate nanopowders were fabricated into chip-style components in EIA (Electronic Industries Alliance) package sizes of 1206 (0.120" x 0.060") and 3632 (0.360" x 0.320").

Once the multilayer devices were produced, a sintering study was performed to determine the optimal sintering profile to use with these materials. In this work, temperatures ranging from 1120 to 1140°C and soak times of 1 to 3 hours were evaluated. At the conclusion of these studies, nanostructured MLCC's with the following characteristics were routinely produced:

- Meet the X7R temperatures specification (i.e., capacitance varies by less than $\pm 15\%$ between -55 and 125°C)
- Dielectric constant > 1400
- Dissipation factor < 0.5%
- Chip capacitance x IR (C-R) product > 16,000 Ω F in 3632-style components
- Breakdown voltage > 2,000V (> 50V/ μ m)

Once the process optimization activities were complete, the NRC-produced capacitors were compared to commercially produced devices. Throughout this investigation, the nanostructured capacitors were found to exhibit superior performance characteristics when compared to the commercial components. Furthermore, these advantages are directly attributable to the fine-grain nature of the devices fabricated by NRC.

The term that most dramatically illustrates the advantages of the microstructurally engineered components is the C-R product. As shown above, the 3632-style components produced by NRC possess C-R products in excess of 16,000 Ω F whereas commercial capacitors in both 1825 and 4540 chip formats were found to possess C-R products on the order of 4,000 Ω F. This finding indicates that the use of nanomaterials offers a non-incremental increase in dielectric breakdown strength without sacrificing the capacitance of the material. Thus, both the size and quantity of capacitors needed in high-voltage capacitor banks can be significantly reduced.

This report summarizes the Phase I research effort and compares the properties of the nanostructured capacitors to those of commercial-off-the-shelf devices. Encouraged by these results, NRC plans to pursue Phase II funding to continue the development of this technology.

I Introduction

Pulse capacitors are needed to support emerging technologies in both the government and industrial sectors. Government applications of this technology include use in linear accelerators (DOE), pulsed lasers and directed energy systems (DOD and NASA), and power electronics. Similar applications of this technology also exist in the private sector, with applications ranging from pulsed lasers for the medical and remote sensing communities to power electronics used in industrial and telecommunications equipment.

In each of the above applications, there is a need to improve upon the power handling capability of the ceramic chip capacitors used in these systems. Nanomaterials offers a unique opportunity to develop capacitors that exhibit both higher breakdown strengths and superior dielectric properties without significantly increasing the cost of the components.

The objective of this work was to design, fabricate, and test the performance of nanostructured multilayer capacitors, and to compare the properties of the NRC-produced devices to commercial-off-the-shelf components. This report describes the potential opportunities for fine-grained ceramic dielectrics and summarizes the work performed by Nanomaterials Research Corporation (NRC) under the Department of Energy Phase I SBIR program entitled "Pulse Capacitors for Next Generation Linear Colliders".

1.1 Applications of High-Voltage Pulse Capacitors

Pulse capacitors with improved performance capabilities are needed for use in particle accelerators, solid state lasers, and energy storage systems (see Figure 1). In each of these applications, the capacitor is charged and discharged repeatedly at frequencies ranging from ~ 10 Hz (pulsed lasers) to 120 Hz (linear colliders). Additionally, these components must be able to reliably withstand applied voltages in excess of 5 kV.

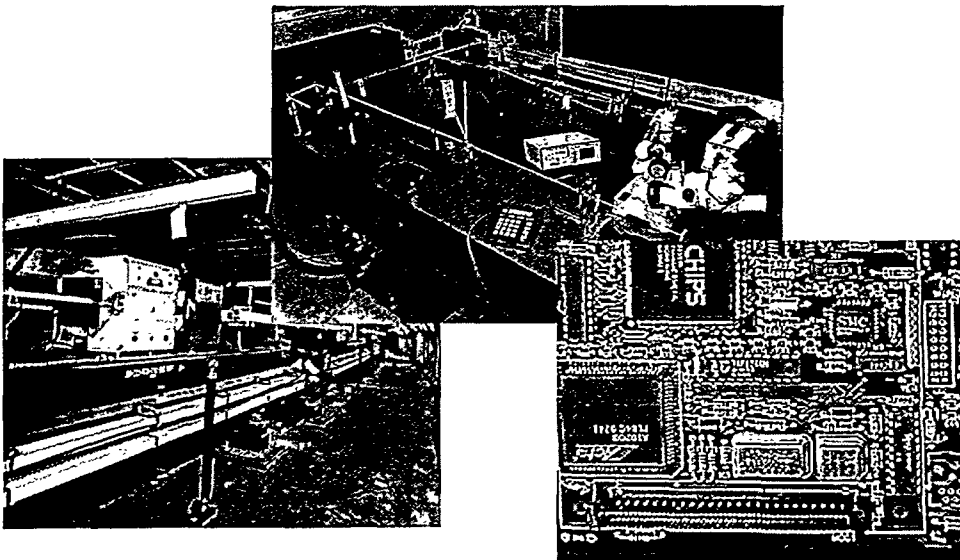


Figure 1. Examples of applications requiring high-voltage pulse power capacitors. These include linear accelerator systems (left), solid state lasers (center), and power electronics (right).

The primary DOE application of pulse capacitors is in linear accelerator systems. For example, the two-mile long linear accelerator, or *linac*, at the Stanford Linear Accelerator Center (SLAC) requires capacitors that operate at a nominal voltage of 5 kV. These components are operated in a partial discharge mode in which they are cycled (i.e., charged and discharged) at 120 Hz. In this system, several independent sections are magnetically coupled to generate 500 kV, 2,000 A pulses. Specific requirements for pulse capacitors include:

- High voltage capability (> 5 kV)
- High capacitance
- Low inductance
- Rapid discharge (< 3 μ sec)
- High reliability (MTBF $> 100,000$ hours)

Similarly, solid state laser systems use capacitive discharges to generate energetic pulses of laser light. For instance, the Nd:YAG lasers that are commonly used in the medical and remote sensing communities typically operate at frequencies on the order of 10 to 20 Hz. As in the previous example, the capacitors used in these systems are repeatedly charged and discharged in a system that requires reliable, high-capacitance components to operate at 500 to 1,000 V.

In addition to the pulsed systems described above, high-voltage capacitors are also used in power electronics and telecommunications systems. These applications also require capacitors that are compatible with high-voltage operation, but in most instances these systems are not operated in a pulsed mode.

As shown in Figure 2, the relative capacitance of ferroelectric ceramic dielectrics decreases when the component is subjected to high voltage conditions. In this example, the relative capacitance decreases to approximately 20% of its nominal value when a voltage equal to one-half its breakdown strength was applied. This behavior is typical of the ceramic capacitors that are currently available in the commercial high dielectric constant marketplace.

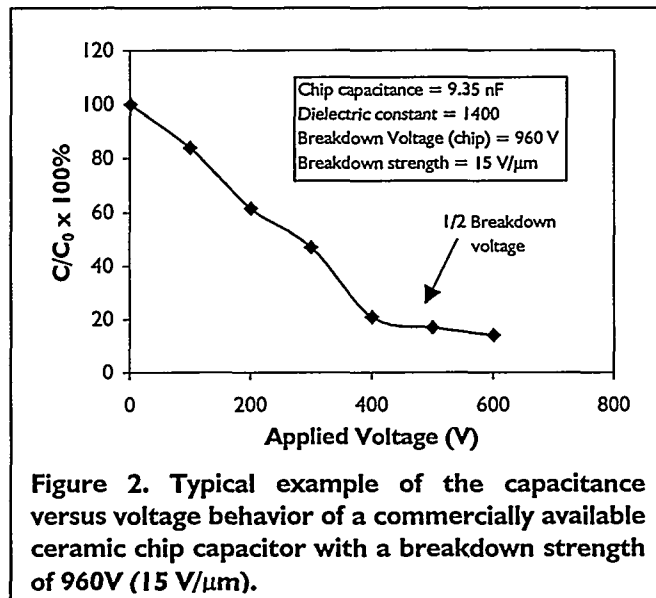


Figure 2. Typical example of the capacitance versus voltage behavior of a commercially available ceramic chip capacitor with a breakdown strength of 960V (15 V/ μ m).

Non-ferroelectric ceramic capacitors, such as NPO devices, are also commercially available. These materials exhibit relatively constant capacitance values when subjected to large D.C. biases. However, NPO ceramics typically possess dielectric constants below 100 and are therefore not practical for use in pulse power or energy storage applications. In high voltage applications it is desirable to use devices with high nominal capacitance values. Otherwise, additional devices must be integrated into the system in order to compensate for the lower capacitance, and these additional components increase both the size of the capacitor network as well as the number of electrical connections.

1.2 Rationale for Nanostructured Capacitors

The current state of the art in high-voltage ceramic capacitors uses BaTiO₃-based dielectrics in which electrically insulating glassy phases are introduced into the grain boundaries. These materials are designed to increase the dielectric breakdown strength of the capacitor, but they also decrease the nominal dielectric constant of the material, and hence the capacitance of the component.

Nanomaterials are a relatively new class of engineering materials in which the mean particle size is typically on the order of 100 nm. In polycrystalline ceramic systems, the extrinsic flaw size is typically on the same order of magnitude as that of the individual particulates. Thus, by developing process technologies that employ nanoscale ceramic powders, devices with inherently small internal defects can be produced. Reducing the extrinsic defect size is particularly important for high-performance dielectric materials that must withstand high operational voltages over long periods of time.

The two properties most influenced by the use of nanomaterials are the dielectric withstanding voltage (DWV) and the insulation resistance (IR). The dielectric withstanding voltage of a ceramic capacitor represents the highest applied voltage that a capacitor can withstand without failing catastrophically and irreversibly. The ability of a dielectric material to withstand these voltages is intrinsically high. However, ceramic capacitors are flaw sensitive brittle materials with extrinsic failure modes. Griffith's classic equation (1) provides the ultimate strength of a brittle material as a function of flaw size [1].

$$\sigma \propto \frac{K_{IC}}{\sqrt{\pi c}} \quad (1)$$

where:

σ = ultimate strength

K_{IC} = critical stress intensity factor (material specific)

c = diameter of the largest internal flaw

Since the critical flaw size in a microstructure is obviously no smaller than the grain size of the material, it follows that a capacitor dielectric containing fine grains has the potential to be more fracture resistant provided that the sizes of the extrinsic flaws (voids, pores) can be minimized. Nanocrystalline materials have the potential to achieve these high strengths and the accompanying elevated breakdown voltages.

The insulation resistance (IR) of a capacitor is quantified by measuring the D.C. current that is passed upon charging of the device. A dielectric microstructure consists of grain boundary and grain interior elements in series. In a nanocrystalline dielectric more inherently resistive grain boundaries are present per unit thickness and thus, the overall insulation resistance of the capacitor can also be increased without sacrificing the part's capacitive properties. Thus, nanomaterials technology offers a unique and revolutionary alternative to the currently used high-voltage dielectrics.

2 Experimental Procedure

2.1 Materials Procurement and Characterization

At the beginning of this program, commercially available BaTiO_3 powders and Pt ink were procured for use in the fabrication of multilayer devices. Cabot BT-16 ceramic dielectric was purchased from Cabot Performance Materials (Boyertown, PA) and 50g of fritless Pt ink was procured from Heraeus Ceramalloy (West Conshohocken, PA).

Once obtained, the nanoscale ceramic powders were completely characterized prior to their use in order to correlate the relationship between the nanoscale microstructure and the performance of the materials produced in this work. Specifically, the following characterization techniques were employed during the Phase I program:

- **Surface area analysis** was performed using a Coulter BET apparatus. This data was also used to estimate the average spherical diameter of the ceramic nanopowders.
- **The average particle size and the particle size distribution** were estimated using Transmission Electron Microscopy (TEM).
- **Phase purity** in the as-produced materials was confirmed via $\text{Cu-K}\alpha$ X-ray diffraction. Impurity analysis was also performed using the Energy Dispersive X-ray Spectroscopy (EDX) feature of the TEM instrument.

The above data is routinely collected for all of the engineering materials used in the manufacture of electronic ceramic components at NRC.

2.2 Powder Doping*

The Electronic Industries Alliance (EIA) specification for X7R dielectrics requires that the components possess the following performance characteristics:

- Capacitance deviates by less than $\pm 15\%$ of the room temperature value between -55 and 125°C
- Dissipation factor < 0.025 (2.5%)
- Insulation resistance $> 100 \text{ M}\Omega$ or the product of the IR and capacitance values is $> 1000 \text{ }\Omega\text{F}$, whichever is less; IR at 125°C is at least 10% of 25°C rating
- Dielectric strength $> 250\%$ of rated voltage for 5 seconds at 50 mA maximum current

To meet these requirements, small amounts of Nb_2O_5 , ZnO , MnO_2 , and Bi_2O_3 were added to the as-received BaTiO_3 powder using a wet chemical process. In this process, the ceramic powder was blended with organic precursors so that the dopant phases were uniformly distributed throughout the material. After drying, the entire powder lot was heated in a vented furnace to remove the organic species.

At the conclusion of this process, a small sample of the material was pressed into several disks and fired. The sintered disks were then tested to ensure the material met the EIA X7R specification.

2.3 Fabrication of Multilayer Chip Capacitors (MLCC's)*

Once the chemically doped barium titanate was available, chip-style multilayer capacitors were produced using a tape casting process [2-3]. As shown in Figure 3, the products of this work were end-terminated ceramic components with interdigitated internal electrodes.

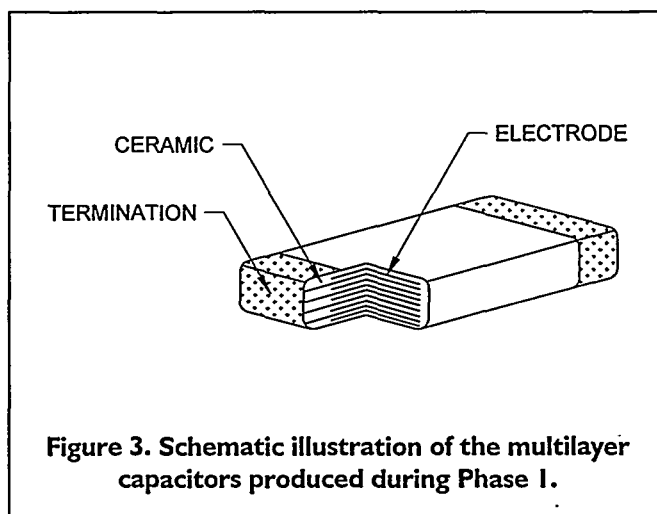


Figure 3. Schematic illustration of the multilayer capacitors produced during Phase I.

Figure 4 shows a flow diagram outlining the steps of the multilayer fabrication process. In this process, the ceramic nanopowder was first dispersed in an organic solvent using a dispersant. The resulting slurry was then attrition milled to break up any powder agglomerates and to fully disperse the nanopowders. Next, a binder and a plasticizer were introduced to the nanopowder dispersion and the slip was ball-milled for an additional length of time to completely dissolve these materials in the solvent.

The slip was cast using a Dreitek model 101 tape casting unit. In this process, the barium titanate tape was cast onto a silicone-coated Mylar® carrier film in a continuous operation in which 10-cm wide tape was produced. As the tape was cast on the Mylar® film, it was dried and rolled onto spools for later use in the multilayer fabrication process. During the Phase I work, 25-meter tapes were produced for use in the manufacture of prototype devices.

Once cast, the tape was cut into 10-cm x 10-cm sheets for use in the multilayer fabrication process. Next, ceramic devices were fabricated by laminating the various layers and removing the Mylar® backing after each lamination step. Figure 4 shows an intermediate step in the lamination process in which the Mylar® backing is being removed from an array of BaTiO₃ capacitors. Once the 10-cm x 10-cm multilayer build-up was complete, the array was diced in accordance with the device design.

Next, the diced chips were heated to 550°C in nitrogen to volatilize the organic constituents. After the burnout cycle was complete, the devices were fired in air at temperatures ranging from 1120 to 1140°C to densify the devices. Finally, a Ag/Pd termination paste was applied to the ends the devices and the termination material was fired to complete the manufacturing process.

During this Phase I program, ceramic capacitors were produced in two package sizes as described by the EIA specifications. The EIA chip designations and device footprints of the components produced in this work are summarized in Table I.

Table I. EIA designations and dimensions of the multilayer capacitors produced during Phase I.

EIA Designation	Length (inches)	Width (inches)
1206	0.120	0.060
3632	0.360	0.320

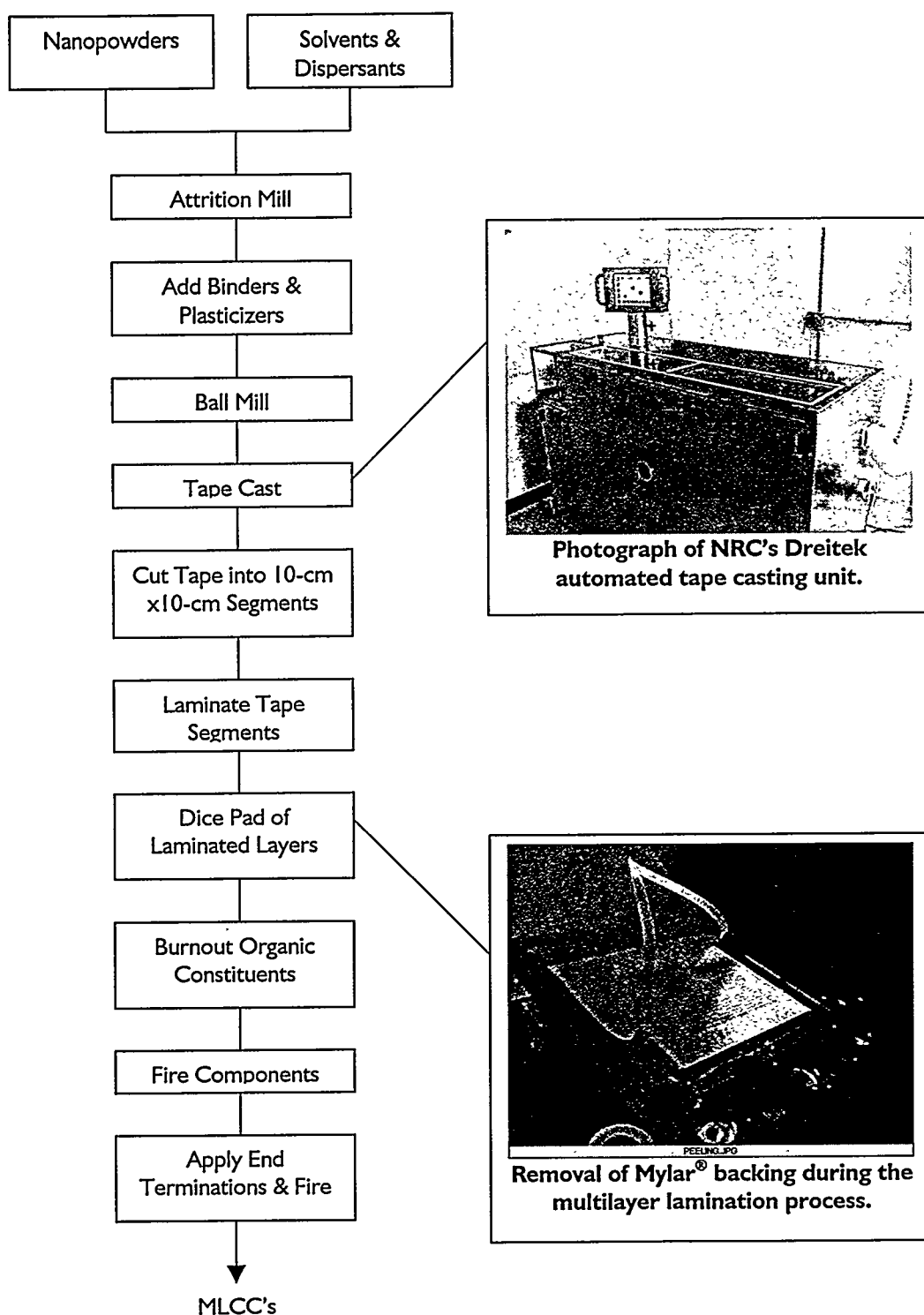


Figure 4. Flow diagram of the multilayer fabrication process.

2.4 Electrical Characterization

The electrical properties of the nanostructured capacitors were measured extensively, and all of the measurements were performed in accordance with the relevant EIA standard on dielectric materials [4]. Descriptions of the various measurement techniques used in the Phase I research are given in the following sections.

2.4.1 Capacitance and Temperature Coefficient of Capacitance (TCC) Measurements

Once the chip-style devices were produced, room temperature capacitance measurements were used to determine the variability associated with various firing profiles and sample lots. The capacitance and dissipation factor ($\tan \delta$) of each capacitor was measured at 1 kHz and 1 V using a Hewlett Packard 4278A Capacitance Meter. From this information, the dielectric constant of the ceramic material was then calculated using the relationship:

$$\kappa = \frac{C_p t}{n \epsilon_0 A} \quad (2)$$

where κ is the dielectric constant, C_p is the capacitance, t is the dielectric layer thickness, n is the number of dielectric layers, ϵ_0 is the permittivity of free space (8.854×10^{-12} F/m), and A is the area under the electrode.

As shown in Figure 6, the temperature coefficient of capacitance, or TCC, was measured between -55 and 125°C using a Hewlett-Packard 4278A Capacitance Meter, a Hewlett-Packard 3488A switch unit, and an environmental chamber. A test fixture was used which enabled the simultaneous measurement of ten (10) specimens per thermal cycle.

Data acquisition was performed using a LabView program that controlled the laboratory instruments and stored the information to a computer via an IEEE 488 interface. The resulting data was then exported to spreadsheets for analysis.



Figure 6. Experimental apparatus for measuring capacitance as a function of temperature.

2.4.2 Insulation Resistance

The insulation resistance (IR) of a capacitor is quantified by measuring the D.C. current that is passed upon charging of the device. In this work, the IR was measured at 25, 125 and 200°C using a QuadTech model 1865 MegOhmmeter/IR Tester. All of the IR measurements were performed using an applied D.C. bias of at least 200V.

2.4.3 Dielectric Breakdown Testing

The breakdown voltages of the MLCC's produced during Phase I were measured using NRC's Hipotronics model HD100 Hipot tester. This instrument has the capability to apply D.C. voltages up to 6 kV. All of the dielectric breakdown testing was performed with the test specimens submerged in dielectric oil to prevent the potential for arcing across the end terminations.

In this procedure, the voltage across the dielectric is increased until the part fails. The dielectric strength of the material (in V/ μm) is then determined based on the thickness of the individual layers within the MLCC structure.

2.4.4 Capacitance versus Voltage Measurements

The capacitance-versus-voltage (C-V) characteristics of the multilayer parts were measured using the static and dynamic measurement techniques described by Love [5]. In this work, the C-V properties were first measured at 20V increments between 0 and 600V using a capacitance meter and a 600-V power supply. From this "static" data, the dielectric constant of each device was calculated at each voltage increment.

In the dynamic method, the dielectric constant of each capacitor was determined by measuring the voltage discharged into a resistor. Using this technique, the dielectric constant was estimated using the following relation:

$$K_v = -\frac{\ell}{\epsilon_0 A R} \left(\frac{d \ln v}{dt} \right)^{-1} \quad (3)$$

where K_v is the dielectric constant, ℓ is the dielectric thickness, ϵ_0 is the permittivity of free space (8.854×10^{-12} F/m), A is the electroded area, and R is the resistor value. The critical aspect of estimating the dielectric constant using this procedure was determining the proper time interval over which to perform the calculation. Figure 7 shows a typical example of the discharge behavior of a ceramic capacitor as a function of time. As seen in this example, the voltage discharge takes place over a very small time interval. Thus, it is important to accurately assess the linear portion of the discharge curve to determine the dielectric constant.

As shown in Figure 7, however, properly identifying the linear region of the discharge curve does yield dielectric constant values that are in good agreement with those obtained using a capacitance meter and a voltage supply. The data shown in Figure 7 is very similar to other devices that were evaluated in the establishment of this measurement technique.

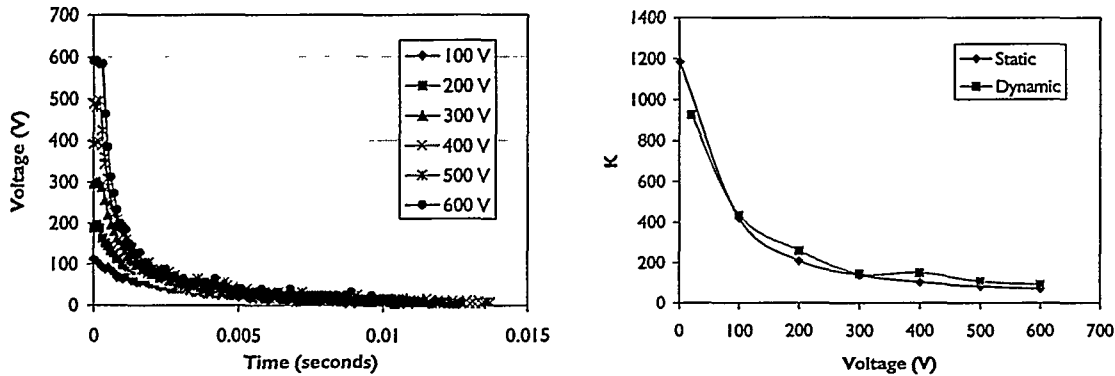


Figure 7. Examples of the voltage discharge behavior (left) and a comparison of the static and dynamic measurement techniques (right) for a ceramic capacitor.

In addition to estimating the dielectric constant, the energy stored at each voltage condition was also determined using the data shown in Figure 1. In this instance, the energy stored, E_v , is determined as follows:

$$E_v = \frac{1}{A\ell} \int_{t_v}^0 i v dt \quad (4).$$

In the above equation, A represents the area under the electrode, ℓ is the dielectric thickness, i is the current, v is the applied voltage, and dt is the time interval.

2.5 Comparison to Commercially Available Devices

In addition to producing and fabricating nanostructured capacitors, the properties of the NRC-produced devices were also compared to two commercially available capacitors produced by Novacap, Inc. (Valencia, CA). The Novacap parts possessed EIA chip sizes of 1825 (0.180" x 0.250") and 4540 (0.450" x 0.400"), and approximately thirty of each capacitor type were tested during Phase I.

The properties of the commercial parts tested in this work included:

- Room temperature capacitance and dissipation factor
- Capacitance versus temperature from -55 to 125°C
- Insulation resistance at 25, 125, and 200°C
- Breakdown voltage
- Capacitance versus voltage at 25°C
- SEM analysis of grain structures

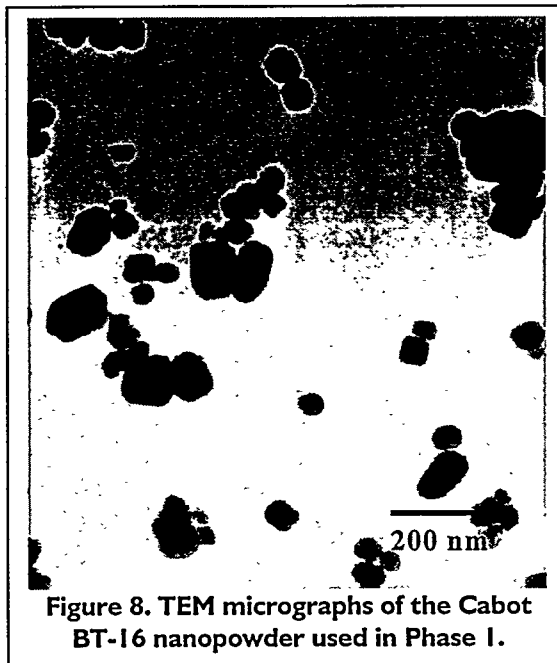
Once these evaluations were complete, the properties of the NRC-produced capacitors were compared to the commercially available devices to identify market areas where the nanostructured devices possess a distinct performance advantage over the existing technology.

3 Experimental Results and Discussion

3.1 Properties of BaTiO_3 Nanopowders

During the Phase I program, approximately 1 kg of Cabot BT-16 powder was consumed in the fabrication of multilayer devices. BET measurements indicate that the powder has a specific surface area of $15.8 \text{ m}^2/\text{g}$, and from this data the average spherical diameter of the nanopowder was estimated to be 65 nm. As shown in Figure 8, all of the powder was less than 125 nm in diameter and a significant portion of the powder was less than 50 nm, thus confirming the BET estimate.

In addition to the particle size analyses, phase-purity in the as-received materials was verified by $\text{Cu-K}\alpha$ X-ray diffraction. The results of this analysis were found to be in good agreement with the data found in the JCPDS database.



3.2 Sintering of 1206-Style Chip Capacitors

The first multilayer devices produced in this work were fabricated into 1206-style chips. Using this case size permitted 300 parts to be obtained from each pad, thus enabling several components to be fired using various processing conditions. As shown in Figure 9, these parts possessed five active layers with a dielectric layer thickness of $35 \mu\text{m}$. These components also possessed electrode thicknesses on the order of $4 \mu\text{m}$.

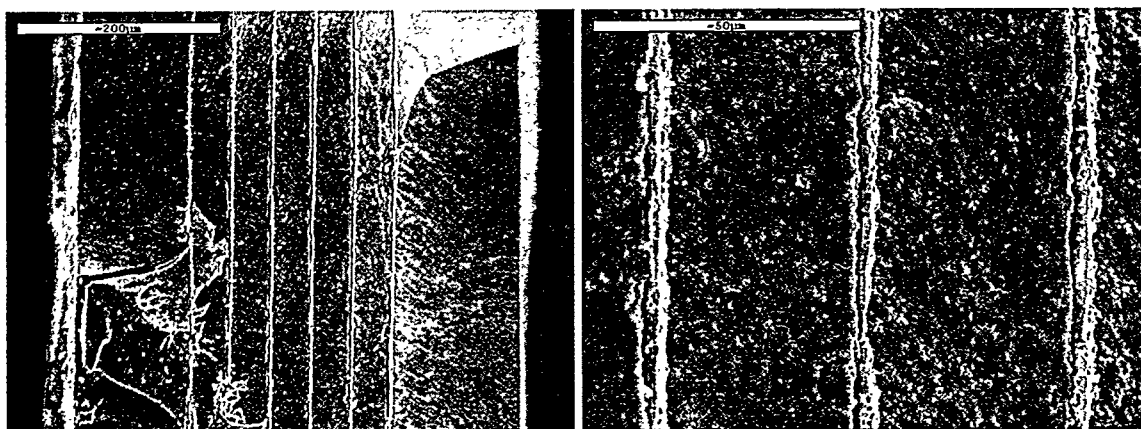


Figure 9. Fracture surfaces of nanostructured BaTiO_3 capacitors from NRC lot number 12061999-01. These devices have $35\text{-}\mu\text{m}$ dielectric layers and $4\text{-}\mu\text{m}$ Pt electrodes.

In this investigation, twenty-five chips were fired at temperatures ranging from 1120 to 1140°C for times of 0.5 to 3.0 hours. After firing, the parts from each sample set were subjected to the full battery of electrical tests discussed in Section 2.4. As shown in Table 2, the best results were obtained by firing the capacitors for 2 hours at 1130°C. Under these conditions, X7R capacitors with a dielectric constant of 1630 and breakdown voltages of 1600 V (or ~ 50 V/ μm) were obtained. As seen in Figure 10, the capacitance values changed by +5% at -55°C and -12% at 125°C, thus meeting the X7R specification.

As seen in Table 2, the capacitors fired for less than 2.0 hours at 1130°C exhibited slightly lower dielectric constants. Increasing either the sintering time or temperature yielded parts with still higher room temperature dielectric constant values, however, the capacitance was found to decrease by more than -15% at 125°C and therefore these components did not meet the EIA X7R temperature specification.

Throughout this work, the dielectric properties of the capacitors within each sample set were found to be very reproducible. For example, Figure 11 shows a control chart for the parts fired at 1130°C for 2 hours. In this instance, both the dielectric constant and the dissipation factor of the capacitors were found to deviate from the mean value by less than $\pm 3\%$

Table 2. Properties of X7R capacitors fired at 1130°C for 1.5 and 2.0 hours.

Property (units)	Soak Time at 1130°C	
	1.5 hours	2.0 hours
Capacitance (nF)	4.13	4.43
Dielectric constant	1525	1650
Dissipation factor	0.56%	0.51%
Number of dielectric layers	6	6
Dielectric thickness (μm)	35	35
Electrode thickness (μm)	4	4
Breakdown voltage (V)	1780	1600
Breakdown strength (V/ μm)	50.8	45.7
IR @ 25°C (Ω)	8.88×10^{11}	8.79×10^{11}
IR @ 125°C (Ω)	1.34×10^9	1.50×10^9
IR @ 200°C (Ω)	9.00×10^6	1.08×10^7
Capacitance x IR @ 25°C (ΩF)	3,667	3,884
TCC	X7R	X7R

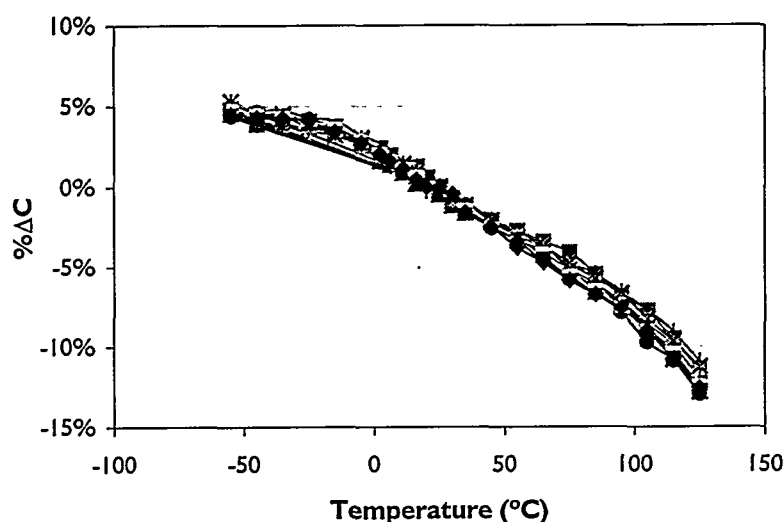


Figure 10. TCC behavior of 1206-style MLCC's fired for 2.0 hours at 1130°C.

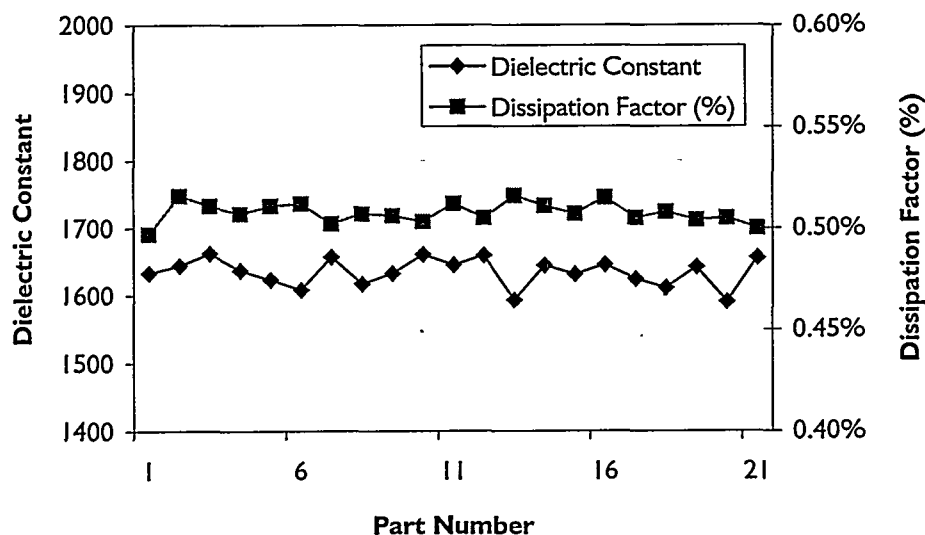


Figure 11. Dielectric constant and dissipation factor values for the 20 1206-style parts fired at 1130°C for 2 hours.

In follow-on experiments, additional 1206 capacitors were fabricated using the same chip design and fired as before. All of these parts were found to possess similar dielectric properties as those previously discussed. After the preliminary tests were complete, the C-V performance of several representative parts were tested using both the static and dynamic methods described in Section 2.4.4.

Although the average breakdown strength was on the order of 2 kV, several components were found to exceed this value by a large margin. As shown in Figure 12, these parts were able to withstand voltages in excess of 3 kV. In this example, discharge measurements were performed

at voltages ranging from 500 to 3,000 V. Over this range, the dielectric constant decreased to approximately 100 while the energy storage capability at 3 kV was 2.5 J/cm³.

Throughout this phase of the work plan, 1206-style capacitors with dielectric constants on the order of 1600 were produced on a regular basis. Furthermore, these parts exhibited high dielectric strengths as compared to commercially available ceramic capacitors. The successful demonstration of capacitors with this combination of properties is a direct result of the use of nanomaterials in device fabrication. These fine-grain microstructures possess a large number of grain boundaries between the internal electrode layers, and this increases the insulation resistance of the devices without decreasing the dielectric constant of the material.

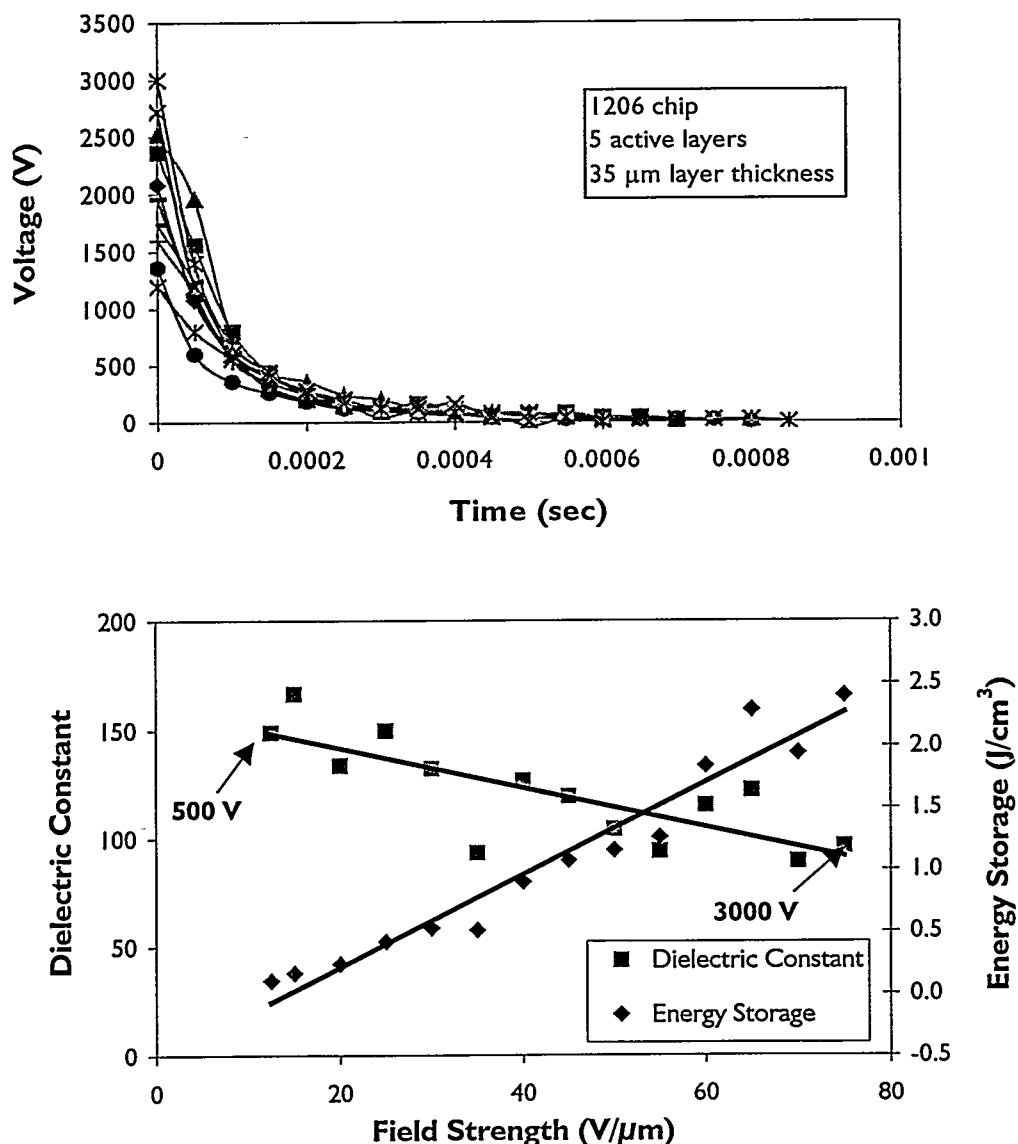


Figure 12. Voltage discharge (above) and dielectric constant and energy storage behaviors (below) of a 1206 chip at applied voltages up to 3 kV.

3.3 Sintering of 3632-Style Chip Capacitors

After evaluating the sintering behavior of the 1206 capacitors, a pad of 3632-style chips was fabricated. These components were fabricated with 15 active layers with a dielectric thickness of approximately 55- μm . Because of the larger component size only 35 parts of this design were obtained from each pad. Therefore, approximately 10 parts were initially sintered for 2 hours at 1130°C.

Using this sintering profile, parts with an average dielectric constant of 1080 and a mean breakdown strength of 1440 V (or 26 V/ μm) were obtained. These values were less than expected, and SEM analyses indicated that the microstructures were not as dense as those of the 1206 components. Therefore, an additional sintering study was performed in order to identify a more appropriate firing cycle for use with these larger components. Table 3 shows the experimental matrix used to evaluate these process variables.

Table 3. Experimental matrix used to evaluate the sintering behavior of the 3632 capacitors.

	1130°C	1140°C
2 hours		
3 hours		

As shown in Figure 13, three of the experimental cells yielded capacitors that met the X7R specification while the fourth cell yielded parts that were just outside of this range. In this investigation, the 3632-style parts fired at 1130°C possessed TCC behaviors that were similar to those of the 1206's fired at lower temperatures. These results indicate that the larger size of the 3632's requires more aggressive sintering cycles in order to achieve the properties obtained in the smaller components. However, that approach must include a careful analysis of the data to ensure that the final products of this work still meet the X7R temperature specification.

All of the 3632-style capacitors produced during this study possessed dielectric constants in excess of 1100. The highest values were found in the parts fired at 1140°C for 3 hours. Although these components were slightly outside the X7R temperature specification, it is likely that similar dielectric constants can be obtained in X7R dielectrics through slight modifications of the sintering profile. Similarly, the devices fired at 1140°C exhibited the highest IR values. This finding is directly attributable to the increased density of the devices. Figure 14 shows the relationship between the sintering temperature and the dielectric constant and IR values obtained in this study.

Based on these results, a follow-on experiment was performed in which additional capacitors were fired at 1140°C for 2.5 hours. As shown in Table 4, capacitors fired under these conditions had dielectric constant and IR values that were similar to those fired at 1140°C for 3 hours, but exhibited a TCC response that met the X7R temperature specification. Accordingly, this sintering profile will be used in the future to process capacitors of this size.

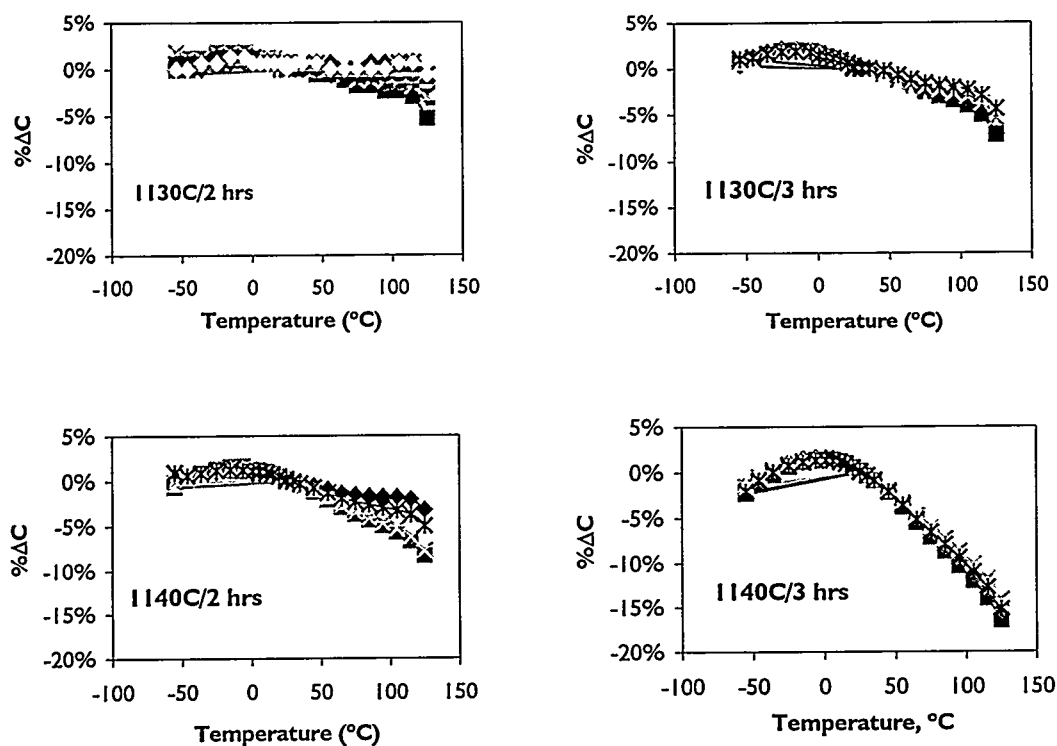


Figure 13. TCC behavior of 3632-style capacitors fired at 1130 and 1140°C for 2 and 3 hours.

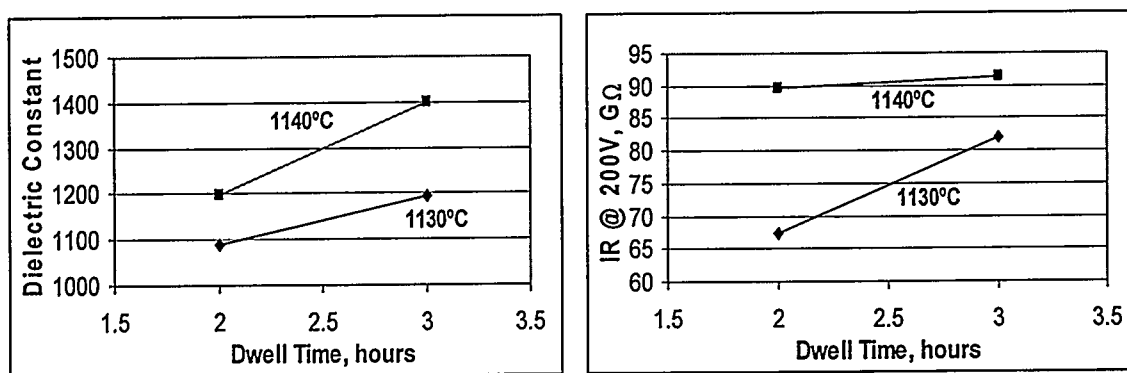


Figure 14. Average dielectric constant and IR values of the 3632-style capacitors fired at 1130 and 1140°C for 2 and 3 hours.

Table 4. Properties of 3632-style MLCC's fired at 1140°C for 2.5 hours.

Property (units)	Value
Capacitance (nF)	184.20
Dissipation factor (%)	0.39
Number of dielectric layers	15
Dielectric thickness (μm)	55
Electrode area (m^2)	5.78×10^{-5}
Electrode thickness (μm)	4
Dielectric constant	1270
Breakdown voltage (V)	1,420
Breakdown strength ($\text{V}/\mu\text{m}$)	25.8
IR @ 25°C (Ω)	8.7×10^{10}
IR @ 125°C (Ω)	3.5×10^8
IR @ 200°C (Ω)	9.0×10^6
Capacitance x IR @25°C (ΩF)	16,008
TCC	X7R

All of the 3632-style parts described above were found to possess dielectric breakdown voltages on the order of 1500V (25 to 30 $\text{V}/\mu\text{m}$). These values are somewhat less than those obtained in the previous work with the 1206-style devices. As shown in Figure 15, all of these parts irreversibly failed near the electrode margin. The likely reason for the decreased breakdown voltage is the generation of stresses near these margins. This portion of a multilayer device is the most susceptible to the generation of stresses during processing and because the area of the 3632 chips is 16 times larger than that of the 1206's the elimination of internal stresses during the device design and processing stages is critical.

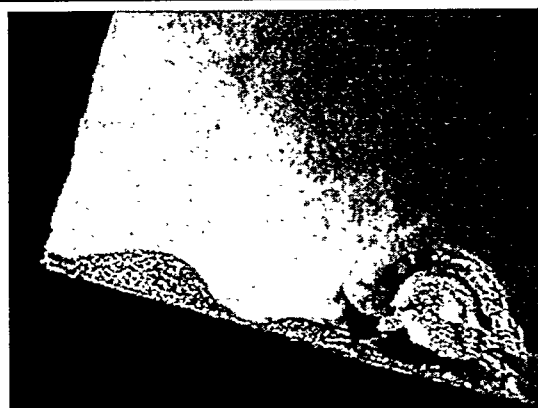


Figure 15. Typical example of the voltage breakdown along the electrode margin within a 3632-style capacitor.

As previously mentioned, the above capacitors possess 55- μm dielectric layers with 4- μm electrodes. Therefore, a key element of the Phase II research will focus on minimizing these stresses through device design and a reduction of the electrode thickness. However, because the 1206 capacitors exhibited such high dielectric strengths, NRC is confident that these design issues can be resolved and that the superior dielectric properties observed in the smaller components can be successfully transitioned into larger case sizes in a timely manner.

3.4 Properties of Commercial-Off-The-Shelf Components

In addition to producing and fabricating nanostructured capacitors, the properties of the NRC-produced devices were also compared to two commercially available capacitors produced by Novacap, Inc. (Valencia, CA). The Novacap parts possessed EIA chip sizes of 1825 (0.180" x 0.250") and 4540 (0.450" x 0.400"). Typical examples of both the 1825 and 4540-style devices are seen in Figure 16.

As shown in Figure 17, both sets of capacitors possessed multilayer structures with 1.5- μ m thick electrodes. This example shows both the multilayer structure as well as the ceramic microstructure for the 4540 devices. The porosity shown in Figure 17 was observed in all of the devices evaluated using scanning electron microscopy. The internal structure of the 1825's was found to be very similar to that of the larger components.

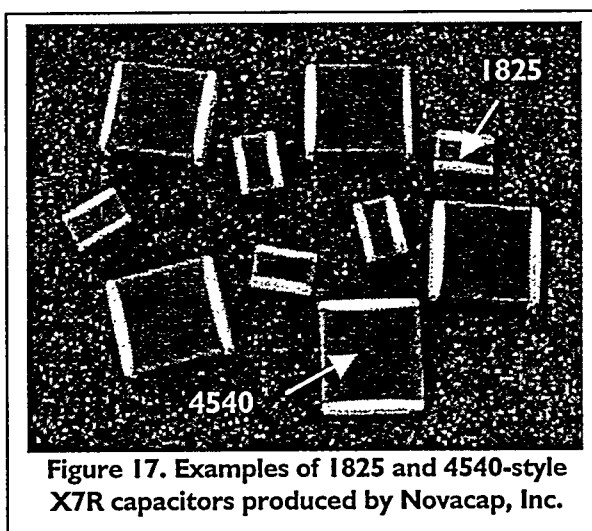


Figure 17. Examples of 1825 and 4540-style X7R capacitors produced by Novacap, Inc.

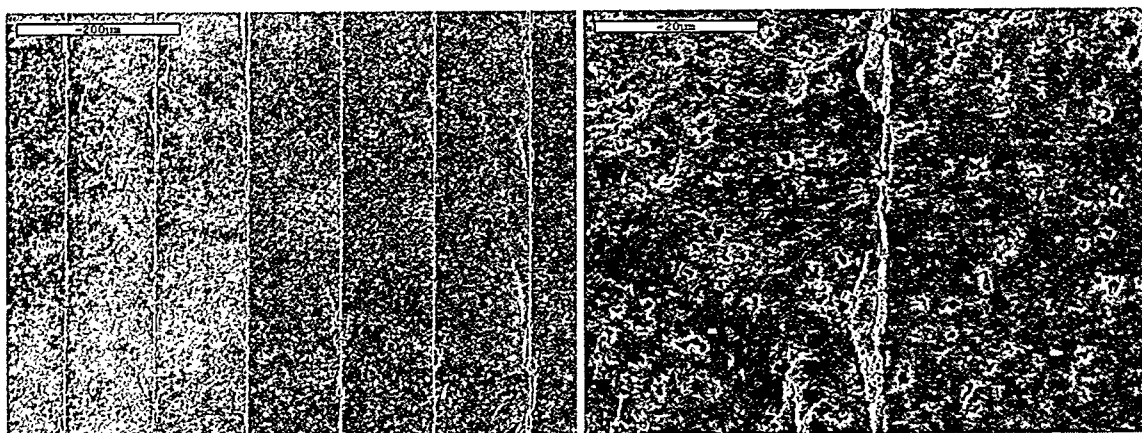


Figure 17. SEM micrographs showing the multilayer structure of Novacap 4540 capacitors with a dielectric constant of 200 and a breakdown voltage in excess of 6 kV.

The properties of the commercially available high-voltage capacitors are summarized in Table 5. In both cases, the devices possess dielectric layer thicknesses in excess of 100 μ m, and had dielectric constants below 700. These relatively low dielectric constants indicate that a glassy phase material, or flux, was added to increase the resistivity of the grain boundary phase. While these additions do increase the breakdown strength and insulation resistance of a dielectric, they also reduce the dielectric constant, and hence the overall capacitance that is achievable within a single MLCC.

Table 5. Properties of high-voltage capacitors procured from Novacap, Inc.

Property (units)	Chip Size	
	1825	4540
Capacitance (nF)	11.03	22.36
Dissipation factor	0.0090	0.0108
Number of dielectric layers	16	24
Dielectric thickness (μm)	160	114
Electrode area (m^2)	1.88×10^{-5}	6.20×10^{-5}
Electrode thickness (μm)	1.2	1.2
Dielectric constant	700	200
Breakdown voltage (kV)	4.1	> 6.0
Breakdown strength ($\text{V}/\mu\text{m}$)	25.6	> 50
IR @ 25°C (Ω)	2.0×10^{11}	1.5×10^{11}
IR @ 125°C (Ω)	1.1×10^9	1.1×10^{10}
IR @ 200°C (Ω)	9.8×10^6	1.1×10^7
Capacitance x IR @25°C (ΩF)	2,206	3,354
TCC	X7R	X7R

3.5 Comparison of Nanostructured Capacitors to State-of-the-Art Devices

Throughout this investigation, the nanostructured X7R capacitors produced by NRC were found to exhibit superior performance characteristics as compared to the commercially available components to which they were compared. As shown in Table 6, both the 1206 and 3632-style capacitors produced by NRC showed dielectric constants in excess of 1,300 and IR values that exceed those of the commercial parts.

The trade-off between the dielectric constant and the insulation resistance is illustrated by the product of the chip capacitance and the IR. In the commercial parts, the dielectric constant was reduced in order to increase the grain boundary resistance of the ceramic. This approach does yield devices with higher breakdown strengths, but it also significantly diminishes the capacitance that is attainable within a single chip.

The use of ultra-fine grain BaTiO_3 powders offsets the need for grain boundary dopants by significantly increasing the number of grain boundaries that occupy the volume between the electrode layers. This increase in the number of grain boundaries yields components that possess higher dielectric constant and insulation resistance values. This is further illustrated in the product of the chip capacitance and IR for these parts. In both the 1206 and 3632-style devices produced at NRC, the product of these two terms was found to be larger than that of the commercial parts. Thus, these findings demonstrate the advantages of nanomaterials and verify the premise behind the Phase I proposal.

Table 6. Comparison of commercially available high-voltage capacitors to the nanostructured devices produced during the Phase I research.

Property (Units)	Novacap/Chip Size		NRC/Chip Size	
	1825	4540	1206	3632
Chip capacitance (nF)	11.03	22.36	4.43	184.20
Dissipation factor (%)	0.90%	1.08%	0.51%	0.39
Number of dielectric layers	16	24	5	15
Dielectric thickness (μm)	160	114	35	55
Electrode area (m^2)	1.88×10^{-5}	6.20×10^{-5}	2.45×10^{-6}	5.78×10^{-5}
Electrode thickness (μm)	1.2	1.2	4	4
Dielectric constant	700	200	1,630	1,270
Breakdown voltage (V)	4,100	> 6,000	1,600	1,420
Breakdown strength (V/ μm)	25.6	> 50	45.7	25.8
IR @ 25°C (Ω)	2.0×10^{11}	1.5×10^{11}	8.8×10^{11}	8.7×10^{10}
IR @ 125°C (Ω)	1.1×10^9	1.1×10^{10}	1.5×10^9	3.5×10^8
IR @ 200°C (Ω)	9.8×10^6	1.1×10^7	1.1×10^7	9.0×10^6
Capacitance x IR @25°C (ΩF)	2,206	3,354	3,894	16,008
TCC	X7R	X7R	X7R	X7R

Finally, as shown in Table 6, the 3632-style capacitors produced by NRC exhibited breakdown voltages on the order of 1500V (or $\sim 30\text{V}/\mu\text{m}$) whereas the 1206-style devices had much higher breakdown strengths. The decreased breakdown voltage of these larger components is attributable to stresses generated at the electrode margins. To offset these stresses, the electrode thicknesses can be reduced by at least 50%. As seen in Figure 17, the Novacap devices possess electrode thicknesses on the order of 1.5 μm and do not exhibit the same dielectric breakdown mechanism as that shown in the parts with thicker electrodes. Nevertheless, the nanostructured capacitors showed similar breakdown strengths even with these internal stress points in the multilayer structure.

Reducing the electrode thickness is readily achievable with conventional multilayer processing equipment. Unfortunately, the time constraints of the Phase I program did not permit that aspect of this work to be performed. However, that effort will be included in the Phase II work plan and NRC is confident that these efforts will yield 3632-style components with dielectric breakdown strengths approaching those obtained in the smaller components.

4 Commercial Relevance and Opportunities

The development of nanostructured high-voltage components can serve to fill a defined and existing niche in the ceramic capacitor market. Once fully developed, a new class of capacitors that are capable of operating at high voltages will be introduced into the marketplace. The ability to manufacture capacitors that exhibit these exceptional properties is a direct result of the nanocrystalline grain structure in the capacitor. Specifically:

- These capacitors exhibited an abnormally high insulation resistance. The data presented in Table 6 shows that the C-R product of the nanostructured 3632 capacitors was significantly greater than that of the comparable capacitors. A higher insulation resistance translates directly to a lower current passed and a lesser power (I^2R) dissipation. This is important since a common failure mechanism in multilayered capacitors is thermal runaway that results from the self-heating of the capacitors.
- These capacitors exhibited an exceptionally high dielectric breakdown voltage. The high breakdown voltage is believed to be a product of two features. The small flaw size in the capacitor is partially attributable to the high breakdown strength since the physical strength in a brittle capacitor material is proportional to the inverse square of the flaw size. The high insulation resistance is also attributable to the high breakdown voltage since the microstructure can withstand higher voltages before thermal runaway and the associated failure occurs.
- The process used to fabricate these devices is amenable to the manufacture of larger components that can be designed to operate at still higher voltages.

For the past three years, NRC has worked extensively to develop nanostructured multilayer devices that exhibit superior performance characteristics as compared to existing devices. Furthermore, NRC was recently awarded a patent [6] for this technology and the company is currently working to identify suitable markets in which to introduce this technology.

5 Summary of Phase I Results

During this Phase I program, nanostructured ceramic chip capacitors with high-voltage capabilities were successfully demonstrated. As shown in Figure 18, this work included the fabrication and testing of both 1206 and 3632-style devices.

Throughout this investigation, the use of ultra-fine ceramic powders yielded devices with performance characteristics that exceeded those of the commercially available capacitors to which they were compared. Most notably, the nanostructured devices exhibited higher dielectric constants and higher insulation resistance values than the commercial parts.

The properties of the nanostructured capacitors that make them particularly useful for pulse power applications include:

- Meet the X7R temperatures specification (i.e., capacitance varies by less than $\pm 15\%$ between -55 and 125°C)
- Dielectric constant > 1400
- Dissipation factor $< 0.5\%$
- Chip capacitance \times IR product $> 16,000 \Omega\text{F}$ in 3632-style components

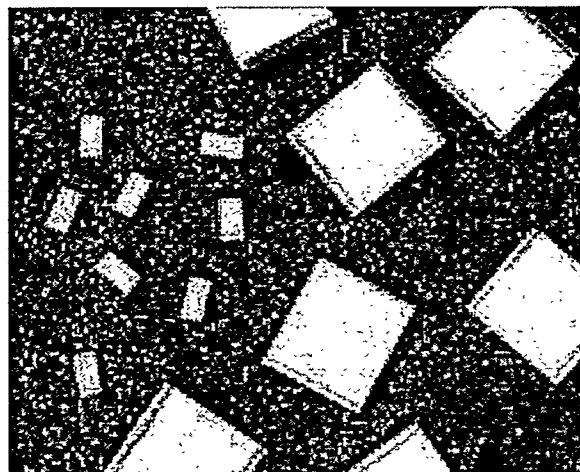


Figure 18. Nanostructured capacitors produced by NRC using 1206 and 3632 case sizes.

- Breakdown voltages $> 2,000\text{V}$ ($> 50\text{V}/\mu\text{m}$)
- Discharge times of ~ 1 msec

The improved properties of the capacitors produced by NRC are attributable to the microstructure of these materials. As previously mentioned, the capacitors produced during Phase I were found to possess average grain sizes on the order of 500 nm. The use of nanoscale ceramic powders increases the number of grain boundaries between each internal electrode pair and thus increases the insulation resistance of the device without compromising the capacitive nature of the material.

Conversely, the insulation resistance of commercial components is increased by adding a glassy phase, or flux, into the grain boundaries of the ceramic. The presence of these secondary phases does increase the insulation resistance and breakdown voltage of the device, but it also suppresses the dielectric constant of the material. Thus, NRC was able to fabricate 180-nF capacitors in a 3632 chip format whereas larger commercial parts possessed capacitance values on the order of 20 nF.

The advantage of the nanostructured materials is most evident when the C-R product of the various devices are compared. In this work, the 3632-style capacitors produced by NRC exhibited a C-R product of approximately 16,000 ΩF whereas the commercial parts possessed C-R products on the order of 4,000 ΩF . This finding is particularly important in the development of high-voltage dielectrics because it enables the production of components with a combination of higher capacitance and enhanced breakdown strengths. This finding is particularly important for high voltage, pulse power applications because it reduces the number of capacitors (and connections) needed to fabricate capacitor banks.

Based on these encouraging results, NRC plans to submit a Phase II proposal to further develop and qualify these devices for use in both government and industrial systems.

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