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A SPICE Model and Electrostatic Field Analysis of the MOS Turn-Off Thyristor

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DISCLAIMER

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A SPICE Model and Electrostatic Field Analysis of the MOS Turn-Off Thyristor

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ABSTRACT

This paper presents a circuit model and an electrostatic field analysis with an approximate model of the SDM170HK MOS turn-off thyristor (MTO) fabricated by Silicon Power Corporation. The circuit model consists of five cells, each containing two bipolar junction transistors and three resistors. The turn-off feature of the MTO was simulated by inserting an array of 21 Fairchild FDS6670A MOSFET importable sub-circuit components between the cathode and the turn-on gate. The model was then used to create a four-terminal sub-circuit component representing the MTO that can be readily imported into computer-aided circuit design programs such as PSPICE and Micro-Cap. The generated static I-V characteristics and simulated switching waveforms are shown.

The electrostatic field analysis was done for the maximum operating voltage of 4.5 kV using the Ansoft Maxwell 3D field simulator. Electrostatic field magnitudes that exceed the nominal air breakdown threshold of 30 kV/cm were observed surrounding the simulated turn-off gate wire, the turn-off gate ring contact, and the cathode ring contact. The resulting areas of high fields are a concern, as arc track marks have been found on the inner surface of the ceramic insulator near the internal gate connections of a failed device.

INTRODUCTION

The increasing demand for a high-power, controllable switch led to the development of the gate turn-off thyristor (GTO). However, the GTO requires a complex gate drive circuit and has a low reverse-biased safe operating area, which are its two major drawbacks [1-2]. The MOS turn-off thyristor (MTO) is a MOS-GTO hybrid device that attempts to solve these problems by externally mounting a number of low on-resistance discrete power MOSFETs that have one set of terminals connected to the gate of the GTO. Several devices of this type are presently commercially available. Another proposed configuration has the power MOSFETs integrated into the four-layer GTO structure during the semiconductor processing [3].

The MTO is a four-terminal device. It has the same appearance as the GTO except for the additional turn-off gate terminal. The circuit symbol and equivalent circuit of the MTO are shown in Fig. 1.

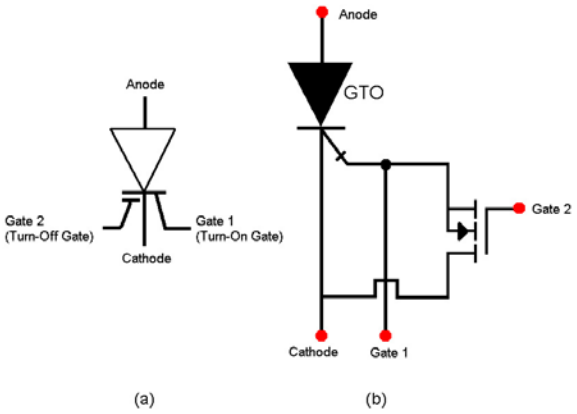


Figure 1. (a) Circuit symbol and (b) equivalent circuit of the MTO.

In order to help baseline this emerging high-power switch technology, a circuit model was created and an electrostatic field analysis with an approximate model was performed for the Silicon Power Corporation (SPCO) SDM170HK MTO. The SDM170HK is rated to have a maximum blocking voltage of 4500 V and a peak controllable cathode current of 500 A. Key values from the device specification sheet [4] are given in the Appendix, Table A.1. A photograph of the device is shown in Fig. 2.

Figure 2. Photograph of the SDM170HK MOS Turn-Off Thyristor fabricated by Silicon Power Corporation.

A number of power semiconductor modeling techniques have been used for circuit simulation in recent years [5]. The more accurate models are based on first principles, requiring solutions to a large system of nonlinear device physics differential equations. The lumped-charge approach [6-7] simplifies the calculations considerably by subdividing the device structure into several charge-storage and connection nodes and applying basic equations from device physics and circuit theory. Attempts have been made to make lumped-charge models for the GTO compatible with SPICE [8-9]. The disadvantage of all physically-based models is that they require a knowledge of internal device geometry and doping impurity concentrations, which is usually unavailable to the application circuit designer.

Circuit models that are not physically based rely on measured device parameters without detailed consideration of device physics. These functional or “black-box” models are less accurate and cannot predict device behavior under all operating conditions. Typically circuit component values for a functional model are determined by making external DC and transient behavior measurements, and the resulting models can be easily imported as sub-circuit components into SPICE-equivalent software packages. Functional models also require minimal computational effort.

One functional model for the GTO uses a set of two-transistor and three-resistor (2T-3R) cells, which is an extension of the classical two-transistor analogy for a four-layer device. The three resistors are added so that the model can simulate S-type negative differential resistance [10]. The model presented in [10] has been tuned with physical insight into the single island turn-off mechanism [11]. Figure 3 illustrates the basis for using the 2T-3R cell for modeling the GTO with SPICE.

This approach uses variation of the 2T-3R cell model suitable for the MTO was to model the SDM170HK by connecting specific available MOSFET circuit models to the gate and cathode terminals of the GTO model. The developed circuit model for the SDM170HK uses the SPICE-compatible Micro-Cap software package and a SPICE-equivalent importable sub-

circuit component to create a packaged component into a library file.

The electrostatic field analysis was done using the Ansoft Maxwell 3D field simulator. The simulator uses finite element analysis to solve for the fields in the defined model under a given set of boundary conditions. An approximate electrostatic model of the MTO was created for the SDM170HK that incorporated measurements of both internal and external part dimensions and estimated material properties. The field modeling was performed to investigate the cause of a device failure, as arc track marks have been found on the inner surface of the ceramic insulator near the gate wire feedthroughs of a failed device.

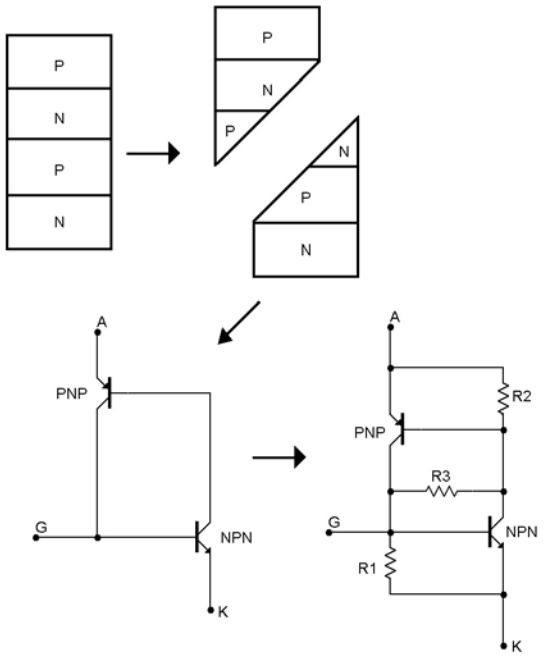


Figure 3. The basis of the 2T-3R cell for a functional SPICE model of the GTO.

CIRCUIT MODEL

The basic structure [3, 12] of the semiconductor body of the MTO is the same as typically used in a GTO. Figure 4 is a representation of the four-layer structure, including the position of one of the power MOSFETs used for turn-off.

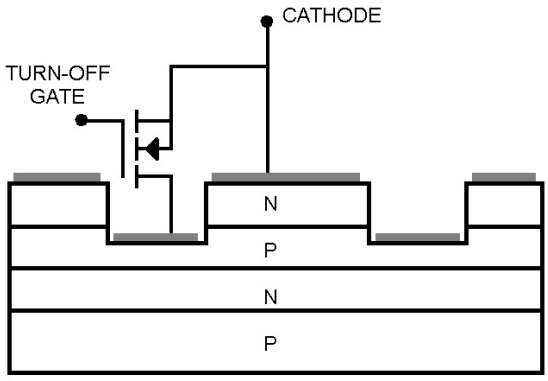


Figure 4. The basic structure of the semiconductor body of the MTO.

One end layer is the p-type anode layer, and the opposite end layer is the n-type cathode layer. The p-type layer that is contiguous to the cathode layer is called the gate layer.

The cathode layer is divided into a multi-island structure forming many elongated protrusions, or "fingers," upon each of which is deposited a metal layer that directly contacts the cathode terminal. The cathode layer, which surrounds these fingers, is removed to leave the gate layer exposed. A metal contact layer is deposited over the exposed portions of the gate layer. Each power MOSFET is placed between the gate layer contact and the cathode terminal, creating a bypass of the gate/cathode p-n junction when the MOSFET is switched to its low-resistance "on" state.

The cathode fingers extend radially from the center of the silicon wafer in a set of concentric ring-shaped arrays. Physical measurements taken of the cathode fingers are given in Table A.2. The overall circuit model for the GTO proposed in [10] consists of a parallel interconnection of several 2T-3R cells, each representing one of the ring-shaped arrays. Figure 5 shows a five-cell GTO model based on the circuit model in [10] for simulating a GTO with five concentric rings of cathode fingers.

The RGCs in Fig. 5 are the gate contact resistances. The RKCs are cathode contact resistances used to model non-uniform current densities entering the cathode fingers. The LMs are for modeling non-uniform island currents that result from mutual inductive coupling between cathode islands [10]. Values for the RGCs, RKCs, and LMs can be found by curve-fitting the circuit simulation switching waveforms to measured data.

The relationship of the values of R1, R2, and R3 to the DC device performance parameters is given in [10], as is the prescription for choosing transistor parameters. The details of the transistor parameter selection algorithm are given in [11].

Figure 6 shows the extension of the 2T-3R cell model for the GTO to create an MTO model. Because the power MOSFET array in the MTO is placed to bypass the gate/cathode p-n junction in the silicon wafer, the MOSFETs in the model are connected to simulate the same bypass. In the model, the drain terminals of the MOSFETs are connected to the base of the NPN transistor, and the source terminals are connected to the cathode.

The 4500V, 500A SDM170HK MTO from Silicon Power Corporation (SPCO) contains a GTO pellet with five concentric rings of fingers. Twenty-one discrete power MOSFETs are connected in parallel between the gate of the GTO pellet and the cathode. The MOSFETs are Fairchild FDS6670A single n-channel, logic level, PowerTrench® MOSFETs.

The complete circuit model for the SPCO SDM170HK is shown in Fig. 7. R1, R2, and R3 for each cell are designated with subscripts ($R1_i$, $R2_i$, $R3_i$). The MOSFET circuit models in Fig. 7 are Fairchild FDS6670A importable sub-circuit component models that can be found in most SPICE-equivalent software libraries.

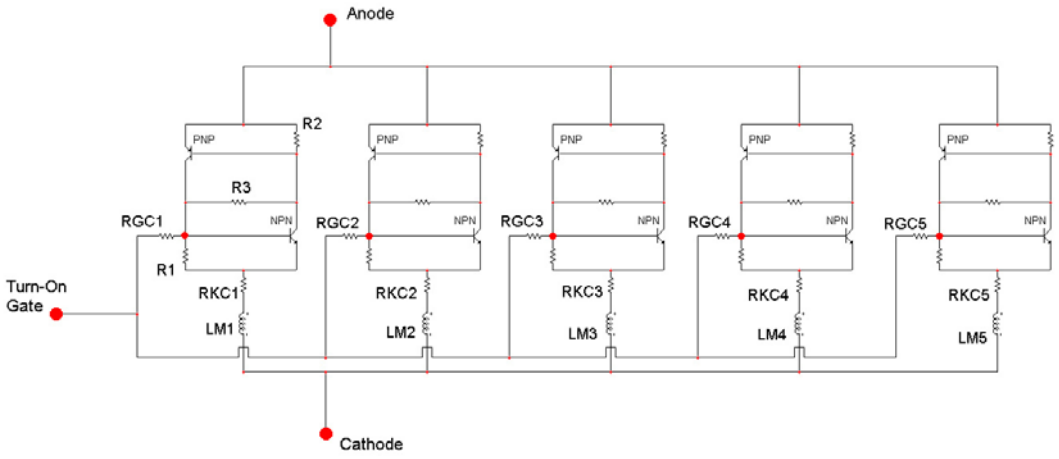


Figure 5. Basic Five-Cell GTO Model.

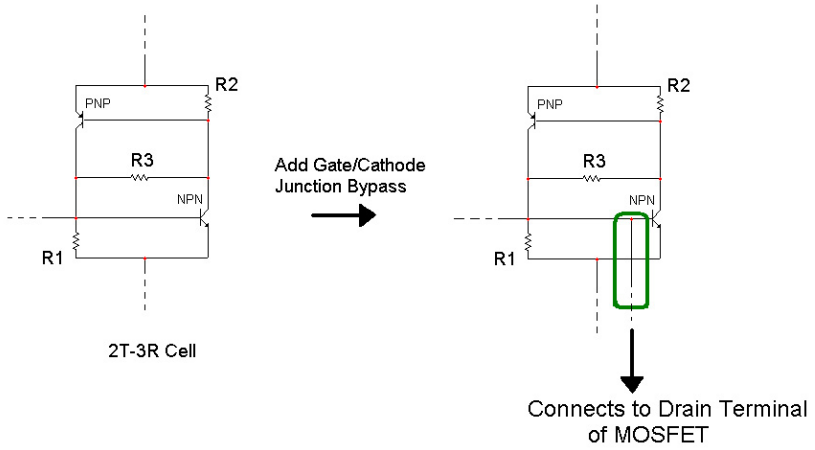


Figure 6. Extension of GTO cell to MTO cell.

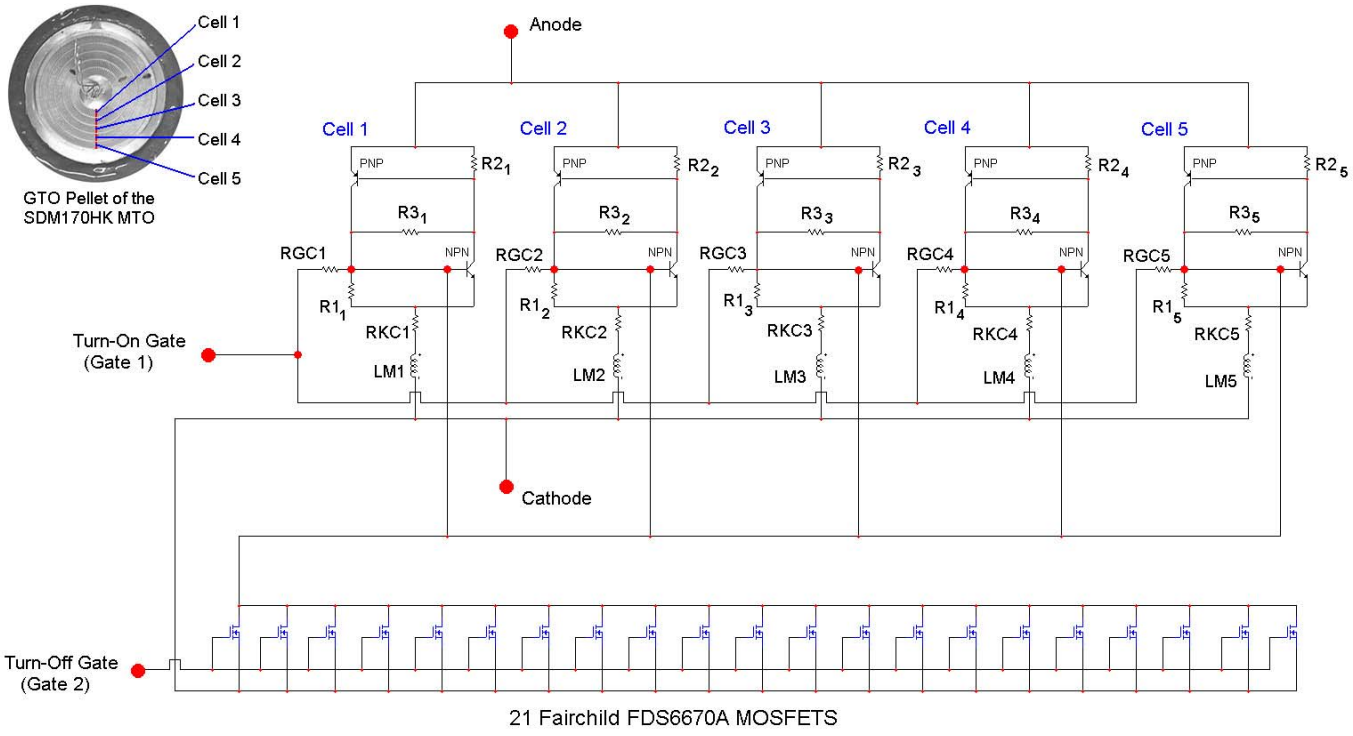


Figure 7. Complete model of the SDM170HK MTO by Silicon Power Corporation.

CIRCUIT MODEL VALIDATION

The SPICE model developed for the SDM170HK MTO was validated by comparing computer-generated DC characteristics to those obtained by experiment.

Figure 8 shows conceptual static I-V characteristics for a GTO. The static I-V characteristics in Fig. 8 give the anode current I_A of a GTO as a function of the anode to cathode voltage V_{AK} for different turn-on gate current values, I_G. The values of interest in Fig. 8 are the forward breakover voltage V_{bo} and the minimum anode current, or holding current, I_h. From Fig. 8 it can be seen that the breakover voltage V_{bo} decreases with increasing I_G.

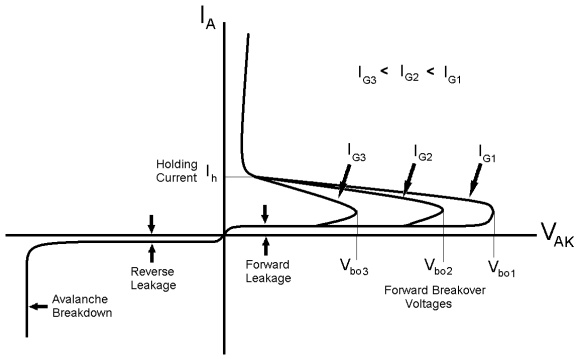


Figure 8. Conceptual static I-V characteristics of a gate turn-off thyristor.

The static I-V characteristic for the SDM170HK MTO was obtained by making direct measurements on the GTO pellet after removing it from the MTO package. Table 1 shows approximate values for I_h based on measurements obtained separately for each of the concentric rings of fingers under different gate currents I_G. The innermost ring of the GTO pellet is designated as "Ring 1," and the rings are numbered successively to the outermost ring, designated as "Ring 5." The gate current I_G in Table 1 should be understood as the current sourced to the gate of the GTO pellet (the turn-on gate of the MTO).

TABLE 1
Summary of Approximate Holding Current Values for the SDM170HK

	Ring 1	Ring 2	Ring 3	Ring 4	Ring 5
I_G (mA)	45	80	150	130	110
I_h (A)	4.2	7	9.4	11	13.8

A static I-V characteristic for the MTO was generated using the SPICE-compatible Micro-Cap 7 circuit simulator [13]. Figure 9 shows a calculated forward-bias characteristic obtained using the circuit model in Fig. 7 for $I_G = 0$. Based on the approximate values for I_h in Table 1 and using a forward breakover voltage V_{bo} = 4500V for $I_G = 0$, the values for R1, R2, and R3 for each of the cells in Fig. 7 were obtained. The values are given in Table A.3 in the Appendix. Note that instead of choosing the same value for R2 for all five cells as in [10], each cell was given a unique value for R2, thereby being more representative of the MTO.

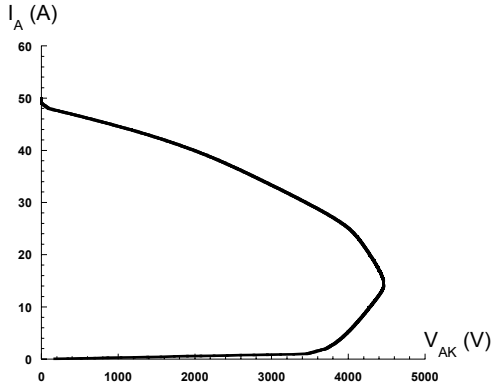


Figure 9. Generated static I-V characteristic for the SDM170HK using the Micro-Cap 7.0 circuit simulator.

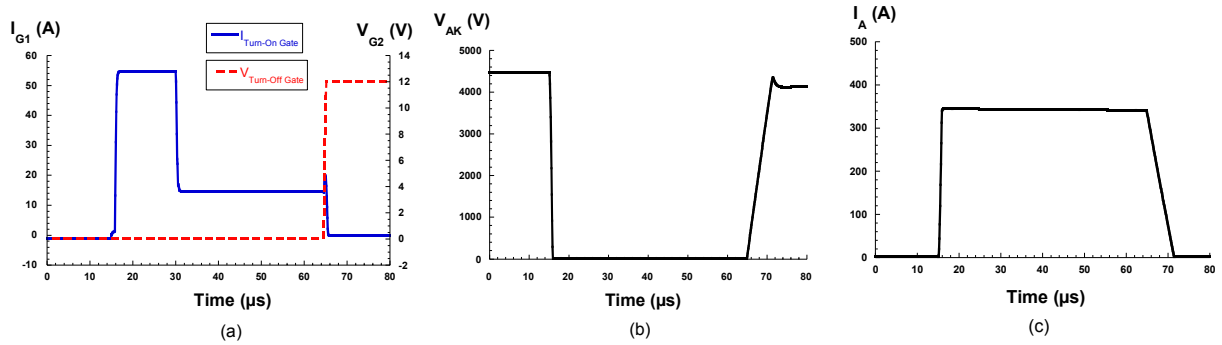


Figure 10. Dynamic switching waveforms generated by Micro-Cap 7.0 for the SDM170HK MTO. (a) The generated turn-on gate current and turn-off gate voltage waveforms. (b) The resulting anode-to-cathode voltage and (c) anode current waveforms using the gate input waveforms shown in (a).

The switching test waveforms generated by Micro-Cap for the SDM170HK using the circuit model in Fig. 7 are shown in Fig. 10. The test circuit used for the switching simulation is shown in Fig. 11.

Fig. 10a shows the turn-on gate current and the turn-off gate voltage waveforms. The rapid turn-on of the MTO is achieved by applying a large initial current pulse to the turn-on gate (gate 1). The large initial pulse can then be reduced to its "back-porch" value, no smaller than 15 A for the SDM170HK. The MTO remains in its conduction state for as long as the "back-porch" current is maintained.

Turn-off is initiated by reducing the turn-on gate current and applying a voltage to the turn-off gate (gate 2). The power MOSFETs switch to their low-resistance "on" state, thereby turning off the MTO. Figures 10b and 10c show the anode-to-cathode voltage and the anode current that result from the input waveforms shown in Fig. 10a, respectively. Typical dynamic switching waveforms of this type for a GTO can be found in [14].

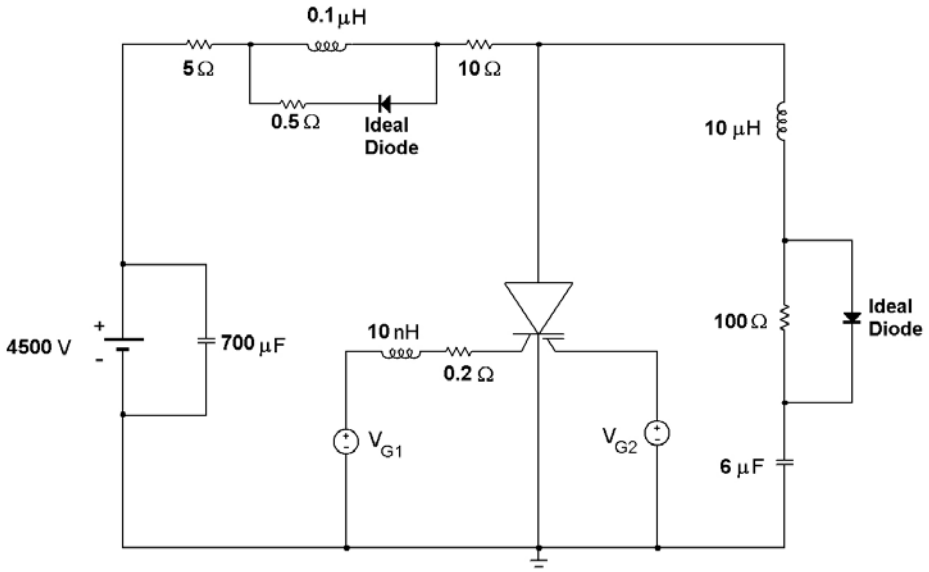


Figure 11. Test circuit used in Micro-Cap 7.0 for obtaining the dynamic switching waveforms for the functional circuit model of the SDM170HK MTO. The diodes in the circuit are Micro-Cap generic diodes with infinite breakdown voltage (ideal diodes).

ELECTROSTATIC FIELD MODELING

To help predict field stresses that may lead to device failure in the SDM170HK, an electrostatic field analysis using an approximate model of the SDM170HK was performed using the Ansoft Maxwell 3D field simulator. The field analysis accurately predicted the location of arc marks found on the inner surface of the ceramic insulator near the internal gate connections of a failed device. The arc track marks that were found on the failed MTO device are shown in Fig. 12.

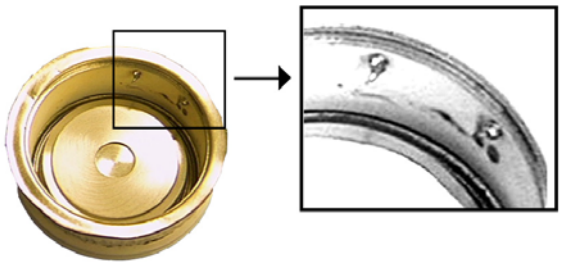


Figure 12. Arc track marks on failed device.

The Ansoft Maxwell 3D field simulator solves for the electric fields in the user-defined problem using finite element analysis of a software-generated tetrahedra mesh [15]. Included in the software is a graphical interface that allows the user to define geometries within a field solution boundary. The user then assigns material properties to the defined solid objects, including dielectric constants and electrical conductivities. Once the geometry of the problem has been created, the user may define the boundary conditions of the problem by assigning voltages to selected geometries. The electric field strength is then solved for everywhere in the problem region.

To create the geometries used in the field simulator for the approximate model of the SDM170HK, precise dimensional measurements were taken of each of the internal and external device components. Using these measurements, the solid models of the device components were each drawn separately in the solid modeler module of the field simulator. They were then assembled into one problem region to produce a complete solid model.

The problem was solved in multiple trials, beginning with simplified geometries and adding complexity with each new trial. In every trial the approximate dielectric constants and conductivities were assigned to each object in the model. The boundary conditions for the problem were defined by applying 4500 V anode-to-cathode and by setting both the gate turn-on and the gate turn-off terminals in the model to 0 V.

In all of the trials, electrostatic fields exceeding the nominal air breakdown threshold of 30 kV/cm were seen surrounding the simulated turn-off gate wire, the turn-off gate ring contact, and the cathode ring contact (or cathode plate).

The results given here are based on the final model used in the field simulator. All of the solid model objects that were used to create the final approximate model of the SDM170HK MTO in the Maxwell 3D field simulator are shown in the Appendix.

After the electrostatic fields had been solved in the final model, the simulator post-processor was used to calculate average and peak field magnitudes surrounding the simulated turn-off gate

wire, the turn-off gate ring contact, and the cathode ring contact.

Figure 13 contains photographs of these three components. Their corresponding solid models for field modeling are shown in the Appendix. The turn-off gate wire connects the gates of the power MOSFETs, and is only partially insulated. The cathode ring contact (or cathode plate) connects the MTO cathode to the cathode fingers of the GTO pellet through a cylindrical resistive element. The source terminals of the power MOSFETs are connected to this ring (or plate), providing the configuration depicted in Fig. 4. The turn-off gate ring contact is used to connect the drain terminals of the power MOSFETs to the gate of the GTO pellet.

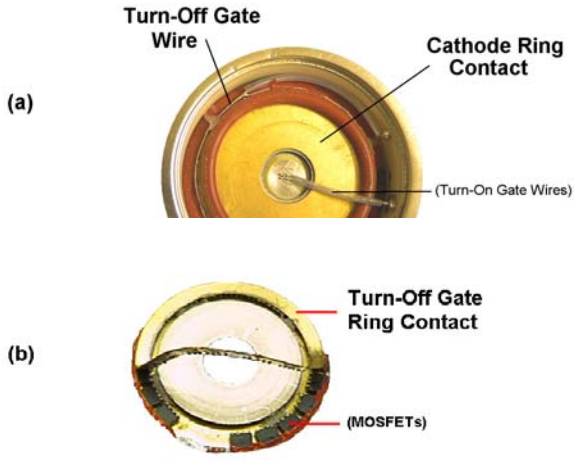


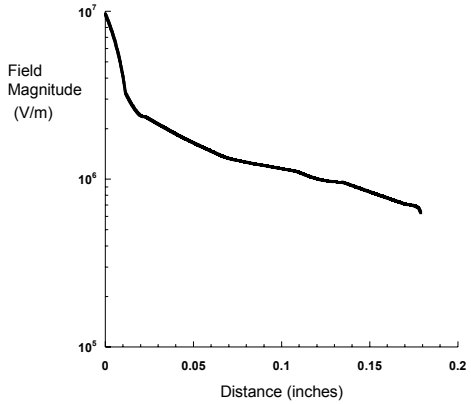
Figure 13. (a) Photograph of turn-off gate wire and cathode ring contact. (b) Photograph of the turn-off gate ring contact, used to connect the drain terminals of the power MOSFETs to the gate of the GTO pellet. The turn-off gate ring contact is pried up, revealing the MOSFETs underneath. Two of the MOSFETs have been removed.

The average and maximum electric field strengths along paths extending radially from each of these three objects to the inner surface of the ceramic insulator were calculated. The paths were placed near the internal MTO gate connections, where the arc track marks were found on a failed device.

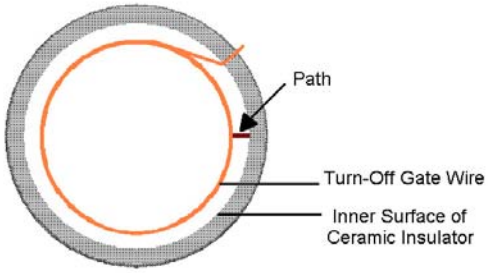
Figure 14a shows a plot of the electric field magnitude calculated along a path extending from the turn-off gate wire to the inner surface of the ceramic insulator. The path used in the approximate model is shown in Fig. 14b. The maximum electric field strength was found to be 9.65×10^6 V/m (96.5 kV/cm). The average field was 1.65×10^6 V/m (16.5 kV/cm).

Figure 15 shows the electric field magnitude calculated along a path extending radially from the simulated cathode ring contact. The maximum electric field strength was calculated to be 3.94×10^6 V/m (39.4 kV/cm). The average field magnitude was 1.07×10^6 V/m (10.7 kV/cm).

The electric field strength calculated along a path extending radially from the simulated turn-off gate ring contact to the inner surface of the ceramic insulator is shown in Fig. 16. It should be noted that part of the path lies within the insulation that surrounds the GTO pellet (see Fig. A.3 in the Appendix). The step seen in the plot shown in Fig 16a is due to the change in the dielectric constant at the interface of the insulation and the air. The maximum electric field strength along the path was 2.11×10^7 V/m (211 kV/cm). The average field magnitude was 1.78×10^6 V/m (17.8 kV/cm).

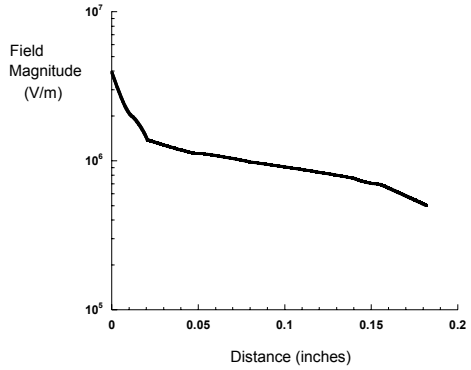


(a)



(b)

Figure 14. (a) Plot of the electric field magnitude along a path extending radially from the turn-off gate wire to the inner surface of the ceramic insulator. (b) Top view of the field simulator model, showing only the turn-off gate wire and the ceramic insulator. The path used to calculate the field is indicated in the figure.



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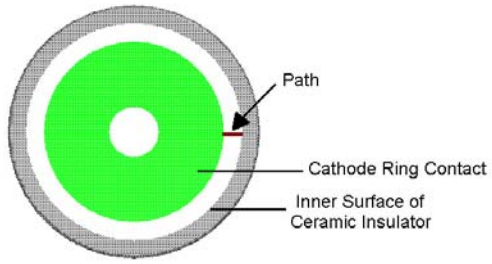
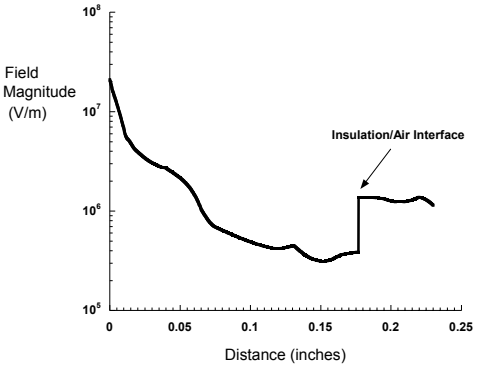
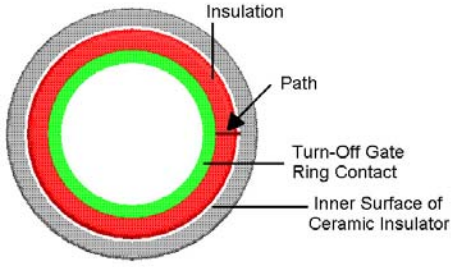


(b)

Figure 15. (a) Plot of the electric field magnitude along a path extending radially from the cathode ring contact to the inner surface of the ceramic insulator. (b) Top view of the field simulator model, showing only the cathode ring contact and the ceramic insulator. The path used to calculate the field is indicated in the figure.



(a)



(b)

Figure 16. (a) Plot of the electric field magnitude along a path extending radially from the turn-off gate ring contact to the inner surface of the ceramic insulator. Part of the path lies within the insulation surrounding the GTO pellet. (b) Top view of the field simulator model, showing only the turn-off gate ring contact, the GTO pellet insulation, and the ceramic insulator. The path used to calculate the field is indicated in the figure.

Two other calculations were made in the approximate model in addition to those already discussed. The magnitude of the electric field along a path extending from cathode to anode along the inner surface of the ceramic insulator was calculated from the model. A plot of the field magnitude along this path is shown in Fig. 17. From the figure it can be seen that the peak electric field magnitude is about 0.4 inches from the cathode end of the ceramic insulator. The arc track marks that were seen on the failed SDM170HK MTO device were also measured to be at this position, as seen in Fig 18.

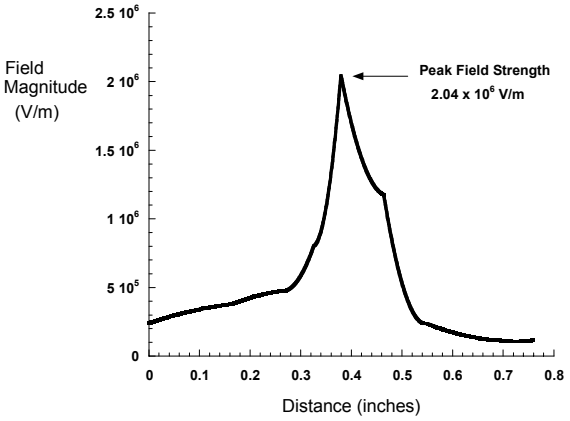


Figure 17. Plot of the magnitude of the electric field along a path extending cathode-to-anode along the inner surface of the ceramic insulator.

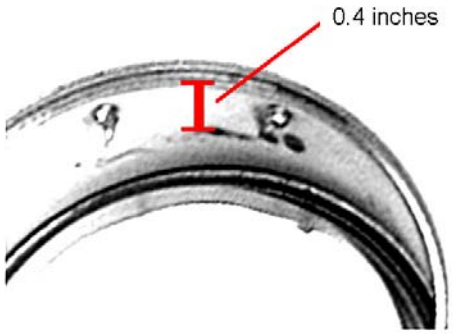


Figure 18. Contrast-enhanced photograph of arc track marks found on a failed SDM170HK MTO device, measured to be 0.4 inches from the cathode end of the ceramic insulator.

The final region that was considered in the electrostatic field analysis was the small region between the anode of the GTO pellet and the inner surface of the ceramic insulator. The radius of the GTO pellet is only slightly smaller than the inner radius of the ceramic insulator, allowing the pellet to fit securely inside. In the approximate model used for the SDM170HK, the radius of the GTO pellet was defined to be only 16.75 mils (.425 mm) smaller than the inner radius of the ceramic insulator.

The electric field magnitude along a path extending radially from the GTO pellet to the ceramic insulator is shown in Fig. 19. As seen in the figure, the magnitude of the field approaches the nominal air breakdown threshold of 30 kV/cm. The maximum field magnitude along this path was 2.36×10^6 V/m (23.6 kV/cm). The average field strength was calculated to be 2.23×10^6 V/m (22.3 kV/cm).

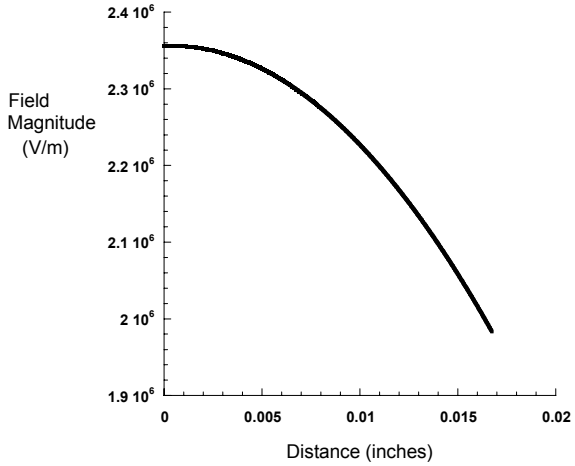


Figure 19. Plot of the magnitude of the electric field along a path extending radially from the anode of the GTO pellet to the inner surface of the ceramic insulator.

CONCLUSION

A SPICE model is presented for the SDM170HK MOS turn-off thyristor (MTO) fabricated by Silicon Power Corporation. The model is based on the two-transistor and three-resistor (2T-3R) cell that allows for S-type negative differential resistance. The ability of the model to simulate the static DC characteristics and the dynamic switching waveforms of the MTO are adequate for initial use in design applications.

An electrostatic field analysis using the Ansoft Maxwell 3D field simulator was also performed for the MTO. Electric field magnitudes exceeding the nominal air breakdown threshold of 30 kV/cm were seen surrounding the turn-off gate wire, the turn-off gate ring contact, and the cathode ring contact. The high-field areas are a concern, as arc track marks have been found on the inner surface of the ceramic insulator near the gate wire feedthroughs of a failed device.

The present study was completed to help baseline an emerging power switch technology. Previously, SPICE-equivalent software packages did not include sub-circuit models for the MOS turn-off thyristor. A versatile, software-importable model of the MTO is now provided to assist the application circuit designer.

The electrostatic field analysis was performed to help identify field stresses in the MTO that could lead to device failure, and to advance efforts aimed at increasing its operating parameters.

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APPENDIX

Note: The photographs and model geometries given here are not to scale and are given only as a reference to illustrate how the Maxwell 3D field simulator model was constructed.

Figure A.1. (a) Photograph of cathode component of the SDM170HK MTO fabricated by Silicon Power Corporation. (b) Top and side views of the model representation of the cathode in the Ansoft Maxwell 3D field simulator.

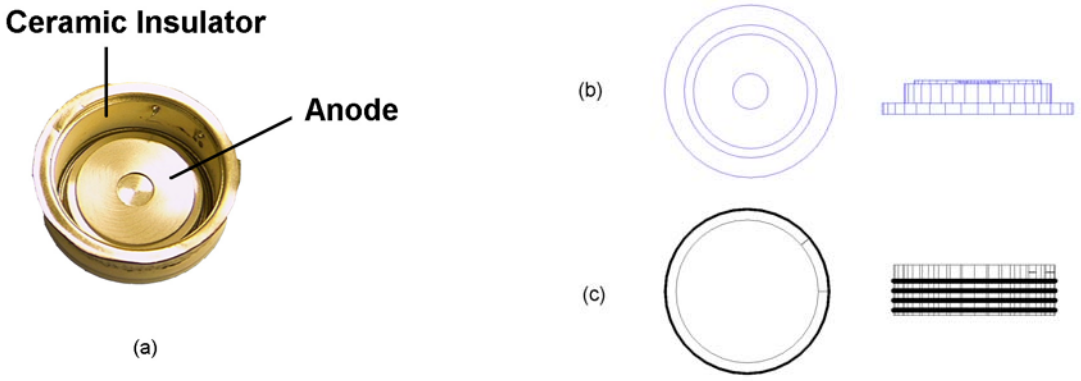

Figure A.2. (a) Photograph of anode and ceramic insulator components of the SDM170HK. (b) Top and side views of the model representation of the anode. (c) Top and side views of the model representation of the ceramic insulator.

Figure A.3. (a) Photograph of the GTO pellet of the SDM170HK. (b) Top and side views of the model representation of the GTO pellet, constructed from a set of objects representing the parts in (a).

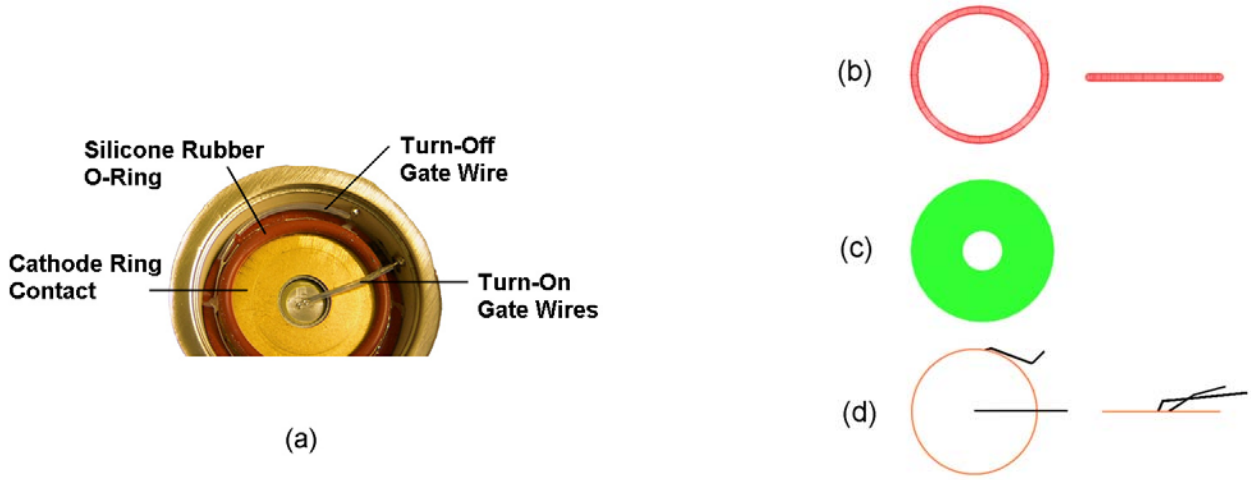

Figure A.4. (a) Photograph of the SDM170HK with the cathode removed, showing the cathode ring contact (or cathode plate), the silicone rubber O-ring, and the gate wires. (b) Top and side views of the model representation of the silicone rubber O-ring. (c) Top view of the model representation of the cathode ring contact. (d) Model representation of the gate wires. The turn-off gate wire is enters through the ceramic insulator and wraps around the ring of power MOSFETs. It is only partially insulated. The turn-on gate wires enter through the ceramic insulator and connect to the gate of the GTO pellet. The wire insulation was included in the model on all gate wires.

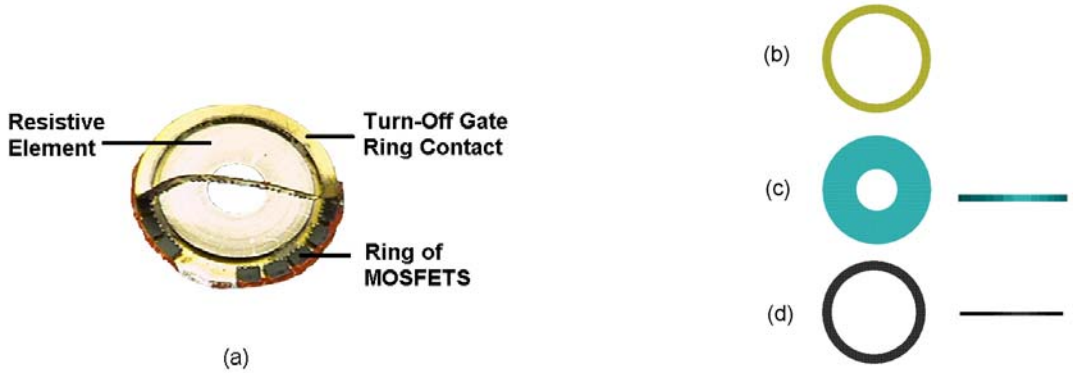

Figure A.5. (a) Photograph of the resistive element (resistor), the turn-off gate ring contact, and the ring of 21 Fairchild FDS6670A PowerTrench® MOSFETs. (b) Top view of the turn-off gate ring contact. (c) Top and side views of the model representation of the resistor. (d) Top and side view of the model representation of the ring of power MOSFETs. The ring of 21 discrete power MOSFETs was approximated by a solid ring of plastic casing with a ring of silicon inside. While this appears to be a crude approximation, it is sufficient for the electrostatic field analysis and allows the Maxwell 3D field simulator to converge more easily.

Figure A.6. (a) Photograph of SDM170HK MTO with the cathode removed. (b) Model representation of the SDM170HK MTO with the cathode removed.

TABLE A.1
Electrical Specifications for the Silicon Power Corporation SDM170HK MTO
Operating Temperature 115 °C

Specification Sheet, Silicon Power Corporation, "SDM170HK2 500A, 4500V, 53mm MTO Thyristor," found at http://www.siliconpower.com/pdf/sdm170v2.pdf, 15 May 2001.

Peak Off State Voltage	**4500 V**
Peak Reverse Voltage	**4500 V**
Peak Controllable Cathode Current	**500 A**
Peak Turn-Off Gate to Cathode Voltage	**20 V**
Peak Continuous Turn-Off Gate to Cathode Voltage	**15 V**
Turn-On Gate Trigger Current	**50 – 100 A**
Minimum Turn-On Gate "Back Porch" Current (Sustain On)	**15 A**
Holding Current	**40 A**
Maximum Off-State Forward and Reverse Leakage Current (V_{AK} = +/- 4500V, $V_{Turn\text{-}Off\ Gate}$ = +15V)	**75 mA**
On-State Voltage	**5.2 V**
Minimum Off Time	**100 μs**
Current Turn-On Delay Time (I_K = 350 A, V_{AK} = 2000 V)	**1.4 μs**
Current Turn-Off Delay Time (I_K = 350 A, V_{AK} = 2000 V, $V_{Turn\text{-}Off\ Gate}$ = +15 V)	**1.2 μs**
Current Rise Time (I_K = 350 A, V_{AK} = 2000 V)	**3 μs**
Current Fall Time (I_K = 350 A, V_{AK} = 2000 V, $V_{Turn\text{-}Off\ Gate}$ = +15 V)	**1.5 μs**

TABLE A.2
Dimensional Measurements Taken of the GTO Pellet Cathode Fingers
of Silicon Power Corporation SDM170HK MTO

	Ring 1	Ring 2	Ring 3	Ring 4	Ring 5
OD – inches	**0.575**	**0.845**	**0.949**	**1.138**	**1.314**
OD – cm	**1.461**	**2.146**	**2.410**	**2.891**	**3.338**
ID – inches	**0.412**	**0.606**	**0.876**	**1.030**	**1.172**
ID – cm	**1.046**	**1.539**	**2.225**	**2.616**	**2.977**
Area – in^2	**0.126**	**0.272**	**0.105**	**0.184**	**0.277**
Area – cm^2	**0.815**	**1.757**	**0.675**	**1.186**	**1.789**
Circumference – inches	**3.101**	**4.558**	**5.733**	**6.81**	**7.810**
Circumference – cm	**7.876**	**11.578**	**14.563**	**17.3**	**19.837**
Approx. number of fingers	**155**	**274**	**344**	**409**	**469**

TABLE A.3
Values of R1, R2, and R3 for Each
2T-3R Cell of the SDM170HK Circuit Model in Fig. 7

	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5
R1	4.7 Ω	4.7 Ω	4.7 Ω	4.7 Ω	4.7 Ω
R2	0.3 Ω	0.17 Ω	0.11 Ω	0.1 Ω	0.08 Ω
R3	17.8 kΩ	17.8 kΩ	17.8 kΩ	17.8 kΩ	17.8 kΩ