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Cavity Light-Emitting Diode for Durable, High-Brightness and High-Efficiency Lighting Applications: First Budget Period Technical Report

Project DE-FC26-06NT42936

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DISCLAIMER

PROJECT SUMMARY

Project Title: Cavity Light-Emitting Diode for Durable, High-Brightness and High-Efficiency Lighting Applications

Project Number: DE-FC26-06NT42936

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Other Team Members: None

Technology Focus: Product

Relevant Subtask Priority Areas:
4.1.2/4.2.2: Practical implementation of materials and device architectures
4.1.3: Improved contact materials and surface modification techniques to improve charge injection

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EXECUTIVE SUMMARY

The objective of this research project was to produce highly efficient white organic light-emitting diode (OLED) devices using a novel device structure called the Cavity Organic Light-Emitting Diode (COLED), which is anticipated to lead to a path for achieving DOE lighting goals of 100 LPW efficacy and 50,000 hours' lifetime at 850 cd/m^2. The product development plan included a two-phase effort to be completed within 36 months. By the end of the two-phase project, the COLED technology was expected to be ready for commercialization of low-cost, white-light-emitting COLED devices with high efficiency and long lifetime.

Achievement of this ambitious goal required upgrading and optimizing the COLED device structure and its fabrication process from its current status. In the past 12 months we have performed the five tasks laid out in the project management plan to improve the COLED device performance by upgrading its components. Below we summarize the progress achieved during the first year of the development effort and the status of all milestones before the project was abruptly stopped.

1. **Reduce dielectric layer thickness and improve its strength**

We optimized the existing process and conceived a novel process to increase the breakdown voltage of the dielectric layer and yield of the COLED device (a new invention, patent application is being filed). *We have exceeded Milestones 1 and 2.* We have achieved 80% yield with 120nm dielectric thickness (Milestone 1 = 50% yield, 125nm) in the first months and 91% yield with 118nm dielectric thickness (Milestone 2 = 90% yield, 125nm).

2. **Develop and evaluate air-stable cathodes with low work function**

We have met Milestones 5 and 6 by successfully demonstrating (a) a stable alloy cathode and (b) a Cu/C60 cathode useful for COLED structures. In addition, we have made significant progress in developing an organic cathode.

3. **Optimize cavity structure**

   3.1 Theoretical calculations: We performed calculations for optical simulation to assess the correlation between light extraction efficiency and the cavity dimension. We also performed theoretical calculations of the electric field distribution and the effective device area as a function of cavity diameter and spacing between the cavities. We then analyzed the possible quantum mechanical effect of the light-emitting polymer molecules filled into the cavity and determined the optimal cavity dimension based on these theoretical calculations and analyses. *We have therefore achieved Milestone 9*.

   3.2 Reduction of cavity dimension: We achieved cavity diameter of ~0.6 μm and spacing of 1.0 μm. *We have exceeded Milestone 10a, which specified both cavity diameter and spacing of 1.0 μm.*

   3.3 Alternative top electrode metal: Although this task was scheduled to be performed only during Year 2, we integrated some of this work in Year 1 with Task 1. We believe that the proper integration of some of these tasks may allow us to work more effectively, which will reduce the overall cost of the project. In this task we have established that tungsten can be used as an alternative to the original Pt top electrode.

4. **Optimize anode and cathode interfaces**

We developed fundamental aspects of cathode / polymer interface, anode / polymer interface, and hole and electron injection / transportation properties of the light emitting polymer (LEP)

in a COLED structure. We have made significant progress in understanding the operating mechanism of the COLED devices.

5. Device characterization

We evaluated various COLED devices by determining their current-voltage-brightness (IVB) characteristics, the breakdown voltage, and the leakage current of the dielectric layer. We have achieved an external quantum efficiency (EQE) of 0.2%, *exceeding the target of 0.1%*. Since the Department of Energy has terminated this project and declined our request for a no-cost extension of the project, we did not have enough time to produce COLED devices using the smaller cavity design. Consequently, some specifications of Milestone 12a have not yet been demonstrated.

The following milestones were set at the beginning of the project after a series of discussions between SRI and Department of Energy personnel:

Phase I (24 months)

Task 1: Reduce Dielectric Layer Thickness

Milestone 1. Dielectric thickness = 125 nm, yield = 50% in month 6

Milestone 2. Dielectric thickness = 125 nm, yield = 90% in month 12

Milestone 3. Dielectric thickness = 100 nm, yield = 70% in month 18

Milestone 4. Dielectric thickness = 100 nm, yield = 90% in month 24

Task 2. Synthesize Air-Stable Cathode

Milestone 5. Evaluation of Mg-Al and Li-Al alloy cathodes completed in month 6

Milestone 6. Evaluation of TiN and C60/Cu cathodes completed in month 12

Milestone 7. Evaluation of organic cathode completed in month 18

Milestone 8. Low-work-function cathode selected in month 24

Task 3. Increase Active Device Area

Milestone 9. Theoretical calculation in cavity dimension completed in month 5

Milestone 10a. Cavity diameter and spacing reduced to 1.0 μm in month 9.

Milestone 10b. Cavity diameter and spacing reduced to 0.3 μm in month 17.

Task 4. Select/Synthesize Interface Material

Milestone 11. An ideal interfacial material identified or synthesized in month 24

Task 5. Produce and Characterize COLED Devices

Milestone 12a. QE ≥ 0.1%; apparent brightness ≥ 500cd/m2, local brightness ≥ 50kcd/m^2 in month 12

Milestone 12b. QE ≥ 1% or 3X higher than a traditional OLED in month 15.

Milestone 13. Brightness ≥ 1000 cd/m^2, voltage ≤ 5V @ 100 cd/m^2, QE > 1% or five times higher than a traditional OLED, efficacy ≥ 30 LPW in month 24.

Phase II (12 months)

Task 6. Fabricate Large COLED (0.577"×0.577" or 1"×1")

Milestone 14. Yield of large COLED devices ≥ 90% in month 30.

Task 7. Produce / Optimize White COLED

Milestone 15. White COLED with CIEx,y = 0.310±0.016, efficacy > 25 LPW in month 27.

Milestone 16. Efficacy improved to > 50 LPW in month 30.

Milestone 17. Efficacy = 100 LPW, Lifetime = 10,000 hours in month 36.

Table 1 summarizes the tasks specified in the management plan and performed in the first year, together with the corresponding achievements. A more detailed description of the individual tasks is given in the next section.

Table 1. Summary of Current Project Status

Tasks	Original Milestone definition		Final Status
1. Dielectric layer	M1	Thickness = 125 nm; Yield ≥50%	Exceeded (120 nm, 80%)
	M2	Thickness = 125 nm; Yield ≥90%	Exceeded (118 nm, 91%)
2. Cathodes	M5	Evaluate Al-alloy cathodes	Met
	M6	Evaluate TiN & Cu/C60 as cathodes	Met
	M7	Significant progress made (scheduled to complete in month 18)	
3.1 Optical simulation	M9	Theoretical calculation to suggest optimal cavity dimensions	Met
3.2 Cavity dimension	M10a	Cavity diameter / spacing = 1.0μm / 1.0μm	Exceeded (0.6 μm/1.0 μm)
3.3 Alternative top electrode metal	No specific milestones. Task scheduled for 2nd year, but started 1st year		
4. Interfaces	No specific milestones. Significant progress made.		
5. Device characterization	M12a	EQE ≥ 0.1%; Voltage ≤ 10 V @100 cd/m^2; Brightness ≥ 500 cd/m^2; Local brightness ≥ 50,000 cd/m^2	EQE = 0.20% Not completed and demonstrated due to project termination

The development work during Year 1 of the project followed the original Statement of Work (SOW) approved by the Department of Energy program manager. The agreement required the introduction within the first year of a manufacturing partner that was acceptable to the Department of Energy. SRI succeeded in securing an agreement with a Japanese company with global and U.S. manufacturing facilities. However, the Department of Energy found this option inadequate and terminated the project.

INTRODUCTION

A COLED device consists of a top electrode (anode) and a bottom electrode (cathode) separated by a thin dielectric layer. In this metal/dielectric stack, numerous small wells, or cavities, are etched through the top electrode and the dielectric layer. These cavities are subsequently filled with LEP molecules. When a voltage is applied between the top and bottom electrodes, holes (from the top electrode) and electrons (from the bottom electrode) are injected into the polymer. Light emission is generated upon recombination of holes and electrons within the polymer along the perimeters of cavities.[1] Figure 1 compares the structures of the COLED and the traditional OLED. The existing COLED fabrication process flow is illustrated in Figure 2.

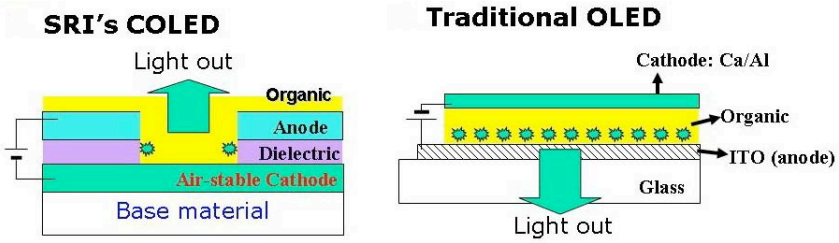

Figure 1. A comparison of SRI's COLED vs. traditional OLED

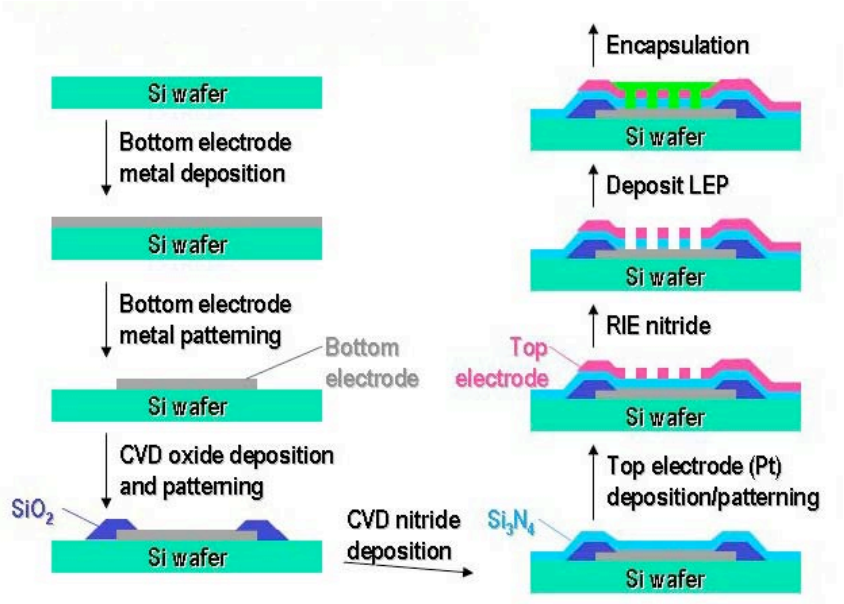

Figure 2. Existing COLED fabrication process flow chart

[1]. Qibing Pei, Cavity-emission Electroluminescent Device and Method for Forming the Device, U.S. Patent 6,593,687 B1, July 15, 2003

A COLED can potentially be 5 times more efficient and can operate at as much as 100 times higher current density with much longer lifetime than an OLED. To fully realize these potential advantages, the COLED technology must overcome the following technical barriers, which were the technical focused points for Years 1 and 2 (Phase I) of this project:

1. **Construct optimum thickness dielectric layer:** In the traditional OLED structure, the optimal thickness of the LEP film is approximately 80-100 nm. In a COLED device, the effective LEP thickness roughly equals the thickness of the dielectric layer. Therefore, the optimal dielectric thickness for a COLED should also be roughly equal to 80-100 nm. Generally speaking, it is technically challenging to produce a defect-free dielectric layer at this thickness with high uniformity, especially over a large area.

2. **Develop low-work-function cathode:** A desired cathode should have a low work function that matches the lowest unoccupied molecular orbital (LUMO) level of the LEP molecules. This is usually achieved by using a low-work-function metal such as calcium, barium, lithium, or magnesium as the cathode. However, these metals are very vulnerable to oxygen and water. Since the cathode of the COLED will be exposed to air and processing chemicals during the COLED fabrication process, these low-work-function metals cannot be used directly in the COLED structure. Thus, new materials with low work function and better chemical stability are needed for the COLED cathode.

3. **Increase active device area:** Since photons are only generated from perimeters of the cavities, the actual active area in a COLED device is smaller than the device surface area. The cavity diameter and cavity spacing of the COLED devices previously produced at SRI by conventional photolithography processing are typically in the range of 3 to 7 μm with an estimated active area of 2-3%. To achieve the same brightness of a traditional OLED at the same applied voltage, the active device area of a COLED should be at least 20% (1/5) of the device surface area, provided the COLED has 5 times higher EQE. This requires reducing the cavity diameter and cavity spacing to the sub-micrometer region (see below for more detailed discussion), which can be achieved by electron-beam lithography or nanoimprint lithography.

4. **Improve metal/polymer interfaces:** The polymer/metal interfaces are critical issues to improve and optimize since they directly affect the effectiveness and balance of hole and electron injection, and consequently the device performance. Conventional approaches for improving a metal/polymer interface include deposition of a special interfacial material on the selected electrode surface or applying a proper surface treatment prior to deposition of the LEP. Since these approaches are generally nonselective to the cathode and anode, they cannot be directly adopted for COLED devices. Generally, the interface integration in current OLED technology still needs a better chemical approach. Hence, advanced methodology developed for the COLED technology as promoted in this project may be also suitable for other OLED devices.

To address the above technical deficiencies, SRI and the Department of Energy defined the following tasks to be performed in Phase I:

Task 1. Reduce dielectric layer to 125 nm (Year 1) and 100 nm (Year 2)

1.1 Optimize surface pretreatment process

1.2 Optimize plasma enhanced chemical vapor deposition (PECVD) parameters

1.3 Optimize multi-layer deposition approach

1.4 Test alternative dielectric materials

1.5 Further optimize selected recipe (Year 2)

Task 2. Develop air-stable cathode

2.1 Continue optimizing Mg-Al and Li-Al cathodes

2.2 Study TiN cathode

2.3 Study Cu/C60 cathode

2.4 Optimize organic cathode

2.5 Select cathode/perform further optimization (Year 2)

Task 3. Optimize cavity structure

3.1 Perform optical simulation on cavity diameter

3.2 Reduce cavity diameter and spacing to ~1.0 μm (Year 1) and 0.3 μm (Year 2)

3.3 Select top electrode material (Year 2)

3.4 Optimize top electrode thickness (Year 2)

Task 4. Optimize interfaces

4.1 Optimize anode interface

4.2 Optimize cathode interface

Task 5. Characterize device

5.1 Determine device electrical and optical characteristics.

These tasks are discussed in detail in the next section.

DETAILED TECHNICAL ACHIEVEMENTS FOR INDIVIDUAL TASKS

TASK 1. REDUCE DIELECTRIC LAYER THICKNESS

Task 1.1-1.3 Optimize Dielectric Layer

Some of the most commonly used dielectric materials in the semiconductor industry include silicon nitride (Si_3N_4), silicon oxide, and metal oxides. Since oxides can form hydroxyl groups that may potentially reduce the efficiency of the COLED devices,[2] we selected Si_3N_4 as the dielectric material of our prototype COLED devices. Generally speaking, the best quality Si_3N_4 films are obtained by low-pressure chemical vapor deposition (LPCVD). However, this process requires high temperature (~700ºC), which is not suitable for the COLED using an aluminum cathode layer. We therefore selected plasma-enhanced chemical vapor deposition (PECVD), which can be performed at lower temperature (~300ºC).

One of the technical challenges for constructing a uniform Si_3N_4 thin film on top of an Al thin film using the PECVD process is the formation of Al hillocks during the PECVD process. The hillock phenomenon is a result of the differences in thermal expansion coefficients between the Al and the Si_3N_4 layers and manifested by thermal cycling stresses. The hillock tips can easily penetrate the dielectric layer, causing a short circuit between the top and bottom electrode and resulting in device failure. We have previously used an Al-Cu-Si alloy to reduce the hillock formation and found that pre-baking the Al-Cu-Si thin film at the PECVD processing temperature (300ºC) overnight followed by an oxygen plasma surface pre-treatment before PECVD deposition can significantly improve the breakdown voltage of the resulting dielectric layer. Therefore, optimizing the conditions of pre-baking time and the oxygen plasma treatment parameters such as power, time, and oxygen pressure was important for obtaining the optimal dielectric layer performance (Task 1.1).

We have also found that the performance of the dielectric layer is significantly improved if the Si_3N_4 deposition is performed in two steps (2-layer approach) in comparison to depositing the same thickness by a single deposition process. Thus, it was important to know whether further splitting the deposition, i.e., to a 3-layer or 4-layer approach, would result in further performance enhancement (Task 1.3).

On the other hand, the quality of the Si_3N_4 layer is significantly influenced by the processing parameters used for the deposition. If the parameters are not optimized, the resulting Si_3N_4 film possesses higher content of residual N-H, which reduces the dielectric strength of the film. We analyzed the Si_3N_4 film using FT-IR and the residual N-H was not detectable in the film deposited using our existing procedure parameters (Task 1.2). This indicates that the current recipe is already optimal.

Since the above tasks involve optimization of multiple process parameters, a Design Of Experiment (DOE) software program was selected to design the experimental matrix and to analyze the data in an efficient way. In this approach, an experimental matrix is generated by the

[2] It was reported by several groups that OH groups functioned as electron traps that reduced the efficiency of an OLED.

software based on the boundary conditions inputted by the user. The experimental results are analyzed by the software using the selected mathematical model to obtain the optimal experimental conditions.

In the first set of experiments (DOE-1), we used a 5-factor fractional factorial Resolution-III design with three center points to study the effects of pre-bake time, number of layers of Si_3N_4, and the Al surface pre-treatment parameters (i.e., the O_2 plasma power, time, and oxygen pressure). One wafer is used for each individual experiment. The breakdown voltage of the resulting COLED devices was measured and the yield of devices was calculated based on the percentage of devices having breakdown voltage ≥ 20 V. The results of DOE-1 are presented in Table 2.

Data analysis of DOE-1 results indicates that the yield is higher under the following conditions:

- ✓ Relatively short pre-bake time is used. We selected a pre-bake time = 0-6 h for the second set of experiments (DOE-2).
- ✓ Medium O_2 plasma power. We selected 400 W for DOE-2.
- ✓ Medium O_2 plasma time. We used 17.5±5 min in DOE-2.
- ✓ O_2 pressure in the range of 90-145 Torr. The selected O_2 pressure for the DOE-2 set of experiments was 115±30 Torr.
- ✓ Although the 3-layer and 2-layer are significantly better than the single layer, the 3-layer is only moderately better than the 2-layer. Considering that the extra process step required for the 3-layer approach results in only moderate improvement, we decided to use the 2-layer approach in future experiments.

Table 2. Experimental Design Matrix and Results of DOE-1

Variables	A	B	C	D	E	Response
Wafer I.D.	**Pre-bake time (h)**	**Number of nitride deposition**	**O_2 plasma time (min)**	**O_2 plasma power (W)**	**O_2 pressure (Torr)**	**Yield (%)**
DOE1-1	0	1	5	550	145	62.5
DOE1-2	10	1	5	150	35	59.3
DOE1-3	0	3	5	150	145	85.2
DOE1-4	10	3	5	550	35	21.1
DOE1-5	0	1	30	550	35	60.9
DOE1-6	10	1	30	150	145	16.7
DOE1-7	0	3	30	150	35	34.6
DOE1-8	10	3	30	550	145	63.6
DOE1-9	5	2	17.5	350	90	66.7
DOE1-10	5	2	17.5	350	90	61.9
DOE1-11	5	2	17.5	350	90	75.0

Bottom electrode composition: 3%Mg 97%Al; total thickness of dielectric layer: ~120 nm; pre-bake temperature: 300ºC

In DOE-2, we used a 3-factor fractional factorial Resolution-III design to further investigate the effects of pre-bake time, plasma time, and O_2 pressure. Two wafers were used for each experiment. The results of DOE-2 are summarized in Table 3.

Table 3. Experimental Design Matrix and Results of DOE-2

Variables	A	B	C	Response
Wafer ID	**Pre-bake time (h)**	**O_2 plasma time (min)**	**O_2 pressure (Torr)**	**Yield (%)**
DOE2-1	0	12.5	145	80
DOE2-2	0	22.5	85	2.8
DOE2-3	6	12.5	85	0
DOE2-4	6	22.5	145	37
DOE2-5	3	17.5	115	59

The results of DOE-2 indicated again that a shorter pre-bake time gave a higher yield. This is consistent with the results of DOE-1, but is contrary to our previous experience using Al-Cu-Si alloy. This result revealed a marked difference in certain properties (possibly, annealing or nanostructural rearrangement) between the Mg-Al alloy and the Cu-Al alloy. We therefore decided that the pre-bake process should be eliminated in future work.

Further analysis of DOE-2 data suggested that a short plasma time (12.5 min) and a high O_2 pressure (145 Torr) gave the best results. We therefore selected a plasma time of 12±4 min and O_2 pressure of 145±20 Torr in DOE-3.

In DOE-3, we used a 3-factor full factorial Resolution-III design to further narrow the processing windows for the plasma time, plasma power, and O_2 pressure. The results are summarized in Table 4.

Table 4. Experimental Design Matrix and Results of DOE-3

Variables	A	B	C	Response
Wafer ID	**plsm power (W)**	**plsm-time (min)**	**O_2-pressure (Torr)**	**Yield (%)**
DOE3-1	330	8	125	75.00
DOE3-2	330	8	165	78.95
DOE3-3	330	16	125	37.50
DOE3-4	330	16	165	56.52
DOE3-5	470	8	125	73.91
DOE3-6	470	8	165	73.91
DOE3-7	470	16	125	72.73
DOE3-8	470	16	165	39.13

The results obtained from DOE-3 suggest that the plasma power and O_2 pressure have only minor effects on the yield. In contrast, the plasma time has a significant effect. Experiments using a plasma time of 8 min seem to give the best yield. Therefore, in future experiments, we will repeat the above experiments using a plasma time of 8±3 min.

Task 1.4 Test Alternative Dielectric Materials

The existing COLED fabrication process (Figure 2) consists of several steps of the PECVD process: one PECVD SiO_2 step and two PECVD Si_3N_4 steps. If some of these process steps can be replaced with solution-processible polymer materials, the fabrication cost will be significantly lower. In this regard, the preceramic polymer PHMS-OH invented at SRI has many unique properties, making it a good candidate for this application.

Siloxanes, including polydimethylsiloxane (PDMS) and silsesquioxane polymers and resins are known as excellent low dielectric materials (k<3) as well as excellent water repellants. However, they have wetting and bonding issues due to their low surface tension and high inherited chemical stability. The preceramic polymer (PHMS-OH) is a semilinear siloxane type of polymer containing a significant level of $[CH_3Si(OH)O]$ monomeric units, which make it highly wettable and allow strong chemical bonding to many materials after curing. During curing the Si-OH groups are condensed to Si-O-Si, generating the final deposited material with the same structure as the commercially used methylsilsesquioxanes. The PHMS-OH forms a stable solution in many organic solvents and can be cured at room temperature or elevated temperature. High-quality films can be produced by spin-coating, dip-coating, and spray-coating. The cured film can resist high temperatures and can be patterned via standard photolithography and reactive ion etching (RIE). In addition, the physical properties of the polymer can be adjusted by modification of the chemical structure. It can potentially be used as an alternative for the PECVD SiO_2 and/or the PECVD Si_3N_4 dielectric layers. It can be used in conjunction with sputter- or CVD-deposited dielectric materials to improve performance.

We first experimented using PHMS-OH as the alternative for the Si_3N_4 and the SiO_2 layers, which require a film thickness of <1 μm. During the early attempts to produce PHMS-OH film at this thickness level, we encountered several technical problems, such as high leakage current through the thin film, poor uniformity, and insufficient adhesion to the substrate (Figure 3).

Figure 3. Pictures of PHMS-OH thin film coated on Al-Mg alloy surface before process optimization. Left: PHMS-OH film peeled off substrate due to insufficient adhesion. Right: non-uniform film.

These problems have been solved by the following approaches:

- ✓ Use an adhesion promoter to improve the adhesion.
- ✓ Use a proper solvent to improve the film uniformity.
- ✓ Purify the PHMS-OH to reduce the leakage current.

Currently, we are able to generate quality thin films ≥ 100 nm thick by spin coating. We have also developed a standard photolithography patterning / RIE process for patterning the PHMS-OH thin film. The leakage current has been reduced by two orders of magnitude. The dielectric strength has been enhanced to 110 kV/mm. Although this dielectric strength is still too low if used as the alternative of the Si_3N_4 layer, it is sufficient to be used as the alternative for the PECVD SiO_2 layer (see Figure 2).

We have also experimented a novel process to improve the breakdown voltage and device yield. Some results of these experiments are presented in Table 5, which clearly shows that the new process significant improves the device yield: although wafer DOE3-11 has the thinnest dielectric layer (117.9 nm), it has the highest yield of 91.3%, exceeding our target of 125 nm and 90% yield (Milestone 2).

Table 5. Results of Experiments Using Mixed Materials and Processes

Wafer ID	O_2 plasma conditions			Process	Dielectric thickness	Yield (%)
	Power (W)	Time (min)	Pressure (Torr)			
DOE3-09	400	12	145	old	145.0	60.9
DOE3-10	400	12	145	old	155.0	82.6
DOE3-11	**400**	**12**	**145**	**NEW**	**117.9**	**91.3**
DOE3-12	400	12	145	old	148.0	44.4

We had previously proposed to evaluate aluminum nitride as the dielectric material for the COLED, since it can potentially further improve the heat dissipation efficiency of the COLED. However, after a careful literature study, we decided to abandon this approach for the time being because it requires developing a completely new process for depositing and etching the AlN film, resulting in an extensive developmental effort. Since Si_3N_4 can satisfy the need for the proposed prototype COLED devices, it was decided to save the limited resources for more critical aspects of the development.

TASK 2. DEVELOP AIR-STABLE CATHODE WITH LOW WORK FUNCTION

Prior to this project, in a proof-of-concept COLED device, we used an Al-Si-Cu alloy as the cathode. Since the work function of these metals is relatively high, 4.3 eV for Al and 4.5 eV for Cu, the resulting COLED devices have lower quantum efficiency due to poor electron injection. In order to improve the electron injection from the cathode, a low work-function cathode is needed.

We proposed several possible approaches, including using (1) an alloy containing a low-work-function element such as Li and Mg, (2) a Cu/C60 complex, (3) a TiN thin film, and (4) an organic cathode. We have conducted experiments on all these approaches and have identified three approaches, the Mg-Al alloy, the Cu/C60, and the organic cathode as promising for further development. The detailed experimental results and discussion are presented in the following sections. We have elected to abandon the TiN cathode for further development due to the technical complexity and the fact that the Cu/C60 and the organic cathodes have shown very promising results.

Task 2.1 Optimize Mg-Al and Li-Al cathodes

Since the cathode metal is the first layer deposited on the substrate, the cathode metal layer needs to have sufficient chemical and thermal stabilities to survive all the subsequent processes, such as RIE and PECVD. Therefore, we first examined the thermal stability of the Li-Al and Mg-Al alloys.

We elected to start with alloys containing 3% Li and 3% Mg. We deposited the alloy film on a Si wafer by sputter deposition, and subsequently baked the wafer at 300ºC (the temperature used for the PECVD process) under nitrogen for several to 10 hours. The wafer was then visually inspected.

It was found that on the Li-Al alloy wafer there was a significant surface roughening observable after baking. This can be easily seen by comparing the photographs of Li-Al-coated wafers before and after baking (Figure 4). The sample before baking was very shiny (right picture), but after baking for several hours, the alloy film became milky white (left picture). Significant phase separation between Li and Al can be seen under an optical microscope (insert on top left).

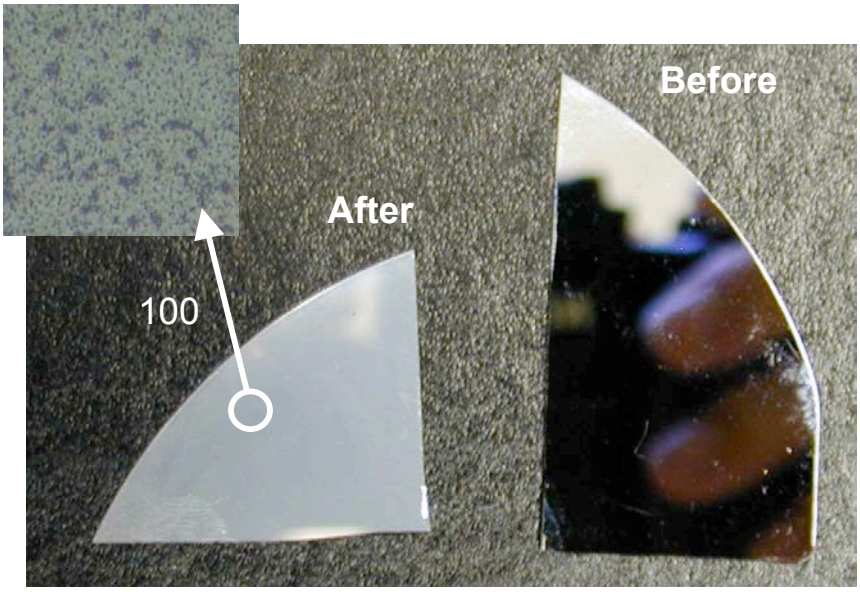

Figure 4. Comparison of Li-Al film before (right) and after (left) baking

Since roughening of the cathode surface will increase the defect density and reduce the uniformity of the dielectric layer deposited in the subsequent PECVD step that will result in device failure, it was decided that the Li-Al alloy is not compatible to the PECVD process. However, if a low temperature dielectric layer processing is matured in the future, such as the solution processible PHMS-OH, we may reconsider this Li-Al alloy approach.

In contrast to the Li-Al alloy, Mg-Al has much better thermal stability. No phase separation or surface roughening is observable after baking the substrate at 300ºC for over 10 hours. The chemical stability of the Mg-Al is also acceptable. Although some standard processing chemicals can result in damage to the Mg-Al film, we have successfully developed alternative processes and found alternative chemicals that will not damage the Mg-Al alloy film. Therefore, we have selected the Mg-Al alloy cathode for further development. All COLED devices discussed in this document use the Mg-Al alloy cathode.

Task 2.2 Study TiN Cathode

Since titanium nitride (TiN) has good electrical conductivity, excellent chemical stability, and adjustable work function, it can potentially be the cathode of a COLED device. In prior research we sputter-deposited a TiN thin film on top of the cathode metal (Al) layer and fabricated COLED devices using the process steps illustrated in Figure 2. It was found that in these COLED devices, the TiN layer was marked damaged by the RIE processes. Therefore, it is necessary either to use a protective layer on top of the TiN (to protect the TiN film from being etched by RIE) or deposit the TiN layer after all the RIE processes.

If the approach of using a protective layer is selected, a series of new processes needs to be developed, such as patterning the individual protective layer, the TiN layer, and the Al layer without damaging the others. On the other hand, since the work function of TiN film varies greatly with the stoichiometry of the film and the process used for the deposition, the evaluation process will involve fabricating COLED devices containing TiN film deposited under various conditions. Since these new processes required a significant development effort, impossible to be accomplished within the budget of this project, we elected the latter approach by trying to deposit the TiN film following the RIE process.

On a standard COLED substrate fabricated using the standard procedure (Figure 2), immediately after the RIE nitride step, we deposited an ultra-thin (5Å, 15Å, 25Å) layer of TiN via the PVD process. We intended to generate a discontinuous TiN film on the COLED substrate to avoid shorting the circuit between the top and bottom electrodes. Unfortunately, even the 5Å TiN film resulted in a short circuit between the top and bottom electrodes, rendering this experiment unsuccessful.

We concluded that it is required to deposit the TiN film before deposition of the dielectric layers (i.e., the SiO_2 and Si_3N_4 layers) and top electrode layer in order to avoid the shorting. As pointed out earlier, this would require developing the processes for patterning the TiN film as well as establishing a reliable process to protect the TiN film from being damaged during subsequent processes, such as the RIE of the SiO_2 and Si_3N_4 layers. In addition, the work function of the TiN film depends greatly on the deposition processing parameters as well as the method of deposition, which requires fabrication and evaluation of many COLED specimens using various deposition techniques and parameters of TiN films. Considering all these

difficulties and the fact that several other cathode candidates have already shown very promising results (see below for more details), we decided that this approach should abandoned.

Task 2.3 Study Cu/C60 Cathode

A Cu-C60 complex has been previously used as the cathode for an organic diode.[3] Since the LUMO of C60 is approximately 3.5 eV, comparable to that of Mg, the Cu/C60 cathode will be good enough for many LEP materials. Besides, the organic nature of C60 may also help to form a better interface between the cathode and the LEP film. Therefore, a C60/Cu cathode is expected to have better overall performance than a Mg-Al alloy cathode.

A similar approach was used for the initial evaluation of the Cu/C60 cathode. Using a regular COLED device consisting of a Mg-Al bottom electrode (150 nm) and a Pt top electrode (150 nm), we thermally evaporated 5Å of Cu, 5Å of C60, and 5Å of Cu in sequence. A light-emitting polymer solution was then spin-coated on the COLED substrate. The IVB characteristics of this COLED were compared to those of a regular COLED without the Cu/C60/Cu depositions (Figure 5).

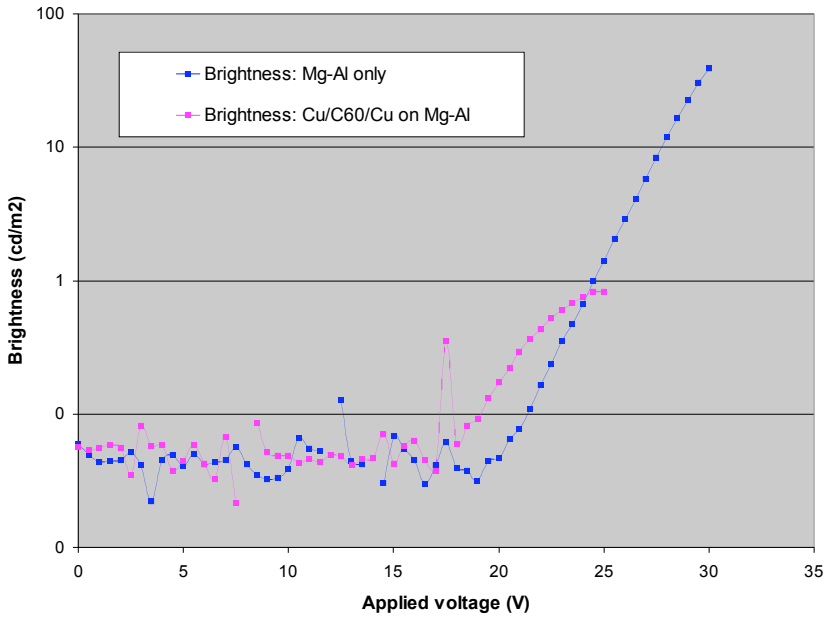

Figure 5. Voltage-brightness (VB) characteristics of a COLED using a Cu/C60 cathode.

Figure 5 clearly demonstrates that the Cu/C60 cathode lowers the device turn-on voltage by approximately 3V, indicating improved electron injection. However, the maximum achievable brightness was reduced, probably due to the fact that the anode (Pt) was also coated by a thin layer of Cu/C60, which reduced the hole injection. Future work will focus on integrating the Cu/C60 cathode process into the COLED fabrication process.

Task 2.4 Optimize Organic Cathode

We have previously demonstrated that an organic molecule can be chemically bonded to a metal electrode surface to serve as a cathode for electron injection. In this project, we reinvestigated the previous approach and invented two novel chemistries of forming an organic cathode with potentially better stability.

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[3]. L. Ma, and Y. Yang, *Appl. Phys. Lett.* **84**, 4786 (2004)

The performance of two novel organic cathodes is promising: the device turn–on voltage is significantly reduced (see Figure 6, compounds #2 and #5). However, we also noticed that the maximum brightness achievable for the devices using an organic cathode is lower than that without using the organic cathode. The cause of this phenomenon is unclear at this time. Since these are only preliminary results, we believe that the performance of the organic cathodes can be significantly improved via optimization of the synthesis process and selecting the proper chemical structure.

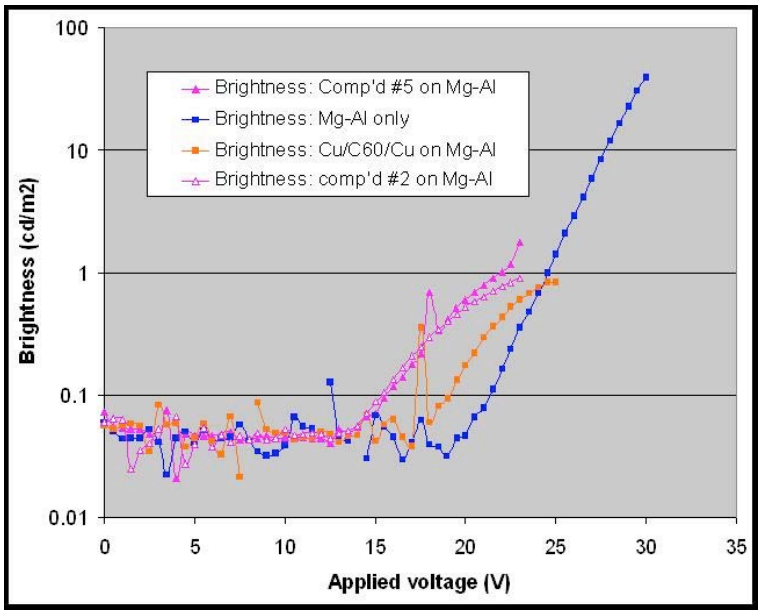


Figure 6. Comparison of the turn-on voltage and brightness of COLED using an organic cathode (pink. synthesized via Scheme I Path 3), a Cu/C60 cathode (yellow brown), and a Mg-Al alloy cathode (blue).

To select the proper organic molecule for the organic cathode, we used cyclic voltametry and UV-Vis absorption spectrum to determine the highest occupied molecular orbit (HOMO) and lowest unoccupied molecular orbit (LUMO) levels of the organic compound. Some of the determined HOMO/LUMO data are tabulated in Table 6.

Table 6. HOMO and LUMO Levels of some Compounds for Organic Cathodes

Compound	LUMO by CV (eV)	UV absorption peak (nm)	Band gap (eV)	HOMO (eV)
1	-3.2	362	3.43	-6.63
2	-3.7	305	4.07	-7.77
3	-3.9	345	3.59	-7.49
4	-3.5	306	4.05	-7.55
5	-3.5	300	4.13	-7.63
6	-3.6	340	3.65	-7.25
7	-4.1	316	3.92	-8.02
8	TBD	300	4.13	TBD
9	-3.8	309	4.01	-7.81
10	TBD	269	4.61	TBD
11	TBD	333	3.72	TBD
12	-4.1	347	3.57	-7.67
13	-3.7	299	4.15	-7.85
14	TBD	365	3.40	TBD

The performance of the above compounds as an organic cathode has not yet been fully evaluated at this time. So far we have only performed a limited test on a few of these compounds such as compounds #2 and #5. Although promising results are obtained from these preliminary experiments, much more research is required to fully realize the advantages of an organic cathode.

In future research, we will study in depth the relations between the chemical structure of the organic cathode, the deposition processes, and the performance of the COLED device. This will include optimizing synthesis processes of the organic cathode, and determining the HOMO and LUMO energy levels of the organic cathodes, and correlating the data to the performance of the resulting COLED devices. The knowledge acquired from this study will help us in pairing the proper organic cathode with the LEP molecule so that the optimal efficiency of the LEP can be realized. We will evaluate all the compounds listed in Table 6 and, at the same time, seek new candidate compounds that potentially have better performance.

TASK 3. OPTIMIZE CAVITY STRUCTURE

For the reasons discussed in the introduction, our original target was to reduce the cavity diameter and cavity spacing to approximately 1 μm in Year 1 and eventually 0.3 μm in Year 2 to achieve 20% of the active device area (effective device area / device surface area). Since the targeted cavity diameter is smaller than the wavelength of visual light, the physical dimension of the cavity might have effects on the optical properties of the COLED device. Therefore, we decided to perform a theoretical investigation on these issues before starting the actual experimental effort to generate cavities at the sub-micrometer level.

We performed optical simulation to investigate how the cavity diameter and spacing would affect the light escaping from the cavity; we have also performed theoretical calculations related

to the electric field distribution within the cavity as a function of cavity diameter and spacing, to establish a valid method to calculate the percentage of the active device area over the entire device surface area. We performed calculations to define the optimal cavity dimension that gives us the maximum active device area and allows the majority of photons to escape from the cavities.

New findings from these calculations suggest that we should retarget the final cavity diameter to 0.5-0.9 μm rather than the original 0.3 μm (see below for more details).

Task 3.1 Optical Simulation

To understand the light emission from an array of polymer channels, we have used the commercial electromagnetic simulation code HFSS (High Frequency Structure Simulator). This code solves the full 3D vector Maxwell's equations using a real space finite element mesh. The mesh is adaptively adjusted until a specified convergence is achieved. In Figure 7 we show the structure that was modeled. The dielectric function for the organic was assumed to be 2.56, for the SiN layer ε_{SiN} = 4.2, and for the Pt layer, values for the dielectric constant as a function of wavelength were taken from the literature. In this study, both square and hexagonal arrays were studied, with little difference in the findings. For the rest of the discussion we will refer to results from both array periodicities.

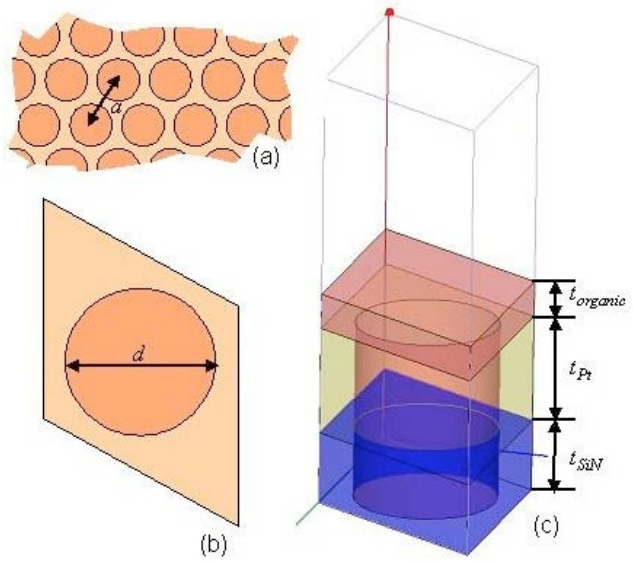


Figure 7. Structure modeled. (a) periodic hexagonal array with period *a*; (b) unit cell of structure modeled; (c) side view of structure modeled, showing bottom SiN layer of thickness t_{SiN} and a platinum contact layer of thickness t_{Pt}. Also shown is the cylindrical hole, which is filled in with organic material and with the hole overfilled with the organic by a layer of thickness $t_{organic}$. A perfect conduction layer is assumed to terminate the bottom of the cell.

The HFSS program does not allow for volumetric light sources as would be found in the OLED device being modeled. To develop an understanding of the impact of the hole diameter on the intensity of light escaping into the free space above the structure, we associated the base of the organic material with a wave port and examined the efficiency of the light escaping from the cylindrical hole. In some of the calculations we assumed that the wave port was located in the plane at the base of the platinum layer. Calculations were done using three wavelengths: 420 nm, 540 nm, and 620 nm. General conclusions are independent of wavelength, so for simplicity we report only the results for green light at 540 nm.

For the nominal case, we assumed $d_{organic}$=50 nm, d_{Pt}=150 nm, d_{SiN}=100 nm, and a nominal ratio d/a = 2/3. Table 7 shows the results of this study.

Table 7. Results of Optical Simulation Study on Hexagonal Array

Spacing	Hole diameter	Fraction of light (@540 nm) escaping
300 nm	160 nm	0.07
300 nm	200 nm	0.03
300 nm	240 nm	0.35

From Table 7 we notice that the fraction of light generated at the port that can escape into free space increases as the diameter of the hole increases. We noticed no differences in general if the hole diameter was held constant, but the periodicity changed, indicating that coherent effects associated with the periodicity are not important. It appears that there is a "cut-off" hole diameter of approximately 240 nm. When the hole diameter is smaller than this "cut-off" value, the majority amount of the light cannot escape.

More extensive calculations were performed in which the thickness of the organic on top of the structure was varied, an anti-reflection coating was added, and single and multimode excitations were used. The general conclusions were that for diameters of 600 nm and above, the majority amount ($\geq$ 80%) of the light can escape. However, since the calculations here assume a wave port excitation, whereas in reality the light is volumetrically produced, and mostly near the perimeter of the cylinder, this difference may have resulted in derivation of the theoretical results from reality. Therefore, the optimal cavity diameter will have to be determined experimentally.

In a separate calculation aiming at maximizing the active device area, it was also suggested that the cavity diameter should be targeted at the range of 0.5-0.9 μm (see below for more details). Based on these results, our future experiments will be targeted to optimize cavity diameter in the range of 0.5-0.9 μm and spacing of 0.2-0.3 μm (see below for more detailed discussion).

Quantum Size Effects in Light Emitting Material: During the annual review meeting (September 5, 2007), representatives from the Department of Energy asked whether the cavity size we selected based on the above calculations would result in a significant quantum effect on the emission wavelength of the COLED device. To answer this question, we asked SRI computational physicists to assess this concern. They concluded that for a cavity diameter of 0.3 μm and above, one would not expect the bandgap of the light-emitting material to deviate significantly from the bulk value. In other words, the quantum size effect is expected to be insignificant (more detailed discussion can be found in Appendix A).

Task 3.2 Reduce Cavity Diameter and Spacing

a) Theoretical analysis

Based on a preliminary estimation, it was assumed that both the cavity diameter and spacing need to be as small as 0.3 μm to achieve approximately 20% of effective/surface area. In a more precise calculation performed recently, we discovered that the percentage of the effective area versus the surface area reaches a maximum when the cavity diameter is slightly larger (by approximately 0.2μm) than the cavity spacing. For example, if the cavity spacing is fixed at 0.3 μm, the maximum effective/surface area of 22.7% is achieved at a cavity diameter of 0.5 μm. Further reduction or increase of the cavity diameter will result in reduction of the effective/surface area. On the other hand, when the cavity diameter increases from 0.5 μm to

0.9 μm, the reduction of the effective/surface area is very small (only drops by 2.6%) (Table 8). A similar phenomenon is also observed if cavity spacing is fixed at 0.2 μm or 0.4 μm.

Table 8. Effective/Surface Area as a Function of Cavity Diameter and Spacing

Diameter (μm)	Spacing* (μm)	Emission zone width (μm)	Effective/surface area (%)
0.7	0.4	0.1	18.0
0.6	**0.4**	**0.1**	**18.1**
0.5	0.4	0.1	17.9
0.9	0.3	0.1	20.1
0.8	0.3	0.1	21.0
0.7	0.3	0.1	21.8
0.6	0.3	0.1	22.4
0.5	**0.3**	**0.1**	**22.7**
0.4	0.3	0.1	22.2
0.3	0.3	0.1	20.2
0.3	0.3	0.15	22.7
0.9	0.2	0.1	24.0
0.8	0.2	0.1	25.4
0.7	0.2	0.1	26.9
0.6	0.2	0.1	28.3
0.5	0.2	0.1	29.6
0.4	**0.2**	**0.1**	**30.2**
0.3	0.2	0.1	29.0

* Spacing is defined as the edge-to-edge spacing of the adjacent cavities.

Based on the above calculation results, in order to achieve ≥ 20% active device area future experiments should be targeted at producing cavity diameters of 0.5 - 0.9 μm with spacings of 0.2-0.3 μm.

The electric field distribution within the cavity is expected to become more uniform as the cavity diameter becomes smaller. Therefore, the actual emission zone width in a small cavity may become larger than the estimated 0.1 μm, which may result in a higher value of effective/surface area than that estimated using a fixed emission zone width of 0.1 μm. To check for this possibility, we performed calculations on the electric field distribution within a cavity as a function of cavity diameter. It was found that significant widening of the emission zone is only observable when the cavity diameter is reduced to approximately 0.3 μm. The actual emission zone width of a 0.3 μm cavity increased to approximately 0.15 μm (Figure 8). However, this increase of emission zone width has only a very minor effect in the effective/surface area. The calculated effective/surface area using 0.15 μm emission zone width is only 2.5% larger than that estimated using the 0.1 μm emission zone width (see Table 8). On the other hand, since our

targeted cavity diameter is larger than 0.3 μm, results from calculations using the fixed emission zone width of 0.1 μm are valid.

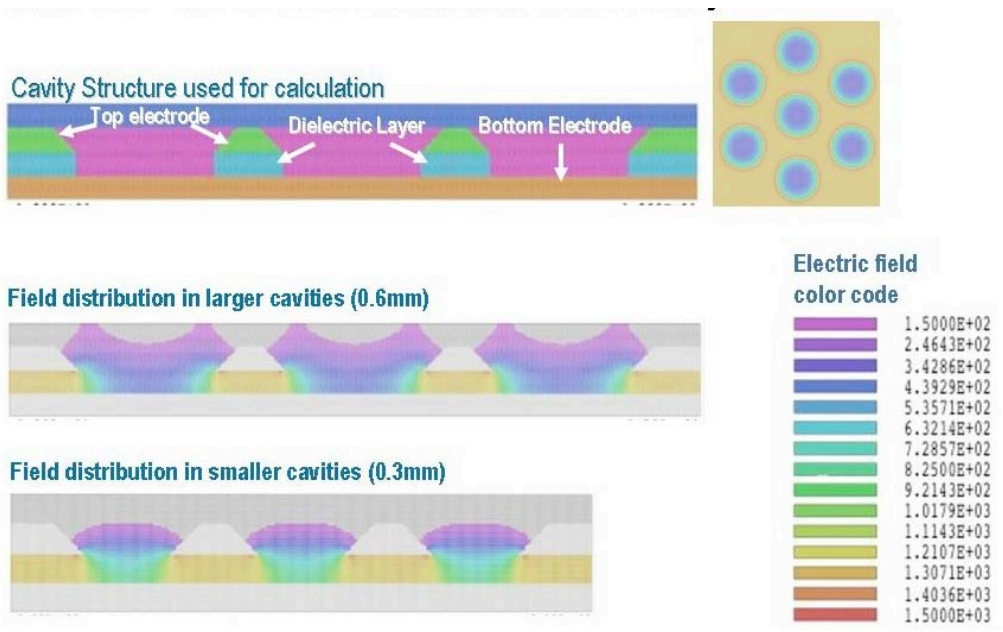


Figure 8. Electric field distribution within cavity as a function of cavity diameter.

b) Experimental approach

Because the emerging nanoimprinting technology can potentially reduce the production cost for COLED in future mass production, we originally proposed to use nanoimprinting technology for producing the cavity array of 1.0 μm (cavity diameter and edge-to-edge spacing) and below. However, the cost for a nanoimprinting mold is generally much higher than that of a standard photo mask. Since in the early development stage of this project, it is expected that several different cavity dimensions will be investigated, using nanoimprinting for this R&D effort will significantly increase the cost of the project (multiple molds are needed). After a discussion with the Department of Energy, we decided to use a two-step approach that would (1) use stepper lithography for the early stage developments and (2) develop the nanoimprinting process for the COLED fabrication once the optimal COLED design is finalized.

We initially selected Noel Technologies (Sunnyvale, CA) to perform the stepper lithography for generating the small cavities. We used two slightly different cavity dimensions:

a) Cavity diameter = edge-to-edge spacing = 0.8 μm

b) Cavity diameter = edge-to-edge spacing =1.0 μm.

Since Noel Technologies had experienced some technical problems with their stepper equipment, the progress in fabricating COLED using the above design was delayed by 2 months. To meet the deadline of the project, we negotiated and commissioned with two other companies, MEMS and Nanotechnology Exchange / CNRI, to perform this task.

In the first attempt, a positive resist was processed using default conditions. The resulting cavity diameter is significantly smaller than the designed values. For example, in the design using 0.8 μm cavity diameter and spacing, the actual cavity diameter achieved is approximately 0.5 ± 0.1 μm (actual edge-to-edge spacing = 1.1 ± 0.1 μm as shown in Figure 9). In addition, we noticed that a significant number of cavities were not opened (Figure 9, upper right). Thus, the actual device active area was significantly smaller than the theoretical value, resulting in no improvement in device brightness (compared with previous COLEDs using larger cavity dimensions). Analysis of the process revealed that these problems occur because of improper exposure dose used for the specific resist used in the process; this can be easily corrected by increasing the exposure dose. Since this experiment was accomplished near the end of the first fiscal year and the Department of Energy declined our request for a no-cost extension, we were not authorized to perform a second experiment to correct this problem, and further experimentation will have to wait until a new funding entity is involved in this development. This is the reason why part of milestone M12a for the first year plan is not met. Although we have exceeded the EQE of M12a, due to the reduced device active area, the device operating voltage is higher and brightness is lower than expectation. If we were given a chance to correct the resist exposure dose, all these specifications of M12a would have been met or exceeded.

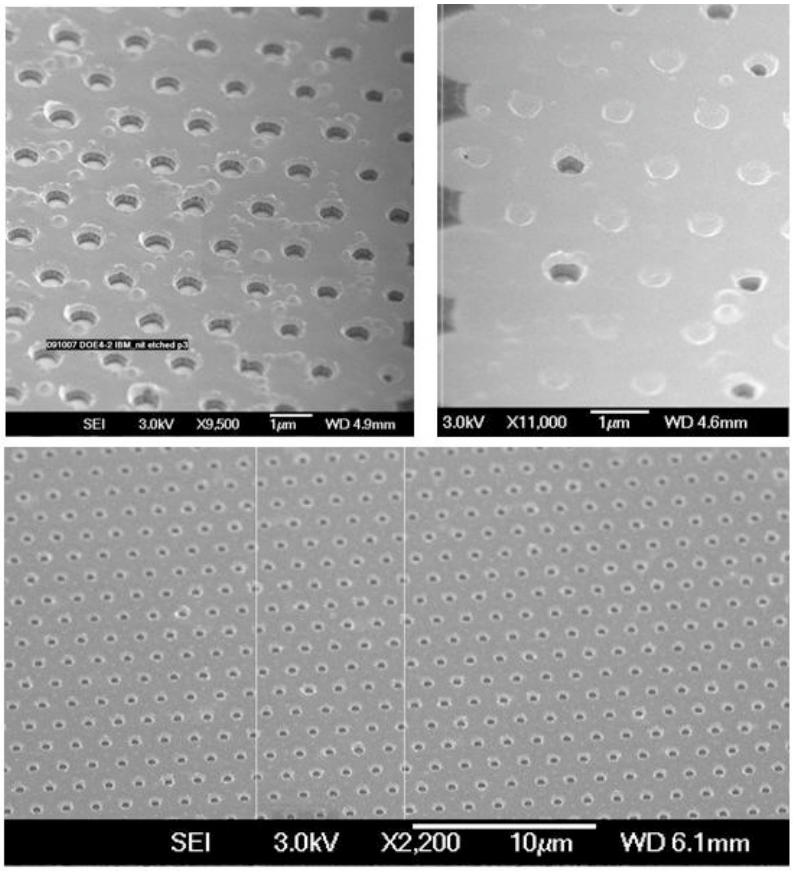


Figure 9. Result of the first attempt in using stepper lithography to generate a 0.8 μm cavity array: (1) cavity diameters are significantly smaller than the expected value of 0.8 μm and (2) some cavities were not opened due to incorrect exposure dope of resist.

Task 3.3 Top Electrode Material Selection (Year 2)

Although this task was scheduled to start in the second year, we started some preliminary work, together with Task 1, to study the validity of using a W top electrode (replacing the Pt top

electrode) in the COLED design. The earlier start of this task intended to accelerate the overall development of the optimized device by the end of Phase I.

The main consideration in replacing the Pt top electrode with a W top electrode is the cost, since Pt is much more expensive than W. Another potential benefit of using W as the top electrode is that W is more chemically reactive so that, when necessary, a proper chemical modification can be performed to improve the anode properties. In contrast, Pt is significantly inert, and only very limited chemistry could possibly be used to modify the Pt surface characteristic.

One challenge was the selective etching of the W vs. the Si_3N_4 layer. Unlike Pt, which is inert to the RIE process, W is etched by the fluorinated gas plasma used to etch the Si_3N_4 layer. Therefore, if the selectivity of the RIE process used for etching the Si_3N_4 layer is not high enough, a poor sidewall profile may result. The two SEM pictures shown in the top row of Figure 10 are examples of poor sidewall profiles resulting from poor RIE selectivity, which lead to non-functional COLED devices.

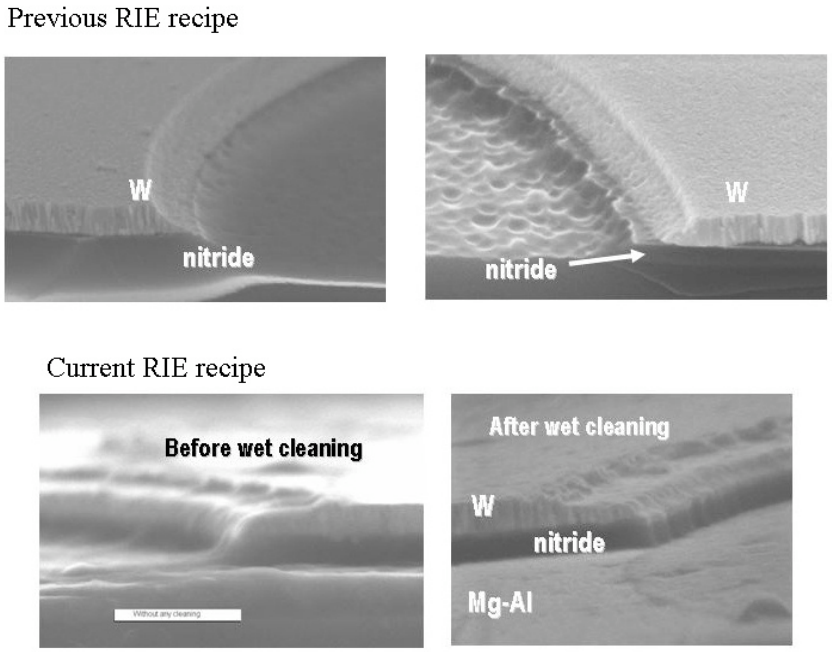


Figure 10. Cross-section SEM of cavity using a W top electrode after RIE of Si_3N_4

The RIE selectivity can be improved by properly adjusting the ratio of O_2 and the fluorinated gas. We performed several experiments to investigate this effect and have developed a recipe that can produce the desired sidewall profile (Figure 10, bottom row). Functional COLED devices using a W top electrode have been demonstrated by using this RIE recipe.

Although the selectivity has been improved, we noticed that the etching rate of W is fast resulting in widening of the cavity (or reduced cavity spacing). Therefore, future designs of the mask dimensions (cavity diameter and spacing) should take this phenomenon into account to ensure that the resulting cavity dimensions are as designed.

It was also noticed that after the RIE, there was a vast amount of residue deposited at the substrate's surface (Figure 10, bottom left), both inside and out side the cavity. While the majority of these foreign materials can be removed using an organic acid solution, there is a thin layer of material on top of the Mg-Al cathode that is not removable (Figure 10, bottom right). A similar phenomenon is also seen in COLEDs using a Pt top electrode. This grayish layer was identified as a mixture of oxides and fluorides of Al and Mg formed due to prolonged exposure to the RIE plasma. The existence of this contaminant layer significantly reduces the performance of the COLED (see below for more detailed discussion).

Task 3.5 Control of the Cavity Sidewall Profile (not part of the original plan)

Although this task was not a part of the management plan, we added this task after finding that the sidewall profile had a tremendous effect on the performance of the COLED devices. One reason for this effect is the sidewall profile of the top electrode that can affect the electric field distribution as well as the morphology of the spin-coated LEP. In addition, we have discovered that in certain circumstances there is a circular Pt wall (Pt ring) built up at the edge of each cavity after ion beam milling (Figure 11). The height of these Pt rings is roughly equal to the thickness of the resist used for the ion beam milling.

Further investigation revealed that these Pt rings are formed during the ion beam milling process by trapping the splashed Pt metal atoms on the sidewall of the photo resist. This phenomenon becomes much more significant when the resist layer has a straight or negative sidewall profile.

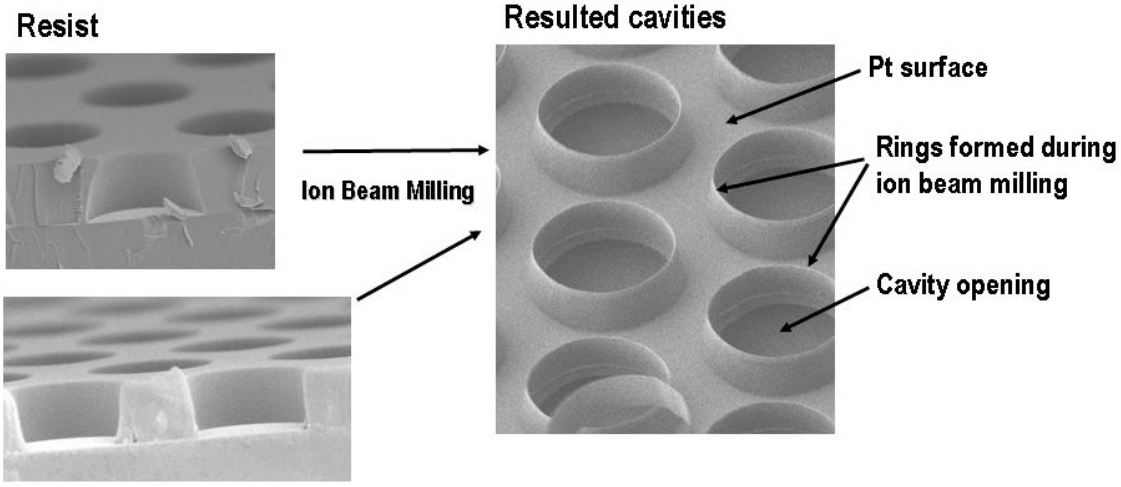


Figure 11. SEM image of a COLED (right) after ion beam milling and stripping off the resist. A straight or negative sidewall profile of the resist (left) results in Pt particle accumulation on the resist inner sidewall, forming a Pt ring on each cavity.

Although the above resist can be used to generate some sidewall profiles on the top electrode (see Figure 12), a unique observation by-itself, these extra rings are difficult to remove. In order to knock them off the substrate, we must sonicate the substrate in an acetone bath, a process that can be very inefficient and time consuming. We tried to increase the power of sonication, but high power usually results in a higher percentage of device failure (short circuit) of the COLED. We concluded that the buildup of Pt rings over the cavity should be avoided.

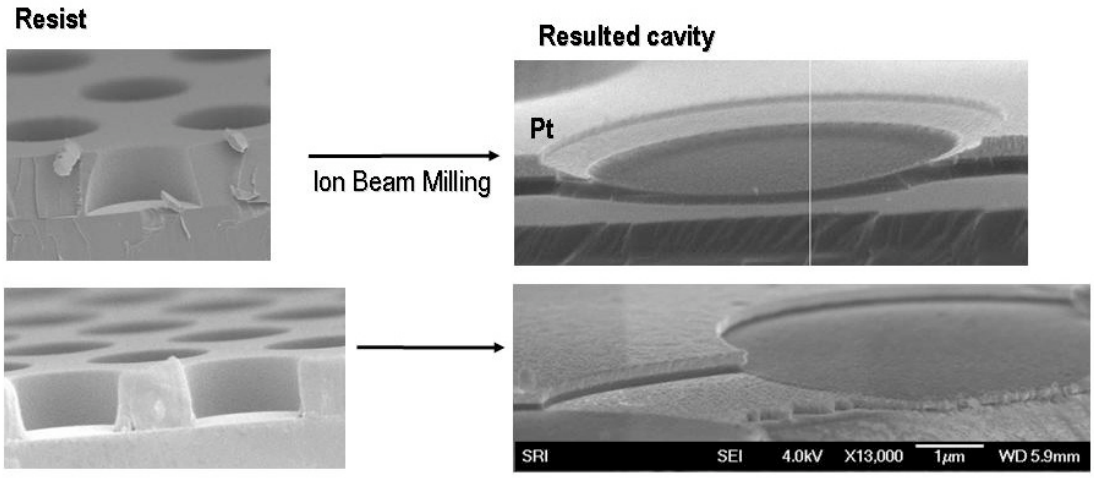


Figure 12. Correlation between the sidewall profile of the top electrode and the resist.

To avoid the formation of these rings, we switched to using a positive resist to generate a positive sidewall profile; i.e., the opening on the top of the resist layer is larger than that at the bottom (Figure 13). In the first attempt, we used a 1.4-μm-thick positive resist. After ion beam milling, a clean (no Pt accumulation) and nearly vertical sidewall on the Pt layer was obtained. It is expected that the sidewall profile of the Pt layer can be further controlled by the resist sidewall profile, which is adjustable by varying the exposure dose. In future development activities we will vary the sidewall profile of the Pt layer from ~90º to ~45º and study how it could affect the device performance.

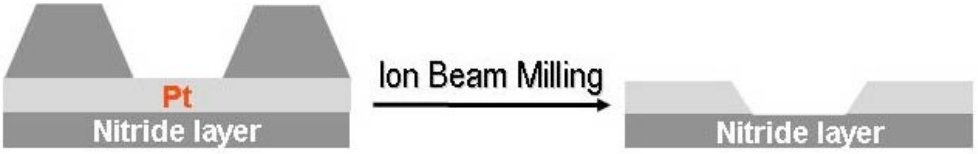


Figure 13. Desired resist profile that prevents accumulation of Pt on sidewall.

TASK 4. OPTIMIZE INTERFACES

Task 4.1 Optimize the Anode/LEP Interface

We have previously found that the COLED brightness and efficiency are improved by several orders of magnitude by incorporating a proper additive into the light-emitting polymer. We postulated that this is due to the improvement of the anode/LEP interface and/or the conductivity of the organic layer. In an effort to optimize the device performance, it is essential to understand the real mechanism behind this phenomenon.

To study the mechanism, we used the traditional sandwich OLED structure and fabricated devices on ITO glass with and without using the additive. The current-voltage-brightness (IVB) characteristics of these devices were determined and compared. From this study, the working mechanism of the additive has been understood. This will allow us to select or design the proper

additive for the individual LEP molecule to achieve optimal performance in the COLED structure.

We used scanning electron microscopy (SEM) to examine both the physical contact between the LEP and the top electrode and the filling of LEP into the cavity using different cavity aspect ratios. Figure 15 shows an image of a large cavity (left, aspect ratio ≈ 30:1) and a small cavity (right, aspect ratio ≈ 3:2). It can be seen that in both cases, the cavity was completely filled with the LEP and good physical contacts between the LEP and the metals were observed.

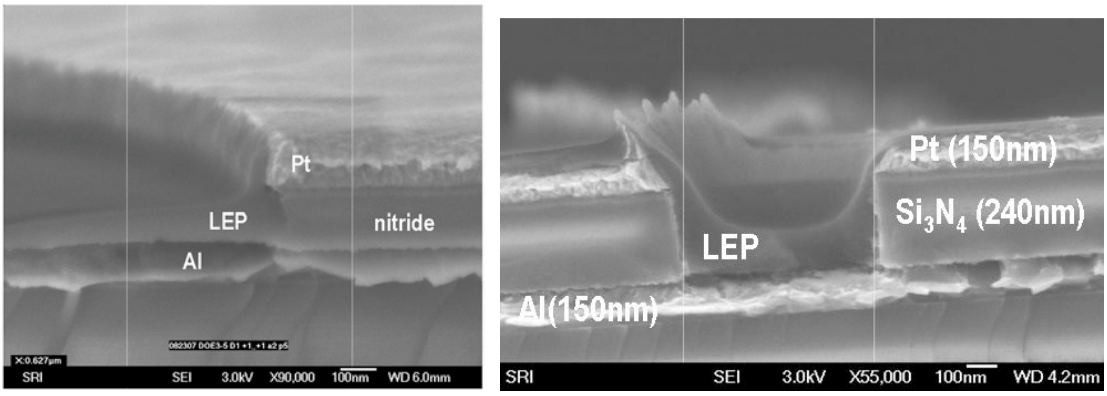


Figure 14. SEM image of a large cavity (left) and a small cavity (right) filled with LEP

In another attempt, we used a novel LEP material provided by a Japanese company. This polymer contains a "built-in" hole and electron transporters. This COLED device performed well without needing any additives. In the future, we plan to study the hole and electron transport properties of this novel material and optimize its performance by either using a proper additive or modifying the LEP chemical structure to maximize its efficiency in a COLED structure.

Task 4.2 Optimize the Cathode / LEP Interface

As mentioned in the previous sections, a thin layer of insulating materials was found on the surface of the Mg-Al cathode after the RIE of the Si_3N_4 (Figure 16). An energy dispersive x-ray analysis (EDAX) detected high contents of oxygen and fluorine elements, suggesting that the majority of the film is aluminum oxide and fluoride. Since the thickness of this layer varies from wafer to wafer, we attributed it to over-etching during the RIE of the nitride dielectric layer. It was found that the existence of the contaminants greatly reduced the performance of the COLED devices.

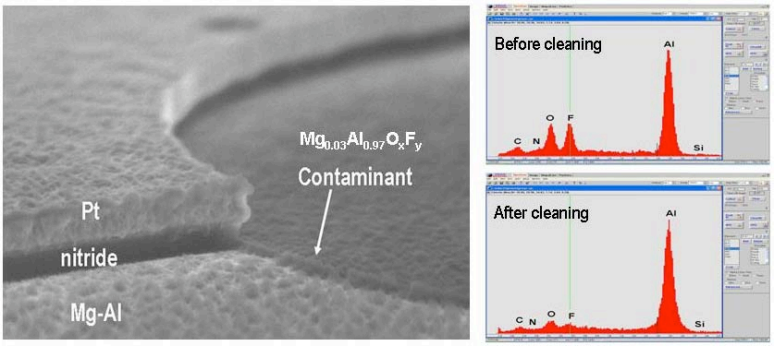


Figure 15. Chemical compositions of cathode surface contaminant by EDAX.

In the past, when an Al-Cu alloy was used, the cathode surface could be easily cleaned by soaking the substrate in an organic acid solution for 0.5-1 min. The current contaminants, however, could not be removed by washing with the same organic acid alone. We thus tried to use a combination of Ar sputter etch followed by soaking in the organic acid solution to remove this contamination. We first sputter-etched the substrate for 1 min, then soaked the substrate in the organic acid solution for 1, 5, and 15 min. We tested these COLED devices after coating them with an LEP solution. The device passing the 5 min organic acid soak time had the lowest turn-on voltage (~13 V) and the highest EQE of 0.2%. A longer soak time (10-15 min) did not improve the COLED performance. We examined the cathode surface with SEM and found significant surface roughening of the sample that had been soaked in the organic acid for 15 min (Figure 15, bottom right). The 5 min soaked sample, however, seems to retain some of the contamination. Since we have previously made devices with turn-on voltage of approximately 5 V, the fact that the turn-on voltage of this device is significantly higher (~13 V) suggests that the cathode surface was not cleaned completely.

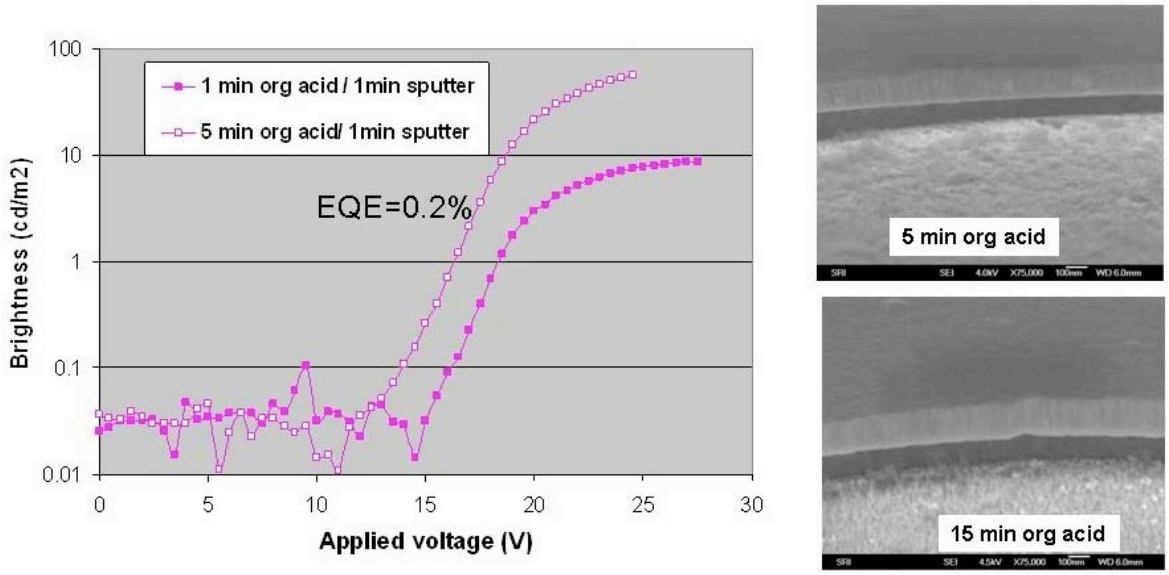
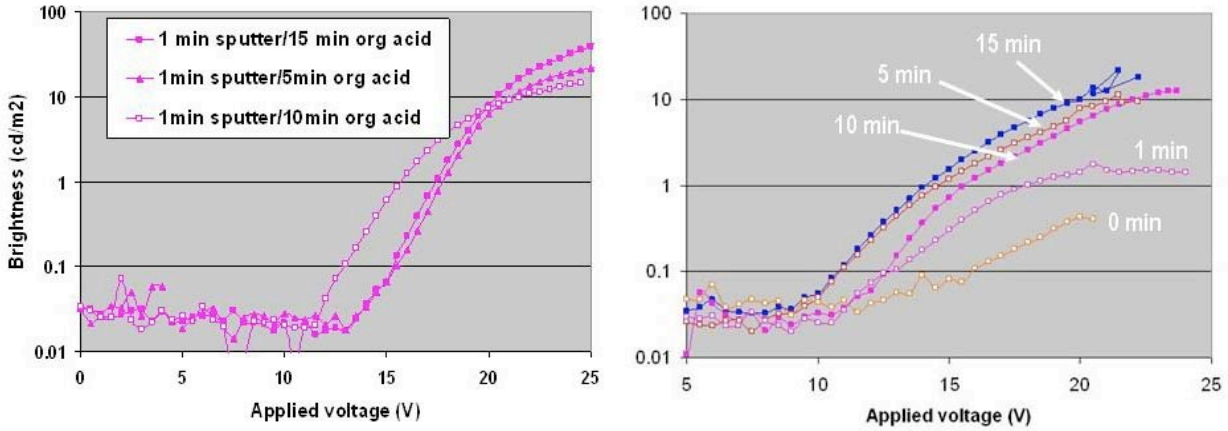


Figure 16. Effect of organic acid soak time on COLED performance.

We thus modified the cleaning recipe to use a 2 min sputter-etch followed by the organic acid soak. In this set of experiments, we used substrates from the same wafer and split them into two groups. Group 1 received a 1-min sputter-etch treatment, while Group 2 received a 2-min treatment. The device turn-on voltage for 5 min, 10 min, and 15 min soak time operations was essentially the same for both groups. If there is a difference between the 5, 10, and 15 min soak time, the difference is smaller than the substrate-to-substrate variations. On the other hand, the COLEDs receiving the 2 min sputter-etch time had a significantly lower EQE. This is probably an indication of damage of the cathode by the sputter-etch process (see Figure 18).



1 min sputter etch + 5-15 min org acid soak
EQE = 0.12%

2 min sputter etch + 0-15 min org acid soak
EQE = 0.056%

Figure 17. Effects of sputter-etch time and organic acid soak time on COLED performance.

It is thus clear that further development of a proper cleaning recipe for the Mg-Al cathode is very critical to the device performance. On the other hand, precisely controlling the RIE time to avoid over-etching and/or using a protective layer to protect the Mg-Al layer from being damaged by the RIE will be essential to ensure good device performance.

TASK 5. CHARACTERIZE DEVICES

We characterized COLED devices by measuring their current-voltage-brightness characteristics, and evaluated the quality of the dielectric layer by its leakage current and breakdown voltage. The COLEDs we fabricated using the old cavity design (cavity diameter / spacing = 8 μm / 3.4 μm and 4.85 μm / 2.38 μm) have shown an EQE of 0.2% (exceeded Milestone 12a of 0.1%) and ~80 cd/m^2 at 25 V (Figure 17). This was achieved under the condition that the cathode was contaminated (see above discussion). With a clean and undamaged cathode, we are confident that the performance of these devices will be much better.

The calculated active area of the old COLED design is 2.2% (cavity diameter / spacing = 8 μm / 3.4 μm) and 3.3% (cavity diameter / spacing = 4.85 μm / 2.38 μm). The newest COLED design uses 0.8 μm / 0.8 μm, corresponding to approximately 10% active area (theoretical value). Therefore, COLEDs using this new design are expected to be 3-5 times brighter and more efficient than what has been achieved using the old designs, which should achieve or exceed all the specifications defined by Milestone 12a. Unfortunately, due to the reasons discussed earlier, the COLED devices using this new design have much less active device area than the theoretical value, resulting in no observable improvement in device brightness and voltage although EQE has exceeded the expectation.

Milestone #12a: Status as of Sept. 30, 2007

EQE ≥ 0.1%; **Voltage ≤ 10V@100cd/m^2;** **Brightness ≥ 500cd/m^2;** **Local brightness ≥ 50,000cd/m^2**	**EQE=0.20%** **Effort abandoned due to termination of project**

CONCLUSIONS AND RECOMMENDATIONS

We have met or exceeded most of the milestones that are critical to the final success of this project:

1. We have succeeded in reducing the dielectric layer to 118 nm and improved the yield of the device to 91% (Milestone targets: 125 nm, 90%).
2. We have successfully developed a Mg-Al alloy cathode, and have demonstrated a Cu/C60 cathode and an organic cathode to be used in the COLED design.
3. We have determined the optimal cavity array dimension by theoretical calculation.
4. We have identified an ideal manufacturing partner, which has developed a unique phosphorescent light-emitting polymer that is most compatible with the COLED lighting mechanism.

All the above achievements are very critical to the final success of this project. Unfortunately, the Department o Energy decided to terminate this project because they did not accept the company selected by SRI as the manufacturing partner. SRI is currently discussing continuation of the development with several companies. With sufficient funding, it is expected that this technology will become mature in 2-3 years.

APPENDIX A: QUANTUM SIZE EFFECTS IN LIGHT EMITTING MATERIAL

John M. Baker, Zhi-Gang Yu, Marcy Berding

A volume of semiconducting material is expected to behave in a manner similar to that of bulk material unless its volume is small enough that the quantum mechanical character of electrons and holes becomes apparent. In a light-emitting material such as an LED, an electron in the conduction band recombines with a hole in the valence band, resulting in the emission of a photon with energy roughly equal to the bandgap. As the size of the emitting material is reduced, the energy of the emitted light will change due to the Coulomb interaction between the electron and hole (whose separation is now constrained spatially) and the interaction with the polarized material.

The question is: At what size do quantum effects become important enough so that the behavior of the material no longer mimics that of the bulk material? One of the primary characteristics of the material is the frequency of light emitted. If quantum size effects change the effective bandgap, then the material will no longer emit light at the expected frequency.

This problem was examined by L.E. Brus[4] in which a simple model of the electron-hole interaction is used to get an 'order of magnitude' estimate for the size of a material at which quantum effects become important.

In this work the electron-hole pairs are treated as bound pairs (Wannier excitons). A model Hamiltonian is constructed from which Schrödinger's equation has the form:

$$H\Phi = \left[\frac{-\hbar^2}{2m_e}\nabla_e{}^2 + \frac{-\hbar^2}{2m_e}\nabla_h{}^2 + V_0\left(S_e, S_h\right)\right]\Phi(S_e, S_h) = E\Phi(S_e, S_h)$$

The first two terms represent the kinetic energy of the electrons and holes. The potential V_0 includes the Coulomb potential between the electron and hole and their interactions with the surrounding medium. The energy obtained from the solution to this equation will shift the effective bandgap (Eg_{eff}=Eg+E) of the material and change the frequency of the light emitted. To understand the size effects, a variational calculation was performed on the following trial wave function:

$$\Phi = \psi_1(S_e)\Psi_1(S_h) + \beta_e\Psi_2(S_e)\Psi_1(S_h) + \beta_h\Psi_1(S_e)\Psi_2(S_h),$$

where the functions $\Psi_{1,2}$, are 2S wave functions for a particle in a sphere of radius R. In this problem the sphere radius represents the size of the light-emitting material. The two adjustable parameters, β_e and β_h, are determined by minimizing the energy E. The radius of the sphere is then changed and the procedure is repeated. In this way the change in the effective bandgap of a

[4] L.E. Brus, "Electron-electron and electron-hole interactions in small semiconductor crystallites: The size dependence of the lowest excited electronic state," J. Chem. Phys., **80**, 4403, (1984)

material is obtained as a function of radius. The following graph shows the results for a variety of semiconductor materials.[5]

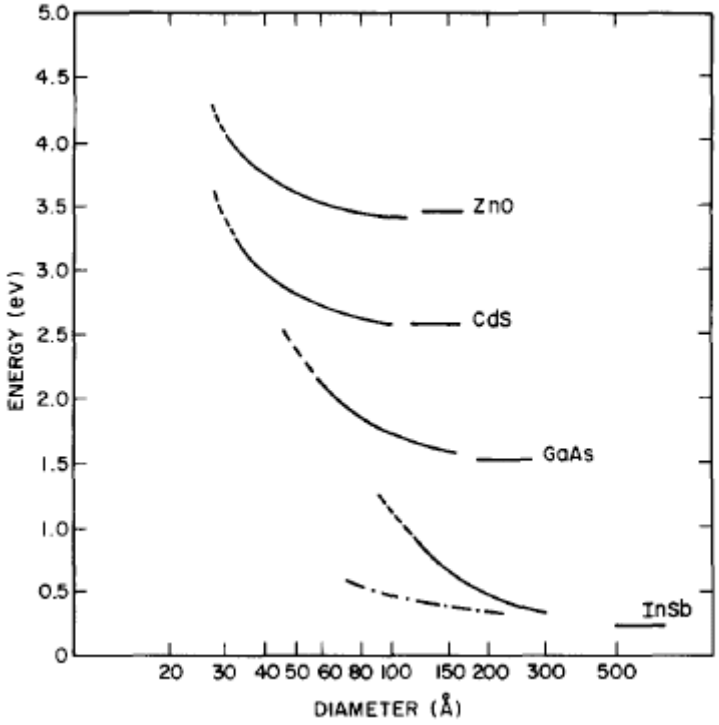


Figure A-1. Effective bandgap of a small sphere of semiconducting materials as a function of radius. The horizontal lines are the bulk values. Quantum size effects become important in the 100A range. (Image taken from Reference 5)

As can be seen from the figure, this model predicts that quantum size effects become important when the system size is reduced to a few hundred angstroms or less. For a light-emitting material 0.3 μm across (3000 A), one would not expect the bandgap to deviate significantly from the bulk value.