DOE PHASE II SBIR GRANT # DE-FG02-05ER84325

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BORON NITRIDE CAPACITORS FOR ADVANCED POWER ELECTRONIC DEVICES

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EXECUTIVE SUMMARY:

The ultimate goal of this project is to fabricate long-life boron nitride capacitors (as disclosed by the USDOE solicitation topic – Appendix A) for advanced SiC power electronics with a broad operating temperature range using a physical vapor deposition (PVD) technique. The use of vapor deposition provides for precise control and quality material formation. New efforts are directed towards optimization of the desired energetic, electrical, thermal, and frequency response properties of the BN–based capacitors. IMS is committed to continuing the successful Phase II effort in order to build industrial capacitor prototype devices for use in specific USDOE and commercial applications areas.

Growth of the capacitor layers was carried out successfully. Major contamination issues of the growth reactor were fully resolved and high quality layers were reproduced. Simulation data provided by the University of Houston's team on thermal and mechanical stresses in this multi-layered capacitor structure set limits in the thickness of films, in the deposition/operating temperatures, and device lifetime. Both wire bonded and surface mount types of capacitors were fabricated and evaluated. The BN capacitor structures tested so far exhibit good frequency stability from 10 kHz to 1MHz and also promising thermal stability in their capacitance values at up to 200ºC. Breakdown voltages for the ~90pF devices are typically 350V/µm in DC scanning mode, with the devices exhibiting stable I-V for 200 V static DC at 200ºC. The thermal admittance spectroscopy (TAS) and current-voltage-temperature (IVT) measurements made by SEMETROL, Inc. are used to further assist in optimizing the synthesis and processing steps by comparison to the established baseline. Improvements were based on reduction of concentration of traps that respond at the frequency of operation, and reduction of leakage paths.

FOLLOW-UP WORK AFTER COMPLETION (11/06/2010) OF PHASE II PROJECT BY IMS

As planned, IMS developed the $SiO_2/BN/SiO_2$ structure to produce electrostatic capacitors designed to operate safely at temperatures up to 350°C and above for use in silicon carbide (SiC) power transistors. The capacitors made so far were in low- medium

range of Farad rating and these scales are very low for most users according to the general reaction from experts we contacted. For better aligning our technology with the needs of end-users, the capacitance values should be increased to the scale of tens to hundreds of microfarads. **At its own expense, IMS has continued to improve the high temperature capacitor technology.** IMS investigated the possibility of making boron oxynitride (BON) layers for a totally in-situ process eliminating the need for ex-situ PECVD SiO_2 being used as diffusion barriers. This action permits a one-step, higher throughput and more reliable process for both integrated and discrete capacitors fabrication. Making BON capacitors with higher Farad ratings allows IMS to address a wide range of aerospace, transportation, and well logging capacitor applications. As anticipated we made significant progess in BNO layer deposition process on silicon substrates. The growth was optimized and the process flow was refined. The results on electrical and thermal characterizations of BNO capacitors were so promising that a US patent was filled on this technology.

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ENGAGED ACTIVITIES & FINDINGS:

1. Devices Growth

In the initial startup period we worked on setting up the high vacuum reactors needed for boron nitride (BN), silicon dioxide (SiO_2), and buried metal electrodes (i.e. Ti, Al) deposition. First, we deposited necessary capacitor layers to test our growth parameters on a small area capacitor. However, Scanning Electron Microscopy (SEM) pictures taken on initially deposited thin films revealed existence of surface particulates (Fig.1). The leakage current scales up with size of the capacitor chip which in turn is affected by the number of surface particulates. This effect could only be minimized if high quality (less defective) all buried layers are deposited. Surface particulates might also induce internal stress which causes changes in surface morphology leading sometimes to delamination (peelings-off) of the capacitor layers. Energy Dispersive X-ray Analysis (EDX) run on first series capacitors revealed trace of meal contamination (i.e. Ta, Al, Fe) due to low grade boron used for evaporation to form BN dielectric layers (Fig.2). This problem was subsequently overcome by using a higher grade boron starting material.

We have then undertaken a thorough cleaning of the PVD reactor. Metal flakes falling from the reactor walls caused a number of difficulties from time to time, as this is a research reactor that is also used to deposit metal plates for the capacitor chips. Eventually, this problem will be eliminated in a production process line where deposition of dielectric (BN) and metal is performed in separately dedicated but clustered vacuum chambers. The cleaning was necessary to minimize any sources of particulates and metal-flake contamination, which is critical for reproducibility and large scale integration of the future capacitor devices with SiC power electronics.

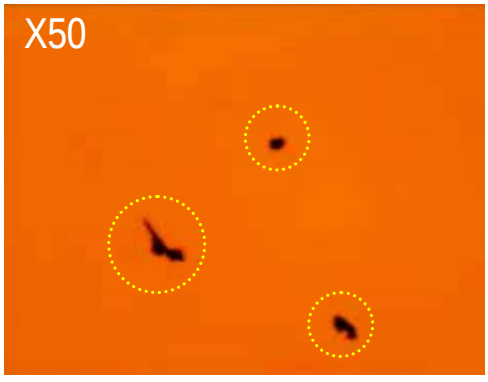


Fig.1 A typical SEM picture of 100 nm $BN/SiO_2/Si$ film showing existence of surface particulates

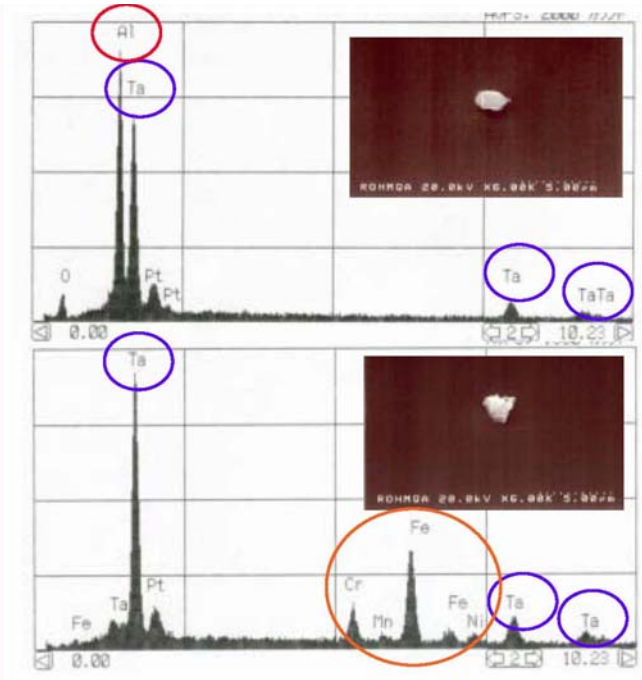


Fig.2 EDX results showing metal unexpected contaminants in BN/Si

EDX run on recent series of capacitors revealed **no trace of meal contamination** (Fig.3). The silicon and oxygen peaks are due to the substrate cleavage and native Si-O bound. Platinum (Pt) was introduced during the Focused Ion Beam/EDX cross sectioning experiment. Prior to cross sectioning, a thin layer of Pt was deposited on the BN area of interest in order to prevent possible sample surface charging during FIB operation and SEM/EDX analyses. The trace of carbon (C) is due to contamination introduced during the sample transfer and preparation. **Finally, the surface particulates and metal contamination issues were fully resolved.**

We also designed and fabricated new deposition stencil masks, which allow for multiple capacitor slots to be made in a single deposition process. We then made capacitors based on insulating thin boron nitride layers and conductive titanium (Ti) internal electrodes. The fabrication technique was based on ion assisted physical vapor deposition (PVD). Besides the boron nitride dielectric layer and metal electrodes, the current process flow requires also fabrication of diffusion barriers made of SiO_2 layers deposited by plasma enhanced chemical vapor (PECVD) technique. These intermediate layers prevent diffusion from the metal electrode through the BN active dielectric layer during high temperature growth, post growth annealing, and device operation.

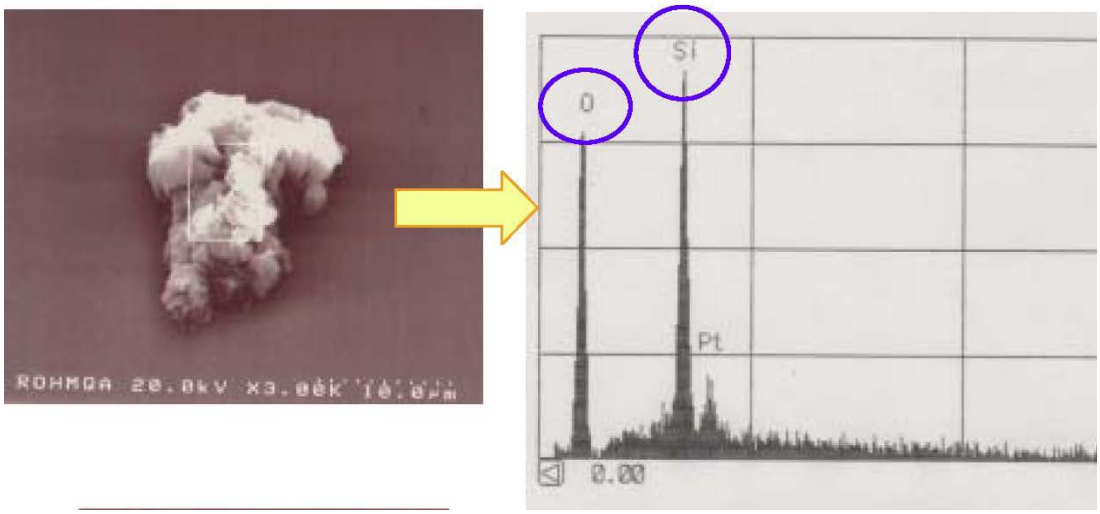


Fig.3 EDX results showing metal contaminants-free BN/Si

2. Design and Simulation

In order to minimize the number of expensive growth and processing runs and meet the device requirements, optimization of the capacitor design was performed by the University of Houston team. As a part of the subcontract with IMS, this team worked on thickness design and simulation to minimize thermal stress observed during the Phase I project in capacitors subjected to high temperatures above 300 ^{o}C. Thermal and mechanical stresses between the

film and the substrate and/or between the films inside the capacitor structure are believed to cause gradual layer delamination and eventually device degradation. The work of the subcontracting team was appropriate for preparing and fine-tuning designs *a priori.* The study and calculation of stresses in the multi-layered capacitor structure provided limits in the thickness of films, in the deposition/operating temperatures, and device lifetime. Theoretically the solid structure can be thermally or mechanically stretched (strained) by about **11%** before it breaks! Furthermore, if stretched just below that strain, it would return to the original condition when the external force is removed. Unfortunately, these predictions cannot be supported by experimental data. Most polycrystalline materials, whether they obey the Leonard-Jones potential or not, have an elastic limit of only **0.2%**; beyond that, plastic deformation sets in. The total film stress for both multilayered BN capacitors at different layer thicknesses was calculated versus different thicknesses of the thin films forming the capacitor chips. The simulations (see below) show that by using electrodes made of Ti/Al/Ti (instead of Al alone), a wide temperature operation range of up to 500°C can be achieved for the capacitors.

The specifications for each of the capacitors are given as follows:

1. Capacitor using Al electrodes: T1=25 ^{o}C, TF= 350 ^{o}C, Substrate: AlN (0.3 mm), Initial Film Thickness: Metal (Al) = 250 nm, Oxide (SiO_2 = 300 nm, SiO_2 capping layer = 1µm, Dielectric (BN) = 100 nm; Effective Stress ~ -250 MPa

2. Capacitor using Ti/Al/Ti electrodes: T1=25 ^{o}C, TF= 500 ^{o}C, Substrate: AlN (0.3 mm), Initial Film Thickness: Metal (Ti/Al/Ti) = 60/250/100 nm, Oxide (SiO_2 = 300 nm, SiO_2 capping layer = 1µm, Dielectric (BN) = 100 nm; Effective Stress = -49 MPa

Figure 4 shows total strain in a capacitor with Al electrodes exceeding the limit for plastic deformation (0.2%) at the given range of temperatures. When the capacitor is at temperatures from 25 ^{o}C to –300 ^{o}C the strain is slightly less than 0.2%. Unlike the case for Al, Figure 5 shows that total strain in the capacitor with Ti/Al/Ti layered metal electrodes does not reach the limit for plastic deformation (0.2%) at a given temperature in the range of up to 500 ^{o}C.

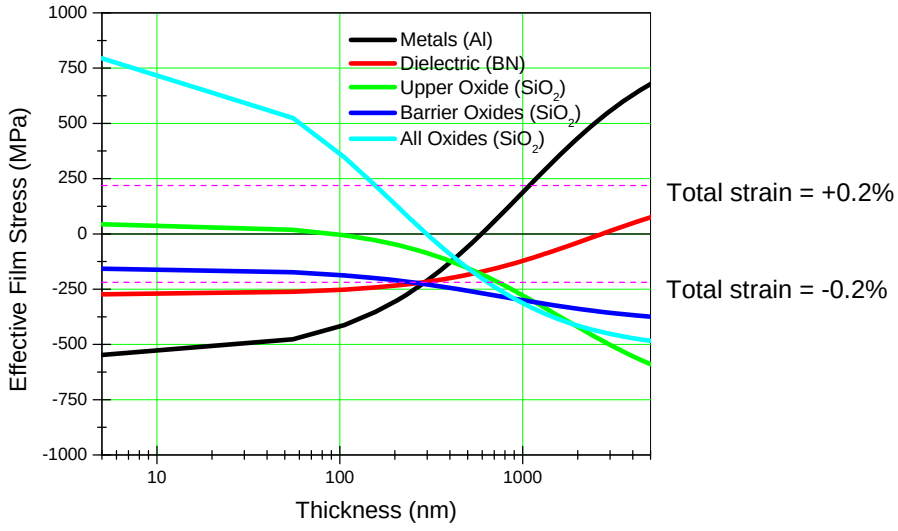


Fig. 4 Effective film stress vs. film thickness in a capacitor made by using Al electrodes.

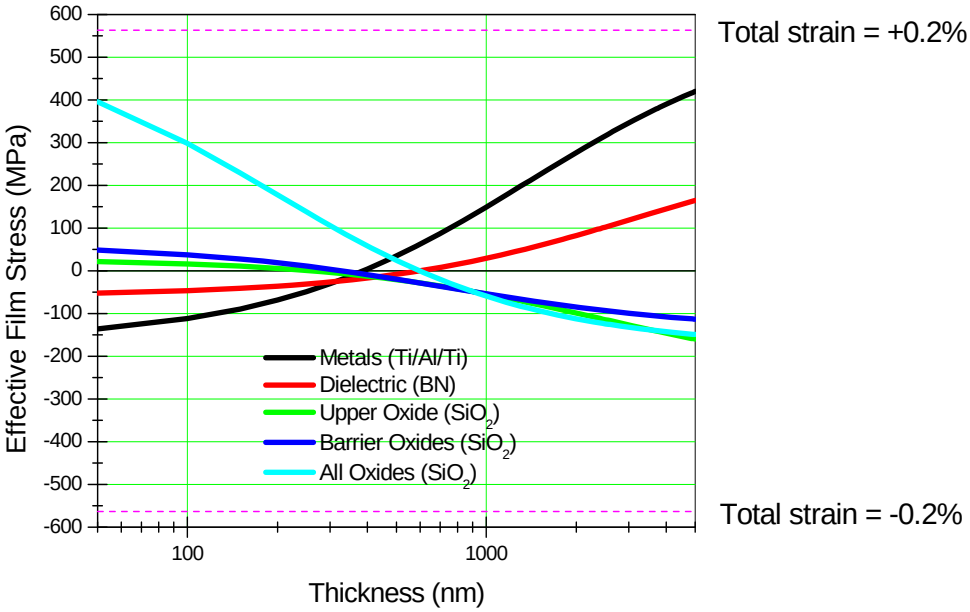


Fig. 5 Effective film stress vs. film thickness in a capacitor made by using Ti/Al/Ti electrodes

3. Fabrication of wire bonded capacitors:

The process flow for making typical wire bonded capacitors of about 100 pF uses a 200 nm thick titanium layer deposited on a silicon substrate through a stencil mask with openings of 0.5 x 3 mm. Openings correspond to the actual size of the capacitor that we anticipate to wire bond to existing SiC –based transistors used for high power high temperature operation. The mask allows for fabrication of 15 identical capacitors on a 2-inch diameter substrate in a single run. Fig.6 illustrates capacitors made on such a substrate along with a schematic of the layers forming the device chips. A 100 nm thick BN dielectric film was deposited between two SiO_2 protective barrier layers (300 nm thick each) using an End Hall ion source (< 100 eV N_2 ions) and evaporating a boron material at a substrate temperature up to 450 ^oC. Finally, the deposition of a second Ti layer (200 nm) was performed using a similar process. The above procedure can be repeated many times in order to achieve the desired capacitance values for a particular application virtually without an increase in the physical thickness of the device.

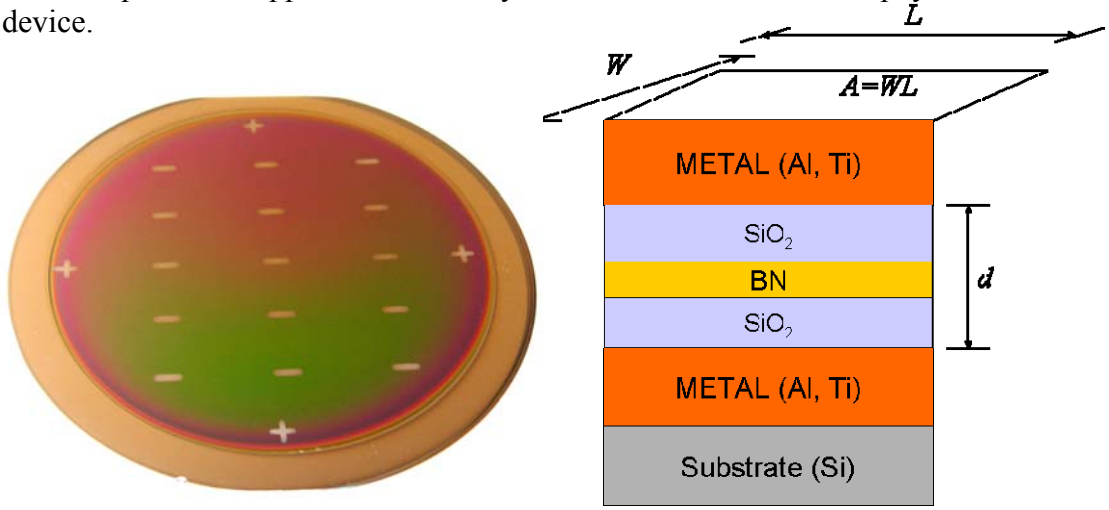


Fig. 6. BN based capacitors made on 2 inch dia. Si substrate.
A schematic of embedded layers is shown on the right.

Two sets of wire bonded type of capacitors were fabricated using the same process flow as previously reported. Device structure and layer thicknesses for both sets are as follow:

Structure: Ti/Al/Ti/SiOx/BN/SiOx/Ti/Al/Ti/Si
Ti/Al/Ti : 100/200/100 nm
BN: 100 nm
SiOx: 360 nm

Top and bottom electrodes are gold/Ni covered.
Au: 300 nm
Ni: 30 nm

4. Fabrication of surface mount capacitors:

The process flow of making typical surface mount capacitors with a medium range capacitance of 1 nF requires 100 nm and 300 nm BN and SiO_2, respectively. The growth parameters for making all layers are the same as in the case of the wire bonded capacitors fabrication. Top and bottom metal electrodes are made of aluminum sandwiched between two titanium electrodes. Ti is superior material for high temperature environment operation. A 60 nm thick titanium layer was deposited on a 3 –inch diameter aluminum nitride (AlN) substrate through a stencil mask with 6 x 7 mm openings covered by a silicon dioxide layer. A 250 nm thick aluminum layer was then deposited on top of titanium, followed by deposition of another 100 nm thick titanium layer. The Ti/Al/Ti stack was deposited by E–beam evaporation in a single run of the PVD reactor. Testing of the tri-layer electrodes indicated fulfillment of two important requirements for the intended BN based capacitors.
First, the presence of Al in the middle of the stack **minimizes the series resistance** of the effective electrode, a requirement critical for stable high frequency operation. In fact, the equivalent resistance of the parallel stack is less than that of aluminum alone. The four-point probe measurement technique gives a sheet resistivity on the order of 1.5 μΩ.cm versus 2.65 μΩ.cm for pure aluminum.

Second, Ti layers act as metal barriers preventing aluminum diffusion at **capacitor operating temperatures** right below the Al melting point. Employment of the Ti layer alone is acceptable for higher operation temperatures, but not suitable for high frequency operation. Finally, a 1 μm thick SiO_2 layer was deposited as a capping layer on top of the complete capacitor structure. Rectangular electrodes are offset and layered to build up the capacitor chip. The capacitor geometry allowed for easy alignment and simple dicing, of the 3-inch wafer to yield about 30 identical EIA 1825 standard capacitors sizes (4.5x6.4x1.6 mm) rectangular capacitors (Fig.7). The capacitors were then loaded onto a mask and about 1 micron thick Ti/Al metal contacts were deposited using E-beam evaporation technique on both sides. For this purpose a special holder that provided a 45° substrate tilt was used. These fabricated capacitors are similar to low-temperature commercial ceramic capacitors which usually come in different capacitance values, max voltage and temperature. The proposed BN capacitors will however tolerate much higher temperatures (> 300 ^{o}C).

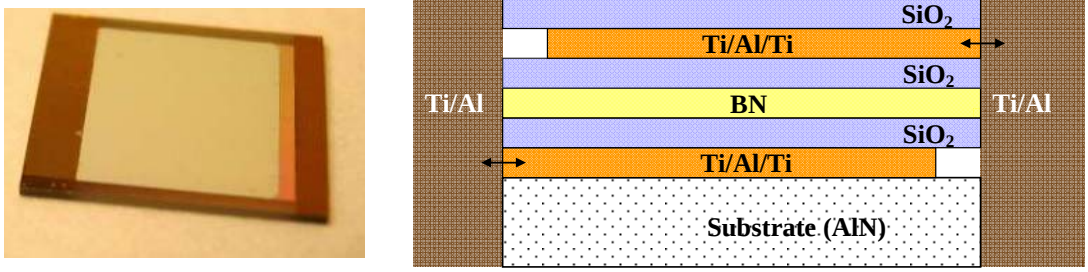


Fig.7. A diced 4.5 x 6.4 mm size capacitor chip. A schematic of embedded layers is shown on the right

5. Device Processing

Boron nitride-based micro-capacitor structures have been processed in two photolithography steps using two new photomasks, one for reactive ion etching (RIE), and the second for chromium/gold deposition. The chromium underlayer improves adhesion of the gold layer used for micro-bonding. Consequently, wire bonding between the capacitors and the bonding pads was then performed successfully. Optical Emission Spectroscopy data was recorded during the RIE process. The time variations of the TiCl (419 nm) and SiO (249 nm) OES signals during the RIE of a MicroCap-2 sample indicates the end point detection at 130 min etch time. Finally, we propose to use a typical meal oxide semiconductor capacitor layout for easier integration in circuits.

5.1. Processing steps:

Samples, having Ti/Al/Ti (deposited using a stencil mask) / (380 nm) SiO_2/(100 nm) BN/ (380 nm) SiO_2/ Ti/Al/Ti/Si(100) wafer, were processed as follows:

1) Photolithography using the Futurrex NR-9 1500PY photoresist and the photomask "Mask 1"to pattern the "via" down to the lower Ti contact.
2) The samples were etched down to the lower Ti contact. This was done using the following RIE conditions: 10 sccm BCl_3, 10 sccm Ar, 22 mTorr reactor pressure, 100 W RF power, and -200 V self dc bias.
3) The samples were then cleaned in acetone to remove all the resist left after the RIE. A second photolithography using the Futurrex NR-9 1500PY photoresist and the photomask "Mask 2" was used on the sample to pattern the contact pads.
4) Cr (10 nm thick, for the last 2 samples)/ Au (680 nm thick) layers were then deposited by e-beam evaporation. Finally, a Cr/Au lift-off process was performed by dissolving the underlying photoresist pads in acetone.

5.2. Endpoint detection:

We used an Ocean Optics PC 2000 UV-VIS miniature fiber optics spectrometer having a resolution of 1.5 nm (FWHM) for etching endpoint detection. Optical Emission Spectroscopy data was recorded under the following RIE conditions: 10 sccm BCl_3/10 sccm Ar, 100 W RF

power, -190 V self bias voltage, 22 mTorr reactor pressure. Spectra recorded were performed without, then with a 2" Si wafer in the reactor. Analysis of this data shows strong SiO and TiCl peaks at 249 nm and 419 nm, respectively, when the Si wafer is being etched. Hence, they can be used as endpoint detection for the Si interface (Fig.8). The time variations of these OES signals during the RIE of a MicroCap-2 sample are shown in Fig.9, indicating the endpoint detection at 130 min etch time.

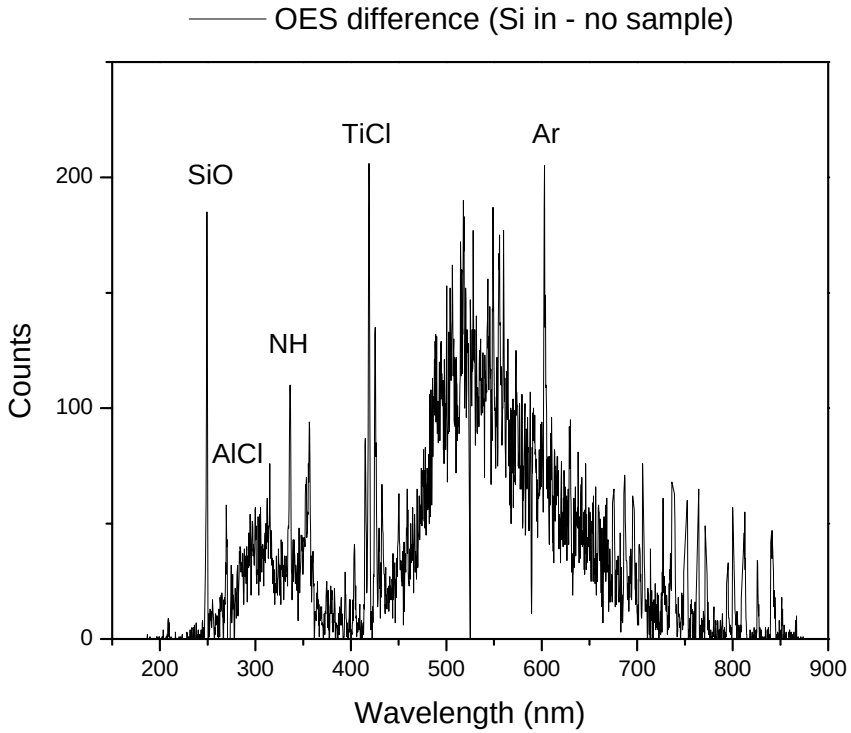


Fig. 8. OES data of BCl_3/Ar plasma with a 2" Si wafer minus the signal without the Si wafer in the reactor.

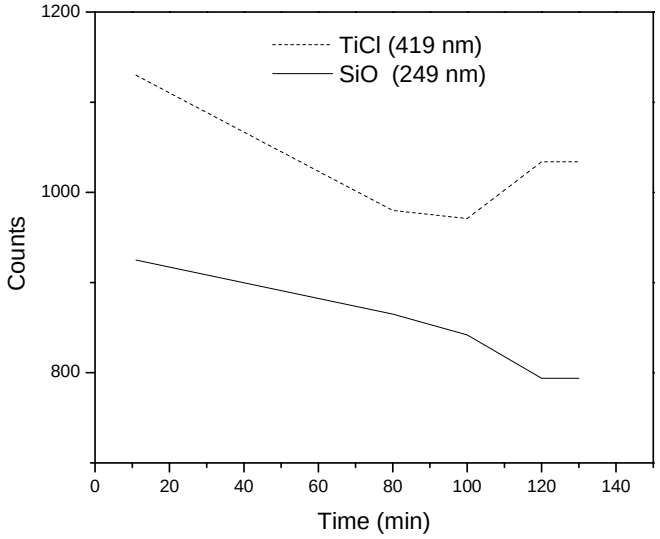


Fig. 9. Time variation of TiCl and SiO OES signals during the RIE in BCl_3/Ar plasma of a MicroCap-2 structure in the reactor.

5.3. Masks:

In-house made "transparency" masks used initially resulted in poor quality device yield. Hence, two high quality photomasks were designed and ordered from HTA Photomask.

5.4. Metal contacts:

Wire bonding to gold contacts deposited directly on SiO_2 peeled off. Therefore, a 10 nm-thick chromium layer was used successfully as an adhesion layer to the gold contact, making bonding to the Au pads very reproducible.

5.5. Wire Bonding:

We worked on wire bonding the metal electrodes of the capacitor to gold pads. In a real electronic package, these pads could represent external devices attachments. Purposely, we used these pads to probe and characterize fabricated capacitors. A Thermosonic ball bonding machine and a gold ~30 μm thick bonding wire was used for this purpose. Prior to wire bond directly on the device, we first tried bonding on a sample silicon substrate coated with 0.5 μm thick gold layer with a 10 nm thin layer of Cr underneath. In this fashion different combinations of bonding parameters were tried and the bonding was optimized for the gold layer deposited on the silicon.

Bonding on plain gold samples gave us the much needed confidence to proceed and wire-bond the actual device. The actual device metal electrodes were covered with gold to enhance/improve adhesion of gold-gold bonding. SEM Images of the bonded devices were taken. The optimized bonding parameters which gave us reproducible results are tabulated below.

Bond	Loop	Search	Force	Time	Power
I	-	5.0	7	7	7.30
II	7	5.30	5.5	6	8.0

Gold wires bonding were then performed successfully after cleaning the samples thoroughly in boiling trichloroethylene, acetone, and methanol (Fig. 10)

The use of photomasks instead of "transparency masks", chromium adhesion layers for the gold pads, and Optical Emission Spectroscopy for endpoint detection had a critical impact on the processing of the microcapacitors, resulting in much improved devices.

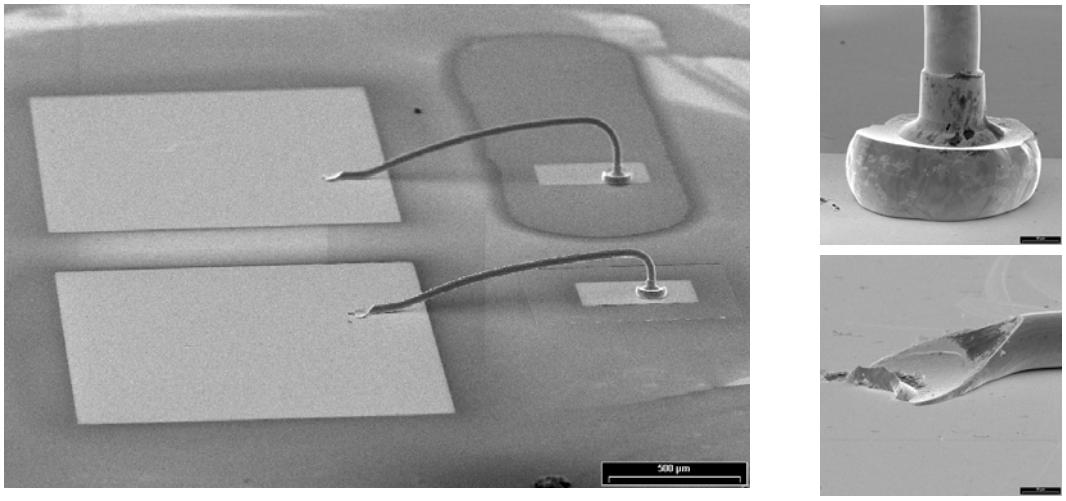


Fig.10. SEM picture of a wire bonded microcapacitor prototype. Higher magnification SEM views of the bonds are also shown.

6. Device Characterization

6.1. In-house Characterization Activities

There were three primary activities for the characterization tasks in the course of this project. In the early stages of the project, we began making improvements in our capacitor I-V measurement setup. This was necessary due to the large noise currents present in the measurement apparatus used in the Phase I project. The new I-V station employs a better picoammeter/voltage source. The change of picoammeter required modifications to our in-house software that drives the measurements. These changes were implemented and tested for functionality. In addition, we have transitioned to triaxial cables for the I-V input to the picoammeter to greatly reduce EM interference and current leakage in the cables. Higher quality cabling has also been used on the probes and the voltage source to improve system performance. Overall, our measurement accuracy has improved by a factor of 10000 for very low current levels. We are also in the process of implementing a shielded enclosure for our probe station to further reduce light and EM interference in the measurements.

The second activity has been compositional analysis of the BN layers. This is related to the investigation of leakage currents in our capacitor structures. Our belief is that one possible leakage source is the incorporation of impurities into the BN layers during film deposition. In order to test for contamination, we have grown a series of layers and had them analyzed by X-ray Photoelectron Spectroscopy (XPS) and Secondary Ion Mass Spectroscopy (SIMS). XPS did not reveal any metal contaminants, but SIMS found significant levels of Al and Fe. These impurities have been substantially reduced by employing a higher-grade boron source material.

The third activity has been electrical measurements of the capacitor structures. Capacitance, quality/dissipation factor, and impedance have been measured for the various layers fabricated. The capacitance value measured at RT and 200 ºC in air varies by <5% from 10kHz to 1MHz. Scanning I-V and static I-V measurements have been performed on a few selected devices in order to quantify the leakage currents and breakdown voltages in the capacitors. For low DC voltages, leakage currents on the order of 50pA at RT and 10pA after several hours of annealing at 200ºC have been recorded. At 200 volts DC, leakage is 50nA at RT. Breakdown measurement performed at RT indicate a BDV around 250V for a total dielectric thickness of 0.7 μm.

1. I-V measurement system

The I-V measurement system used during the initial period of the project had major shortcomings when trying to measure very low currents, such as the leakage currents in our capacitors. The issue was that the measurement noise current was proportional to the scan voltage. This is shown in Figure 11 below. Although the picoammeter was rated at a background current of 1nA, such accuracy was only possible at very low voltages. To measure the leakage current of the capacitor structures, hundreds of volts are needed, which of course leads to high background currents, even for an open circuit configuration. After switching to the new picoammeter/voltage source, the problem has been completely eliminated. The background noise current is solely determined by the measurement current scale sensitivity and not by the drive voltage. With a noise current on the order of picoamps at highest sensitivity, our leakage current measurement accuracy has improved by ~10^4 – 10^5, even without the EM shielding. The only downside to this particular unit is that it has a maximum drive voltage of 500V and a maximum current of 2.5mA at 500V.

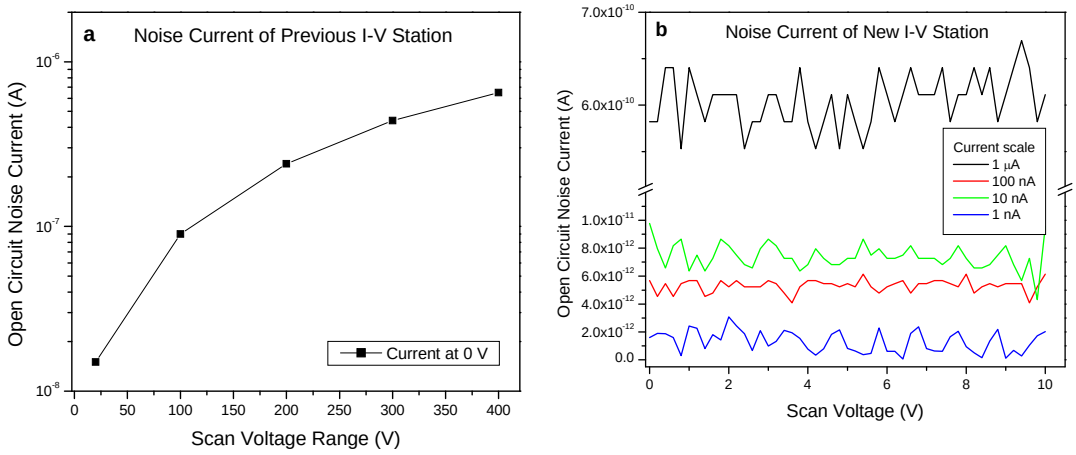


Fig. 11. (a) Plot of the open circuit current (noise) versus scan range for the I-V system used during the Phase I project. (b) The new system implemented in the Phase II has a much lower noise floor which is independent of the scan voltage range and is thus more appropriate for capacitor I-V characterization.

2. Compositional analysis of BN layers

X-ray photoelectron spectroscopy and secondary ion mass spectroscopy have been performed on some of our BN layers by Evans Analytical Group (EAG). XPS data from one of the samples is shown below in Figure 12. For this film, the sample was sputtered approximately 100 nm into the layer before a survey scan was taken. Only peaks corresponding to B, N, Ar, and O are present to within the sensitivity of the instrument (~0.1-0.5%). The presence of approximately 6% O_2 is due to two factors: a small amount of incorporation into the BN film and a re-deposition of surface oxygen during the sputtering process. In either case, the presence of a small percentage of O is not a cause of concern since boron oxide is also a dielectric material.

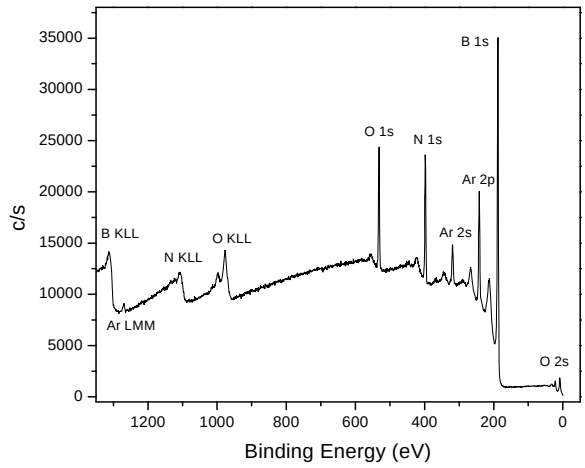


Fig. 12. Plot of the XPS analysis of a 300nm BN film on silicon. Only B, N, Ar (sputtering beam), and O are present in the film.

Following the XPS analysis, SIMS was performed by EAG to look for likely contaminants based on our chamber configuration and source material impurities. Al, Fe, and Cr at levels above $10^{18}cm^{-3}$ were found on some samples. AlN and CrN are ceramic materials, so are therefore not likely a contributing factor to the BN electrical properties. We have tracked the impurity levels of a series of BN films and have discovered that, in almost all cases, the various impurity concentrations go down with increasing growth number. Thus, later samples typically have fewer impurities. Data for Al, Cr, and Fe levels in a four sample series is shown below as lines in Figure 13. Note that the chamber was not vented to atmosphere nor used for other depositions. Only BN was deposited in this series. Since the impurities are all metals and not gaseous or liquids, this would rule out the chamber vacuum as the cause of the impurities. The most likely remaining cause is the boron source material itself. The impurity level data (vendor supplied) supports this hypothesis in that the Cr, Fe, and Al impurities (which have lower melting points and/or higher vapor pressures than the boron) drop rapidly with usage. After switching to a higher grade of boron, the levels of these impurities was greatly reduced, as can be seen by the markers in Figure 13.

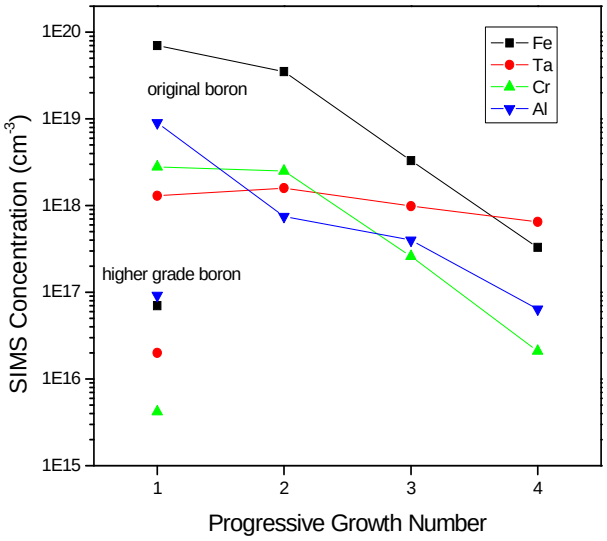


Fig. 13. Plot of various metal impurities present in a series of four BN layers as a function of run number. The reduction of impurity levels as more runs are performed points to the source materials, specifically boron, as the most likely cause of the contamination.

3. Electrical measurements of BN capacitor structures

Capacitance, quality/dissipation factor, and impedance have been measured for the various BN capacitor structures fabricated. Some devices have been measured only as-fabricated, while others have been subjected to burn-in up to 350ºC in vacuum and in air. Both types have been heated to 200ºC in air and C-I-V measurements performed. Overall, the capacitance of the structures typically varies by <less than 5% from 10kHz to 1MHz with Q factors from 50-115. Shown in Figure 14a is the capacitance of one device, which was pre-treated at 350ºC in air before a 139 hour anneal at 200ºC. The capacitance is very stable over this time at this temperature with a decrease of only 1%, most of which occurred in the first 24 hours. For comparison, the device shown in Figure 14b was not pre-treated. As a result it exhibits a 4.5% decrease in the first 4 hours, but only a 0.6% decrease over the next 18 hours. This is an early evidence of excellent device stability at 200ºC for extended periods.

DC I-V measurements in both scanning and static modes have been performed on the capacitor structures. In scanning mode, the devices exhibit a resistance of ~15GΩ at 10V, and resistances of 2-3 GΩ and 1-2 GΩ at 40V and 100V, respectively (Figure 15a and 15b). At 200V, the resistance is essentially the same as at 100V. This data corresponds to a leakage current of approximately 0.6nA at 10V, 15nA at 40V, 60-80nA at 100V, and 120-160nA at 200V.

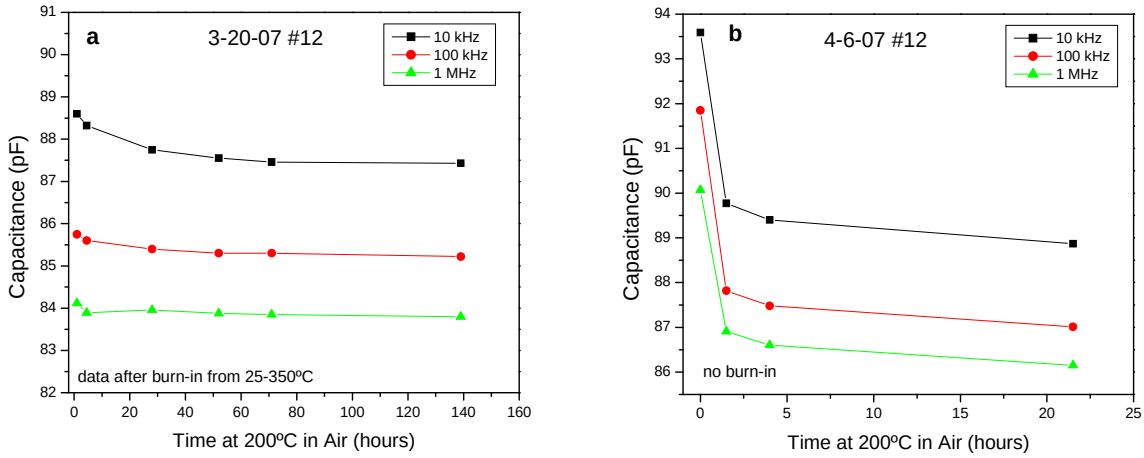


Fig. 14. (a) Time dependent capacitance of a burned-in device held at 200ºC. ΔC is ~1% over the full time range, and 0.4% from 28-139 hours. (b) Time dependent capacitance of a device held at 200ºC that was not burned in. ΔC is ~5% over the 22 hours, but only 0.4% from 4-22 hours.

DC I-V measurements in both scanning and static modes have been performed on the capacitor structures. In scanning mode, the devices exhibit a resistance of ~15GΩ at 10V, and resistances of 2-3 GΩ and 1-2 GΩ at 40V and 100V, respectively (Figure 15a and 15b). At 200V, the resistance is essentially the same as at 100V. This data corresponds to a leakage current of approximately 0.6nA at 10V, 15nA at 40V, 60-80nA at 100V, and 120-160nA at 200V.

At 200ºC, the I-V of the samples was also measured. Shown in Figures 16a and 16b are the 0-10V and 0-200V scans taken at several time points. No prior burn-in of these devices was performed. At low DC voltages the leakage currents are reduced significantly with time at 200ºC, while the high voltage scans show first a strong reduction in leakage followed by a slow increase back near the initial levels. Such behavior is not yet understood.
Static measurements were also performed while the sample was at 200ºC. Shorter measurements of 30 seconds exhibited similar behavior to longer (~30 minutes) tests. Shown in Figures 17a and 17b are static scan data for 10V and 200V, respectively. Steady state leakage at 10V showed a decrease from ~60pA to 10pA as the sample stayed at 200ºC, but went up at 200V from ~45nA to 420nA over the same period. The cause of both the scanning and static I-V behavior at different voltages is believed to be due to the SiO_2 layer in the capacitor structure, but more investigation is needed to verify and address the issue.

Finally, room temperature breakdown measurements of the devices were performed. The structures typically exhibited a BDV of ~250V for a total dielectric thickness of 0.7 μm as illustrated in Figure 18. It should be noted that the I-V sourcemeter/picoammeter has a

current limit of 2.5mA at voltages above 10V. Thus, the structure was not completely "broken" at 255V as indicated by the second scan which was performed after the initial break scan.

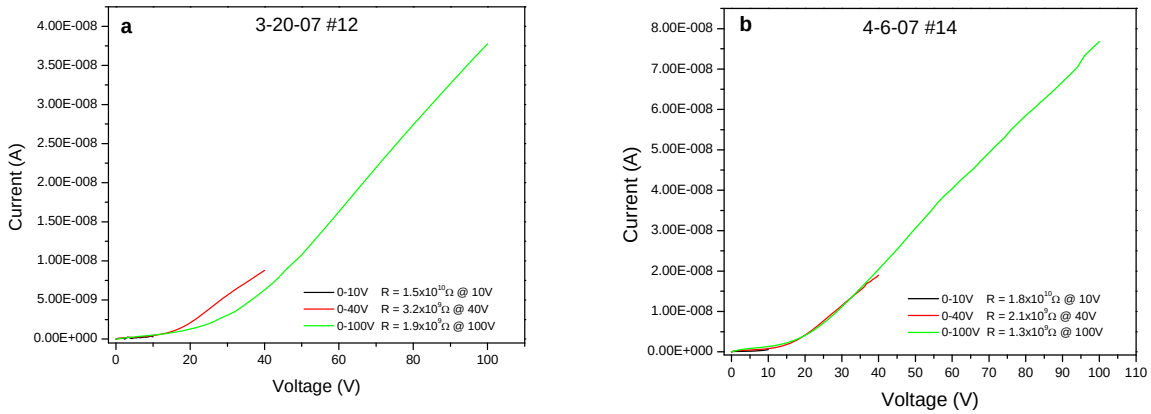


Fig. 15. Room-temperature scanning I-V measurements for BN capacitor structures processed in (a) March 07 and (b) April 07. The device resistance varies from ~15GΩ at low voltages and 1-2GΩ at higher voltages.

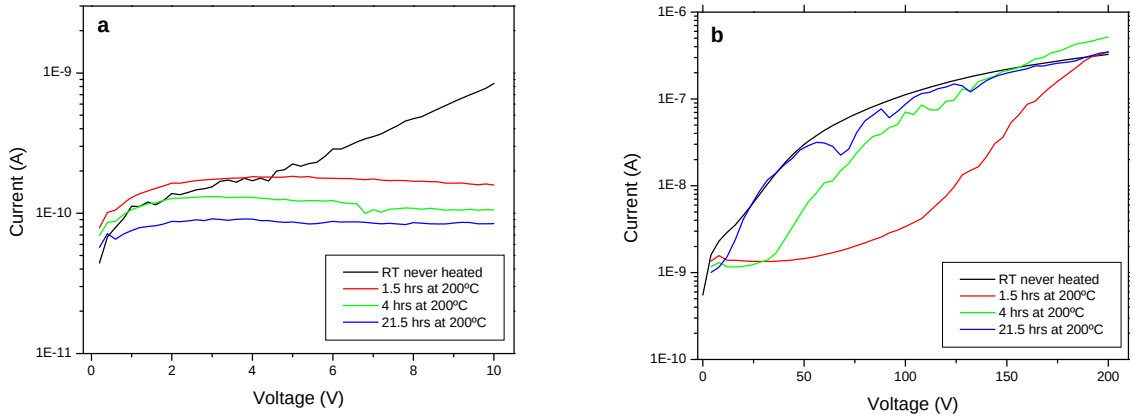


Fig. 16 (a,b). Scanning I-V measurements at 200ºC for the BN capacitor structures tested in Figure 15.

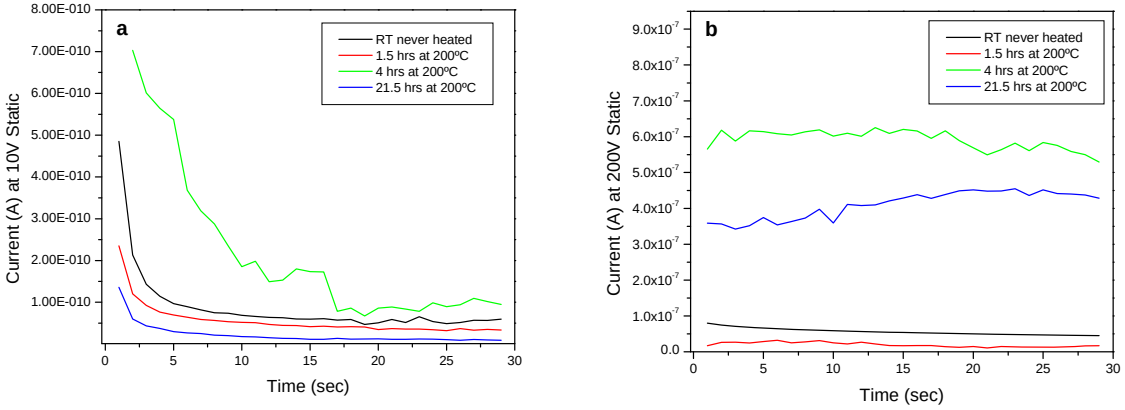


Fig. 17 (a,b). Static I-V measurements at different times held at 200ºC for the devices shown in Fig. 15 and Fig. 16. Longer tests of up to 30 minutes (data not shown) exhibited similar results indicating the stability of the BN capacitor structures at elevated temperatures and voltages.

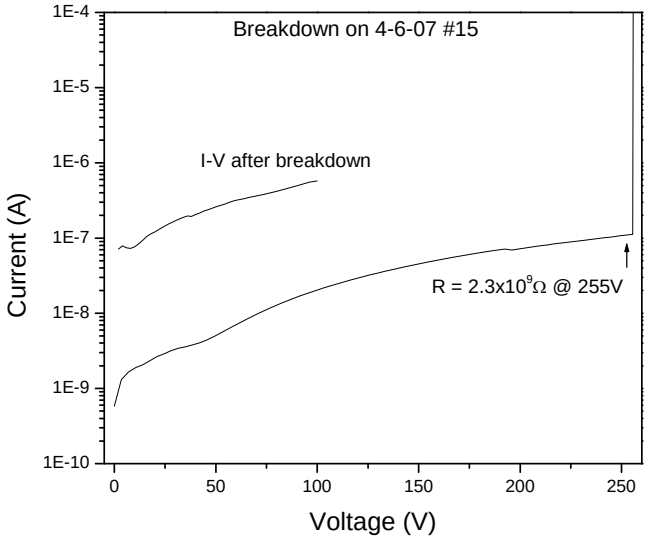


Fig. 18. Room-temperature breakdown measurement for a BN capacitor structure. The value of ~250V is typical of the small number of devices on which we have performed BDV tests.

For the surface mount type capacitors, preliminary I-V data recorded at RT show a low leakage current in the order of 300 to 600 nA at 200 V DC (Fig.19).

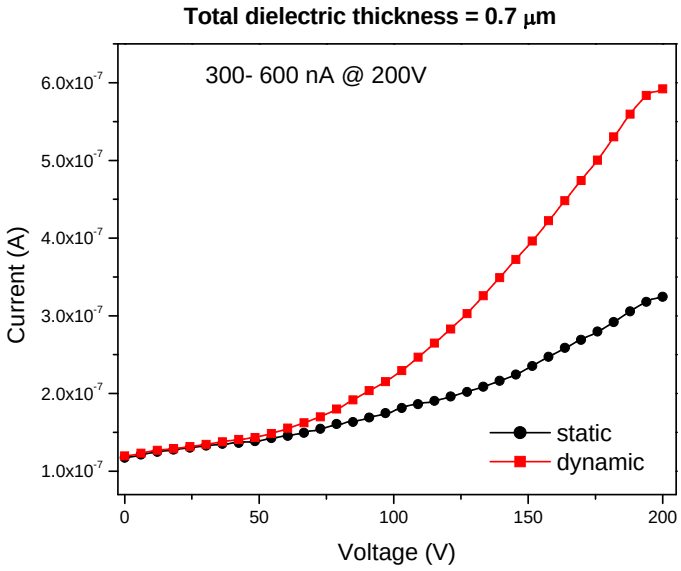


Fig. 19 I-V measurements at RT for 6 x 7 mm size capacitor chip.

4. Capacitance measurements of BN capacitor structures

4.1. Characterization of the wire bonded capacitors:

The fabricated samples had an array of 5 devices each. All of them were wire bonded and capacitance versus frequency measurements were conducted on them. Experiments revealed that samples 2, 4 out of 5 devices were in good working conditions (Fig. 20b) whereas sample 1 showed 2 out of the 5 working devices only (Fig 10a). SEM Images of the devices were taken to assure surface cleanliness prior to wire bonding. Also, the variation of capacitance values with frequency was minimal or almost the same for sample 2 as compared to sample 1. Sample 2 was cleaned with solvents following processing and then wire bonded.

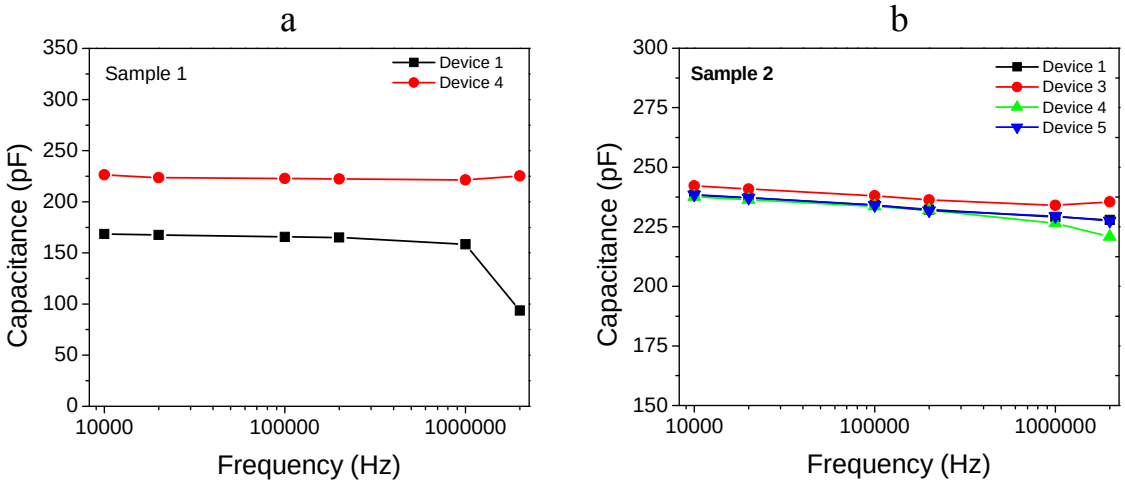


Figure 20. Capacitance versus Frequency plots for devices from Sample 1 and 2

4.2. Characterization of the surface mount capacitors:

Capacitance, quality/dissipation factor, and impedance have been measured for the BN capacitor structures fabricated. Some devices have been measured only as-fabricated, while others have been heated to 200ºC in air and C-I-V measurements performed. Overall, the capacitance of the structures typically varies by less than 5% from 10kHz to 1MHz. Shown in Figure 4 is the capacitance of one device which was tested as-fabricated (Fig. 21a) and then heated in air at 200ºC for 68 hours (Fig. 21b). After an initial decrease over 24 hours, the capacitance becomes very stable over the remaining 44 hours with a decrease of only 1.6%.

At 200ºC, the DC I-V of the samples was also measured. Shown in Figure 22 are the 0-10V scans taken at several time points during the 68 hour anneal. Prior to annealing, the devices exhibit a resistance of ~2.5 GΩ at 10V. During the annealing, the resistance

quickly increases, reaching around 50 GΩ after 68 hours. The resistances have been calculated from the slope of the I-V curves near 10V.

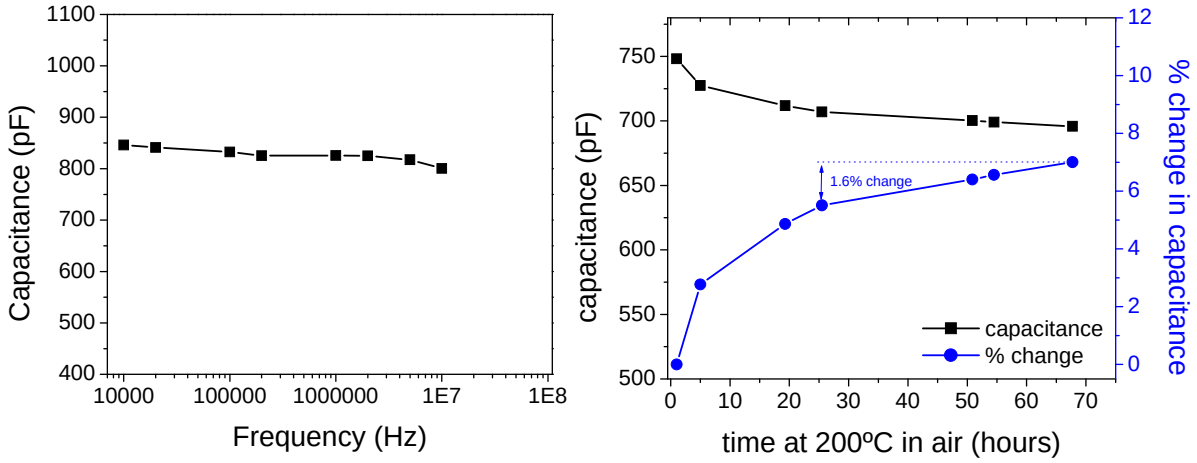


Figure 21. (a) Low and high frequency capacitance of an as-fabricated device. (b) Time dependent low frequency capacitance of a device held for 68 hours at 200ºC that was not burned in. ΔC is ~1.6% between 24 hours and 68 hours.

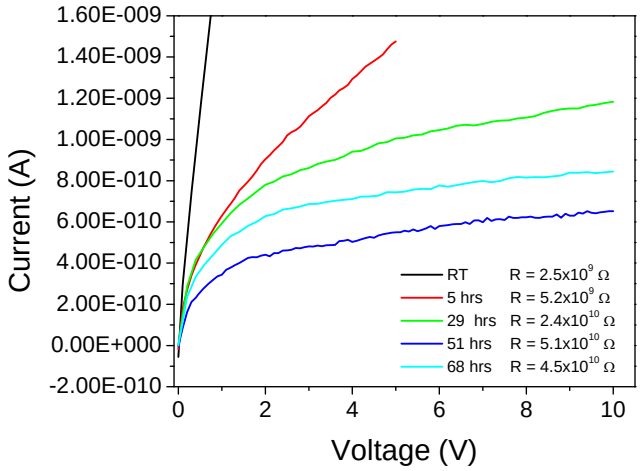


Figure 22. Scanning I-V measurements for BN capacitor structures as a function of temperature during a 68 hour anneal at 200ºC in air.

6.2. Characterization at SEMETROL Facilities (subcontract)

Capacitors that use BN as a dielectric in power converters will benefit from characterizations that clearly point the way to improved and optimized synthesis methods, and also allow predictions of performance. The characterization methods that Semetrol is performing on capacitors developed under this program and that are proven useful are thermal admittance spectroscopy (TAS), current-voltage-temperature (IVT), and photoadmittance.

Samples description:

Ti/Al/Ti/SiO_2/BN/SiO_2/Ti/Al/Ti/Si capacitor structures. BN is 100 nm thick, and the SiO_2 is 380 nm thick. BN-2 was synthesized with higher purity boron.

Sample numbers: BN-1, BN-2

6.2.1. Thermal Admittance Spectroscopy of BN capacitor.

Description:

The samples synthesized using boron of two different purities were characterized using thermal admittance spectroscopy (TAS) in both capacitance and conductance modes (TAS-C, TAS-G). Defects, including native and impurity related defects, introduce disturbances in the periodic lattice potential that can serve to trap charge carriers. The traps are characterized by their energy, capture cross-section, and concentration. The energy and capture cross-section are used to determine the emission rate as:

$$e = \sigma N_c \nu_{th} \exp\left(\frac{-E_T}{kT}\right)$$

where σ is the capture cross section, N_c is the conduction band density of states (or N_v for emission to the valence band), E_T is the trap energy, k is Boltzmann's constant, and T is temperature. At operating frequencies much greater than the emission rate, or low temperatures, the emission rate is slow enough so that trapped charges remain on the defect. However, at higher temperatures, the emission rate may be high enough to follow the switching rate. The effect is to change a square pulse into one that changes with an exponentially decaying time constant, which has an impact on the slew rate. There are several methods that can be used to characterize the trapping centers in BN.

Thermal admittance spectroscopy measures the capacitance and conductance as a function of frequency and temperature. At a fixed temperature, as the frequency of the test signal is reduced, deeper traps are able to respond and contribute to the capacitance and conductance. Similarly, as the temperature increases, the emission rate of a defect increases and the trap can contribute to the measured property. At a threshold in frequency or temperature, the deep level appears as a step in the capacitance, or a peak in the conductance. The temperature of the inflection point of each plot of capacitance versus temperature at a fixed frequency is used along with the frequency, as one point in an Arrhenius plot. The energy of the defects can be obtained from plotting pairs of frequency and temperature points in an Arrhenius plot

of emission rate (frequency of measurement) versus 1/kT. The capacitance and conductance each change with frequency and temperature according to the following expressions:

$$G(\omega,T) = \frac{\omega_t (C_0 - C_\infty)}{1 + \left(\omega_t / \omega\right)^2}$$

$$C(\omega,T) = C_\infty + \frac{C_0 - C_\infty}{1 + \left(\omega / \omega_t\right)^2}$$

where C_0 and C_∞ are the low and high frequency capacitance values, and ω_t is proportional to the emission rate of free carriers from the deep level to a band edge.

$$\omega_t = c_e N_c \exp\left(\frac{-\Delta E}{kT}\right)$$

Here, c_e is the capture coefficient, which is the product of capture cross section and thermal velocity, (σv), ΔE is the activation energy, similar to the previous expression for emission rate. When $\omega_t = \omega$ the capacitance is at an inflection point, and the conductance is at a peak. The temperature of the inflection point or the peak is used along with the frequency of measurement in the Arrhenius plot of $\log(\omega_t)$ versus 1/kT, which has a slope equal to the trap energy, and capture cross section proportional to the y-axis intercept, according to the previous equation. The size of the step change in capacitance can be used as a measure of the trap concentration.

Results:

BN-1:

TAS-C is shown on the left panel of Fig. 23 for a structure grown using the lower purity boron. TAS-G for the same sample is shown on the right. The largest trap is at high temperature, emerging at the lowest frequencies at 300 K, and another lower concentration trap is seen at low temperatures. The measurement temperature was limited to 530K to avoid damaging the capacitor structures. Analysis of the plots revealed that the high temperature step is actually two traps, as shown in Fig. 24, and the Arrhenius plot of Fig. 25. The energies are 0.31 and 0.21 eV. Fig. 24 is the derivative of the conductance TAS data at 3kHz.

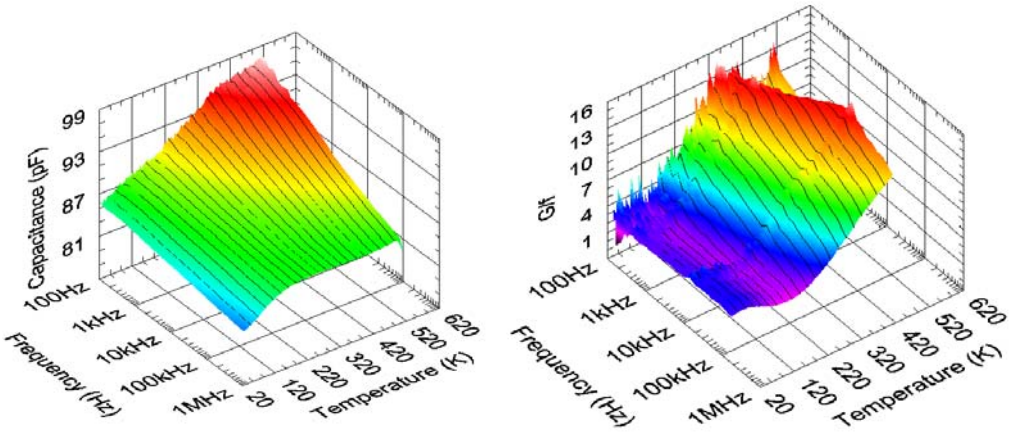


Fig.23. Capacitance and conductance for BN grown with lower purity boron.

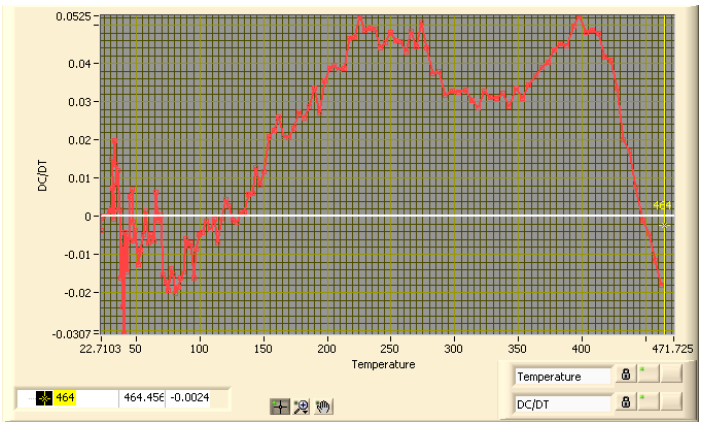


Fig.24. Derivative of the conductance TAS data showing two traps at 250 and 400 K for frequency of 3kHz.

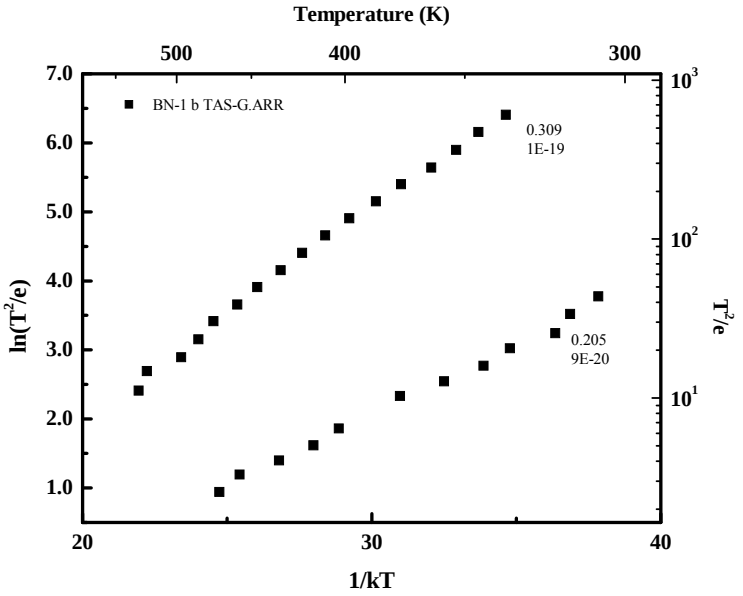


Fig.25. Arrhenius plot of the traps shown if Fig. 23 for the BN synthesized with lower purity boron

BN-2:

The same measurements on the BN synthesized with high purity boron show a pronounced step at low temperature, and a trap emerging at higher temperature (Fig.26). The Arrhenius plots and energies are given in Fig. 27. The low temperature defect has a distribution of

energies from 60-80 meV. Only one defect was detected at high temperature, in contrast to the two traps seen in BN-1. The high temperature trap energy is 0.37 eV.

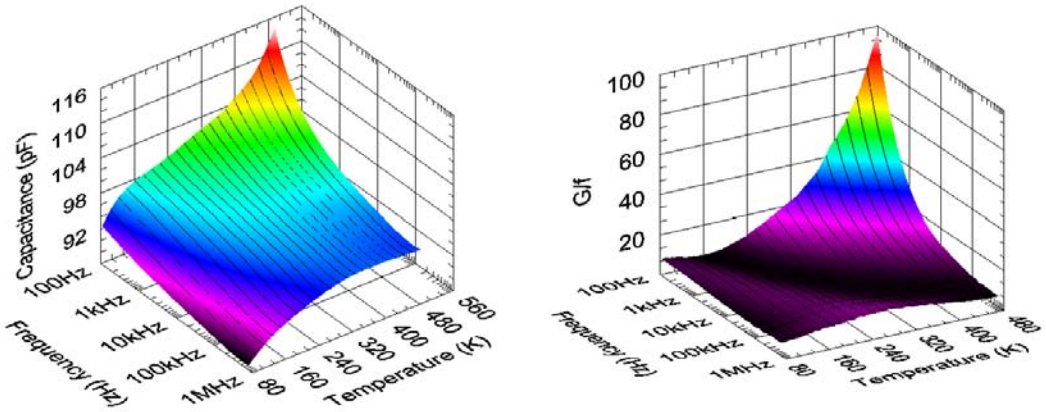


Fig.26. TAS-C (left) and TAS-G (right) for the BN grown with higher purity boron.

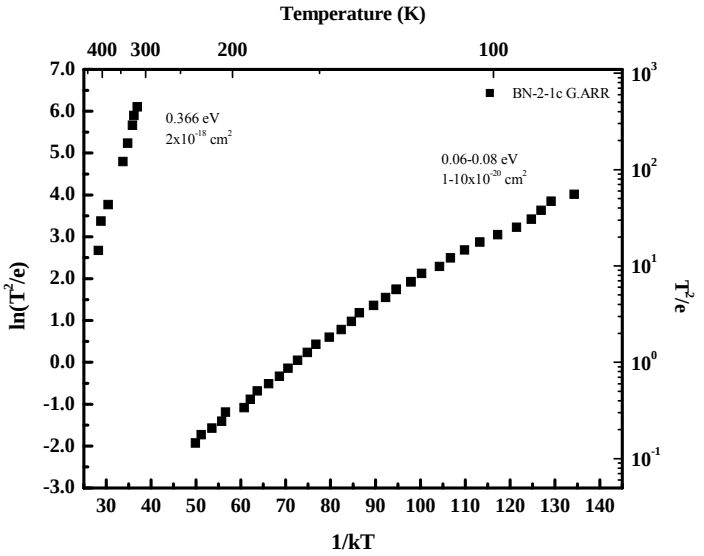


Fig.27. Arrhenius plot of the TAS-G from Fig. 23.

The step in capacitance can be used to obtain the relative density of traps in the two samples. The BN grown with lower purity boron has a change in charge of 3.8%, and the BN grown with higher purity boron changes by only 2.8%.

6.2.2. Current-Voltage-Temperature (IVT):

The energy of the dominant conducting path in each sample was measured by recording the current at several voltages as the temperature was increased. The current at a fixed voltage therefore gives the temperature dependence of the resistance of the material. Plotting ln(I) versus 1/kT at a fixed voltage provides the energy from the slope of the linear region of the plot. The magnitude of the current provides a relative measure of the density of conducting states.

BN-1:
1.3-1.4 eV conduction path energy. Current is 830 pA at 550 K.

BN-2:
0.6 eV conduction path energy. Current is 180 pA at 550 K.

Lower energy conduction path would generally provide higher current, given the same density of conducting states. The lower current for the higher purity BN indicates a much lower density of conducting states, as also seen by the smaller capacitance step in TAS-C. Another possibility may be that the conduction is from band to band rather than via conduction band or valence band states alone. In that case, states closer to mid-gap will provide much greater rate of recombination than states nearer to either band edge. 1.3-1.4 eV is therefore the rate-limiting step in the recombination path for the BN with lower purity. The complementary state, E_g-1.3eV, is a majority carrier trap with higher transition rate due to higher density of majority carriers.

Characterization summary: Two samples of boron nitride (BN) where characterized using thermal admittance spectroscopy (TAS) and current-voltage-temperature (IVT) measurements. The highest density defects in the BN grown with lower purity boron had energies of 0.21 and 0.31 eV. BN grown with high purity boron has a defect with energy of 0.37 eV. A measure of the density of defects with the largest concentration and deepest in energy, was based on the magnitude of the change in capacitance comparing the low frequency capacitance to the capacitance at high frequency. The change in charge is 2.8% for the high purity BN, and 3.8% for the BN grown with lower purity boron. A deeper defect was evident from a step starting to emerge at low frequency at the highest temperatures used. IVT revealed the energy of the dominant conduction paths. The lower purity BN has an energy of 1.3-1.4 eV, compared to 0.6 eV for the higher purity BN. Defects closer to midgap act as efficient recombination centers. The leakage current at 550K is more than four times smaller for the BN grown with higher purity boron.

6.2.3. TAS and IVT characterization of 2nd batch of wire boded capacitors:

Sample description:
Ti/Al/Ti/SiO_x/BN/SiO_x/Ti/Al/Ti/Si capacitor structures. BN is 115 nm thick, and the SiO_x is 360 nm thick. This sample is similar to MC-4, which was characterized in the previous report. In MC-4 the boron was evaporated using a tungsten crucible instead of graphite to avoid carbon contamination.
Sample numbers: Sample 3 (Semetrol #MC0712-03)

Thermal Admittance Spectroscopy:
Thermal Admittance Spectroscopy (TAS) measures the capacitance and conductance as a function of frequency and temperature. As the frequency is decreased, deeper traps will be able to follow the sinusoidal test signal and contribute to the capacitance. The increase

in threshold frequency as the temperature is increased allows the energy of the defect centers to be measured. The magnitude of the increase is a measure of the concentration of traps. The method is described in further detail in a previous report.
The wafer has several identical capacitor structures. The wafer was scribed and cleaved between each row of devices for seven pieces. Three adjacent capacitors and one from the opposite side of the wafer were characterized using IVT and TAS. The measurements were made using a 0.2 V sine wave at frequencies from 100 Hz to 1 MHz, over the temperature range from 35 K to 400 K.

Results: As in the previous sample, the capacitance increases as expected up to about 400K (Fig. 28), at which point the capacitance starts to decrease for many of the capacitors. The previous report shows C(T) at 100kHz. Fig. 29 is at 10 kHz, which shifts the features up in temperature. #1, 2 and 3 are adjacent. Capacitor #1 is from the edge of the wafer and has much higher capacitance than the other three. Capacitor #6 is from the opposite side of the wafer, and has a larger low temperature step, indicating a higher concentration of traps, and smaller relative step at high temperature.

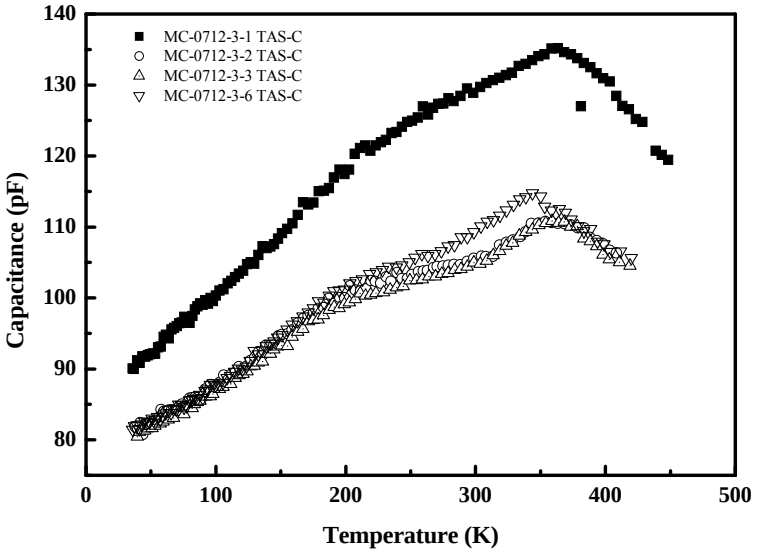


Figure 28. Comparison of thermal admittance spectroscopy data for four capacitors from sample #3 (MC-0712-3).

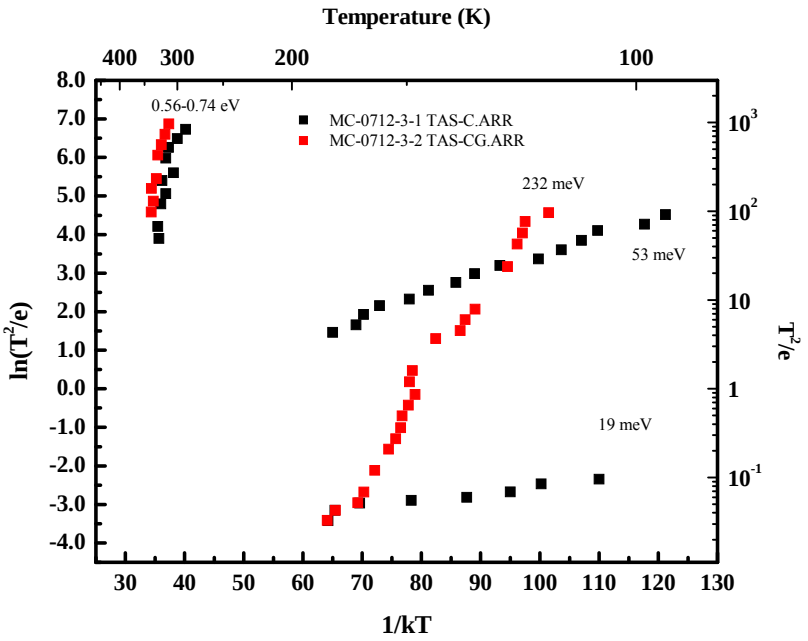


Figure 19. Arrhenius plot of TAS-C data for sample MC-0712-3 capacitors #1 and #2. The other two capacitors have energies similar to capacitor #2.

The size of the step in the capacitance versus frequency is used to determine the concentration of traps. Two ranges were used corresponding to the two steps in Fig. 1. For comparison purposes, the change in capacitance is taken from 40 K to 180 K, and 180 K to 360 K, measured at 100 Hz.

Plotting the threshold frequency, normalized for temperature (T^2 factor), versus 1/kT has a slope equal to the energy of the trap (Figure 1). Capacitors 2, 3, and 6 have similar energies. Capacitor #1 did not show the trap at 0.23-0.27 eV, but has two lower energy traps in the same temperature range. The energy of the high temperature trap (0.56-0.74 eV) is an estimate only, since the capacitance starts to decrease at temperatures where the trap is measurable. Table I is a summary of the trap properties.

Table 1. Energy and concentration of capacitors from sample MC-0712-3 from thermal admittance spectroscopy measurements.

Sample #	40-180K Temp. (K)	E_T (eV)	σ (cm^2)	40-180K Conc. Change	180-360K Temp. (K)	E_T (eV)	σ (cm^2)	180-360K Conc. Change
MC-0712-3-1	132	0.02	2.70E-20	0.4177	315	0.56	1.40E-15	0.335
	130	0.053	1.90E-21					
MC-0712-3-2	134	0.232	3.40E-14	0.3148	322	0.743	2.90E-13	0.3456
MC-0712-3-3	146	0.264	4.50E-14	0.3365	302	0.608	2.40E-14	0.3664
MC-0712-3-6	152	0.274	3.10E-13	0.3476	276	0.682	3.00E-12	0.3987

The uniformity, based on the standard deviation of the concentration change of three of the four capacitors, is 1.7% for the concentration of the low energy trap and 2.7%

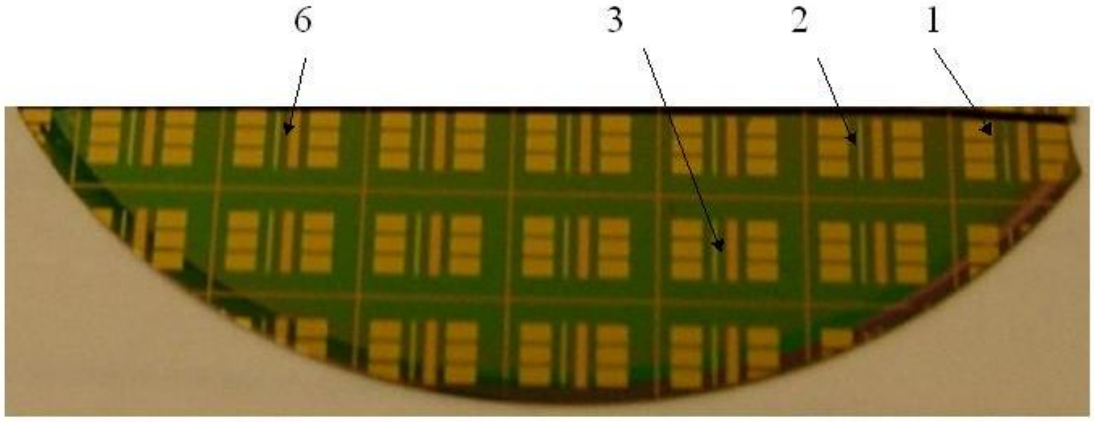
for the higher energy trap. Uniformity including the edge of the wafer is not as good, increasing the respective standard deviation of trap concentrations to 4.5% and 2.8%.

6.2.4. Current-Voltage-Temperature (IVT):

The energy of the dominant conducting path in each sample was measured by recording the current at several voltages as the temperature was increased. The current at a fixed voltage therefore gives the temperature dependence of the resistance of the material. Plotting ln(I) versus 1/kT at a fixed voltage provides the energy from the slope of the linear region of the plot. The magnitude of the current provides a relative measure of the density of conducting states.
Results: The IVT measurements also show which of the traps provide the leakage path for current. As in previous IVT measurements, two energies were found, one at 0.2 eV and one at 0.6-0.7 eV. Table 2 summarizes the dynamic resistance and leakage current at 400 K. Capacitor #1, from the edge of the sample, has higher resistance by a factor of 3-4, and lower leakage current.

Table 2. Resistance and leakage current at 400K for each of the four capacitors.

Sample	Dynamic resistance (8-10V) (GΩ)	Leakage current at 10V (nAmps)
1	14.7	0.56
2	3.2	2.5
3	4.4	1.9
6	5.3	1.4



Characterization summary: Four capacitor structures were characterized from one sample using thermal admittance spectroscopy (TAS) for density and energy of trapping centers, and current-voltage-temperature (IVT) measurements for the energy of the

dominant leakage path and relative magnitude of leakage current for comparison between capacitors. This characterization gives an indication of how much variation there is across a wafer. Two energies were found using either method: 0.2 eV and 0.6-0.7 eV. A capacitor from the edge of the wafer has significantly higher concentration of the trap at low energy, and lower concentration of the higher energy trap. It also has lower leakage currents. The leakage current near room temperature has an activation energy of 0.6-0.7 eV. The other capacitors have the same trend; lower concentration of the high energy trap results in lower leakage currents and higher dynamic resistance. The standard deviation in trap concentration of the high energy trap is 2.8% for the four capacitors.

ADDENDUM: FOLLOW-UP WORK AFTER PHASE II COMPLETION

Fabrication and characterization of BNO capacitors:

The growth of the BON thin films was carried out in the same vacuum chamber that was used for BN based capacitors. Nitrous oxide N_2O is used as the feed gas to the ion source and solid boron is sublimated using an electron beam. The nitrous oxide flux is 3-4 sccm. The base pressure of the chamber is 10^{-8} torr .The pressure during growth is 10^{-5} torr and the wafer temperature is maintained at 600°C during the growth. 2" silicon wafer was used as the substrate. The wafer is degreased with solvents (Trichloroethylene, Acetone and Methanol) and then etched with HF (1:10) to remove any native oxide. It is then loaded into the growth chamber and then preheated at 950^0C for 1-2 minutes. The as-grown films were analyzed with SEM, XRD and XPS. For capacitor fabrication, Titanium is used as metal for both the top and the bottom electrodes. In this study, we have investigated some material properties of the film namely, the elemental composition of the film, surface morphology and crystallinity and additionally the device properties of a capacitor structure were also studied. The Surface morphology by SEM is smooth, continuous and devoid of any pinholes as compared to BN film taken at the same magnification level. Fig.30 b. shows the presence of pinholes in BN films.

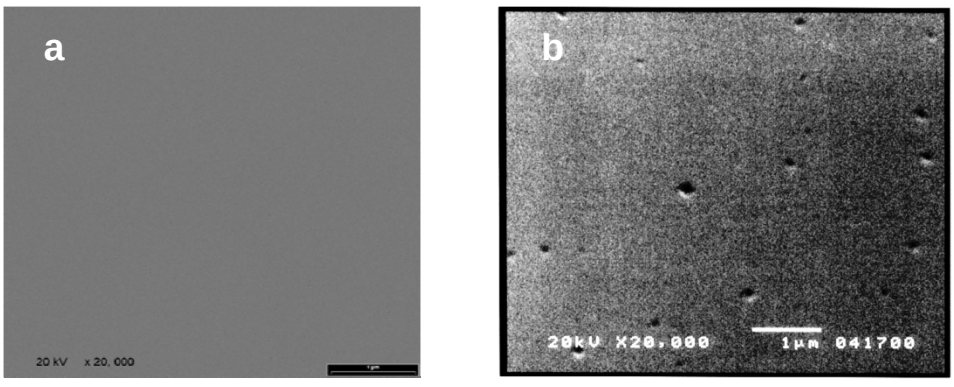


Fig.30. SEM micrograph of a) Boron oxynitride, b) Boron

XRD analysis was performed to find the degree of crystallinity in the BON film. The XRD plot is shown in Fig.31b. Apart from the signals for silicon and titanium, a peak at 29.5^0 [1] can be seen and corresponds to BON compound. Although the peak is present, its intensity is very small and weak. There are other broad and very weak peaks present from 35^0-39^0. Our results suggest that the film is amorphous with a very little crystalline content. **The formation of an amorphous film is easier than formation of a polycrystalline film because of the uniform stoichiometry required for a polycrystalline film. Also, by having amorphous gate dielectrics, which have dense microstructures allows us to avoid many of the problems associated with grain boundaries in polycrystalline dielectrics**.

XPS studies were performed to analyze the elemental and chemical composition of the film. To trim our efforts and expenses, a graded sample with alternate layers of metal (spacer layer) and dielectric (BON layer) was made. The BON layer was grown at different temperatures (500^0C, 550^0C and 600^0C) and the metal (Titanium) was deposited at room temperature. The top layer was duplicated to check deposition reproducibility. The metal layers were 10nm thick. Figures 32a,b show the typical structure and XPS depth profile of the sample.

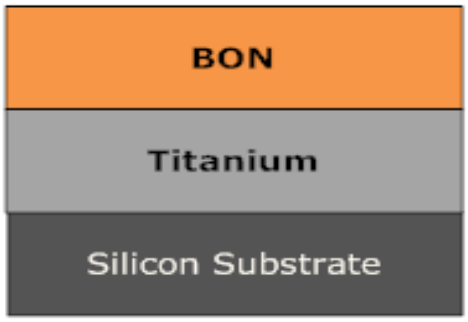


Fig 31a: Sample structure subjected to XRD Analysis

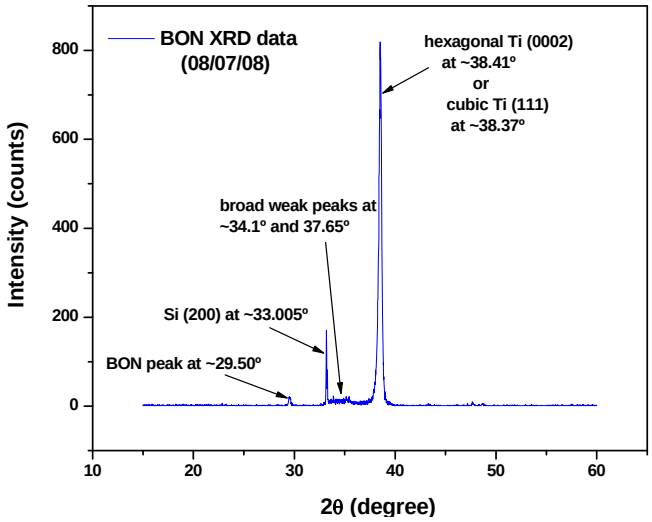


Fig 31b: XRD plot of the analyzed

Fig 32a: Graded Sample for XPS Analysis

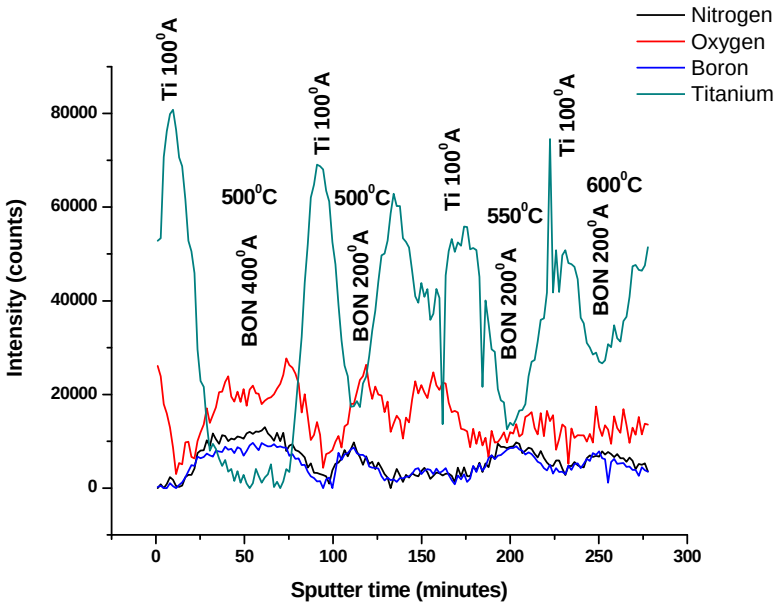


Fig 32b: XPS Depth Profile of the graded sample

From Fig.33c and also from Table 3, it is clear that there is little variation in the oxygen and nitrogen 1s peaks at the different growth temperatures.

B1s on the other hand shows peaks at 188.3eV, 190.3eV and 192.5eV. The peak at 188eV corresponds to the B1s peak of metallic boron (supported by XPS analysis of pure B sample). The peak at 190.4eV confirms the presence of BN [2,3]. Pure boron oxide (B_2O_3) peak is at 193.7eV [3]. The peak at 192.5eV is in the intermediate range of pure BN and pure B_2O_3 [4]. It also falls within the binding range B1s (191eV-193eV) as reported by Chen *et al*.[5]. The binding energies of the elements (boron, nitrogen and oxygen) were measured and are presented in Fig.33 c,d. The graphical results are also tabulated for a better understanding.

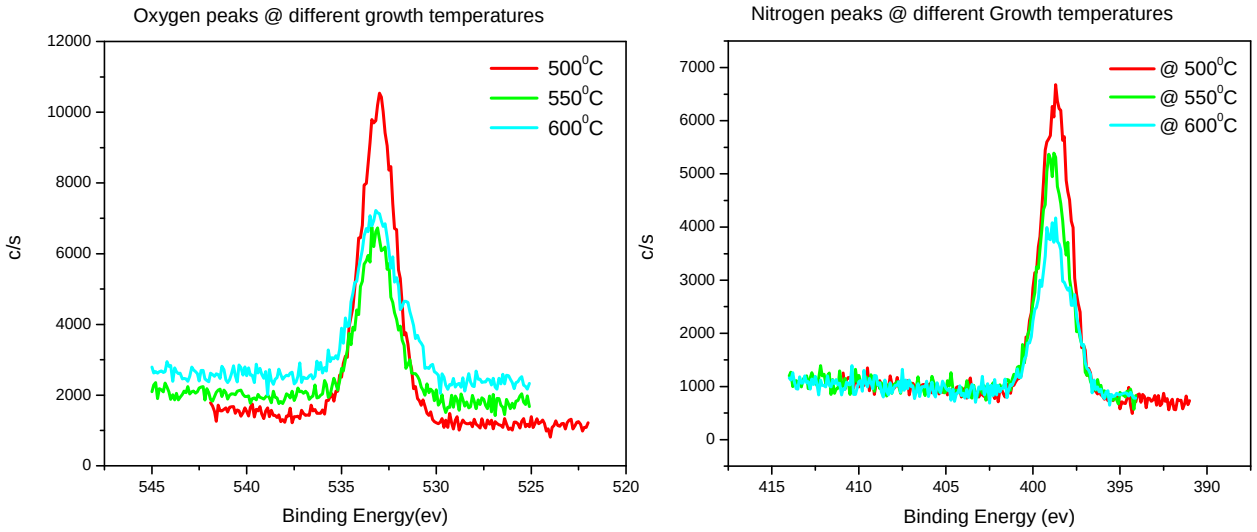


Fig 33c: High Resolution XPS Spectra of O1s and N1s

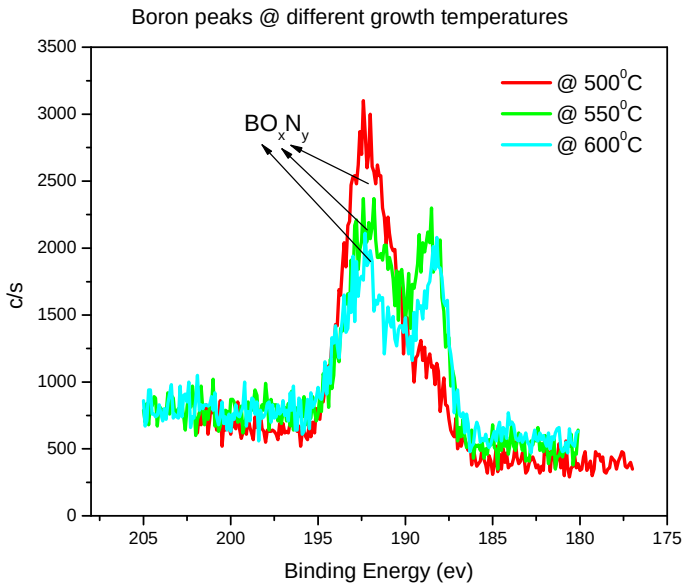


Table 3

	500°C	550°C	600°C
Boron	189.2	188.46	188.31
	192.1	190.4	190.31
		192.42	192.52
Nitrogen	398.4	398.82	398.77
Oxygen	532.92	533.14	533.04

Fig 33d: High Resolution XPS spectra of B1s

The chemical composition of each layer was analyzed and is shown on Table.4. The film stoichiometry at different temperatures is also shown on Table 5.

Table 4

Temperature of Growth	Boron	Nitrogen	Oxygen	Titanium
500^{0}C	52.13	22.57	24.96	0.33
550^{0}C	56.54	19.88	17.61	5.95
600^{0}C	49.88	17.54	21.21	11.35

Table 5

Temperature of Growth	Composition
500^{0}C	$B_{0.52}$ $N_{0.23}$ $O_{0.25}$
550^{0}C	$B_{0.6}$ $N_{0.21}$ $O_{0.18}$
600^{0}C	$B_{0.56}$ $N_{0.2}$ $O_{0.24}$

Prototype capacitors with boron oxynitride as dielectric have been fabricated. Preliminary results (Fig.34 and Fig.35) indicate a very small variation (~3%) of capacitance over a range of frequencies (10 KHz – 2 MHz). The measured capacitance values from different spots at 10 KHz were about 0.2 nF. This is for a typical 200 nm thick $B_{1.0}O_{0.5}N_{0.5}$ layer and an area of 1 mm^2 for the 100 nm thick Ti electrode. The variation in capacitance over a range of temperatures 25°C - 400°C is about 13% for a 300 nm thick $B_{1.0}O_{0.5}N_{0.5}$ layer with similar footprint and metal electrodes. **The dielectric constant (permittivity) of the BON thin films is found to be 5.5 – 8 as compared to 3.9 of SiO_2.** The associated loss is found to be smaller when compared to Boron Nitride of equivalent physical thickness and exhibit good linearity in terms of electrode area.

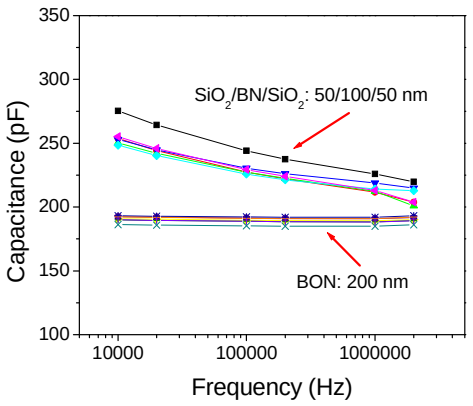


Fig.34. Capacitance obtained on BN with diffusion barriers and BON of equivalent thickness. Colors denote different spots on 2" ∅ Si wafer

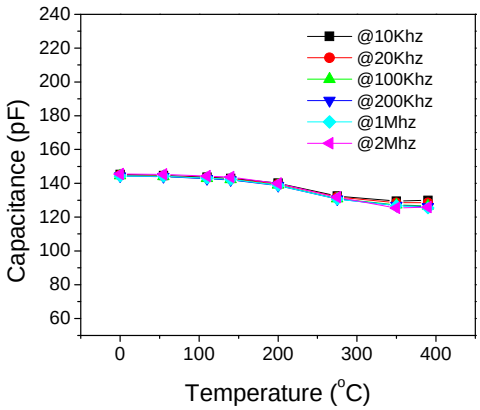


Fig.35. Variation in capacitance of BON capacitor as a function of temperature

Boron Oxynitride has effectively eliminated the need for a diffusion barrier and has proved to be self-sustaining at high temperatures.

CONCLUSION

We believe that IMS is clearly in the path of developing a capacitor technology with a broad operating temperature range to support the USDOE effort in advanced SiC power electronics and other commercial applications. We are at the stage of making prototype capacitors and perform additional testing in order to reach the anticipated level of effort to move the technology to the market place. This could be achieved under a Phase III SBIR Program we would like to pursue. With dedicated equipment and available funds IMS should be able to scale up the process to larger foot print, preferably on flexible substrate, to mirror the commercialized sintered technology but with the additional and necessary high temperature performance and thus increase the capacitance values to the scale of tens to hundreds of microfarads. This will allow IMS to meet the need of a wider spectrum of end-users.

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Appendix A

Topic Number: DOE-04-29a

Subtopic Summary:

Advanced Power Electronics Component Materials—Over the past 10 years, advanced silicon power chips have revolutionized power conversion with the use of new power semi-conductor devices such as Integrated Gate Bi-Polar Transistors (IGBTs). Although these devices continue to improve in performance and power handling capability, there exist alternative materials that could revolutionize the performance of power electronic components. Materials such as gallium-arsenide, diamond, and, in particular, silicon-carbide (SiC) offer potentially outstanding properties for power conversion: large band-gap, high breakdown field, good thermal conductivity, and a high saturation velocity. In addition, SiC has high elastic modulus and toughness, and SiC devices can operate at temperatures up to 600^{o}C. Grant applications are sought to develop technology to further the use of these materials in improved power electronics devices. Areas of interest include: overcoming micro-pipe defects in SiC wafers (i.e., small tubular voids that run through the wafers in a direction normal to the polished wafer surface), innovative thermal management, advanced bonding and soldering techniques that can withstand higher temperatures, incorporating long-life capacitors in advanced SiC components, insulated metal substrates, elimination of wire bonds, automated manufacturing, and innovative packaging.