Fermi National Accelerator Laboratory

D-Zero Central Fiber Tracker

AFEII
Analog Front End Board

Design Specification

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Based on AFEI specs by
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1. GENERAL INFORMATION

This document describes the design of the 2nd iteration of the Analog Front End Board (AFEII), which has the function of receiving charge signals from the Central Fiber Tracker (CFT) and providing digital hit pattern and charge amplitude information from those charge signals. This second iteration is intended to address limitations of the current AFE (referred to as AFEI in this document). These limitations become increasingly deleterious to the performance of the Central Fiber Tracker as instantaneous luminosity increases. The limitations are inherent in the design of the key front end chips on the AFEI board (the SVXIIe and the SIFT) and the architecture of the board itself. The key limitations of the AFEI are:

- SVX saturation
- Discriminator to analog readout cross talk
- Tick to tick pedestal variation
- Channel to channel pedestal variation

The new version of the AFE board, AFEII, addresses these limitations by use of a new chip, the TriP-t and by architectural changes, while retaining the well understood and desirable features of the AFEI board.

1.1. System Introduction

The CFT system consists of a set of 8 concentric cylinders of optical fiber arranged in layers. Each of these layers has 'axial' fibers, that is, those which run parallel to the beam direction; there are also 'stereo' fibers, which wrap in gentle helices around the beam line. Half of the 'stereo' fibers have a clockwise twist, and the other half have a counter-clockwise twist, such that data from a correlated clockwise and counter-clockwise pair of hits indicates a distance from the interaction point along the beam axis. Two boards are installed into a mechanical 'cassette', which views a total of 1024 fibers. The mechanical design of the cassette requires that the two boards be on opposite sides; part height clearances require that both boards face 'away' from the centerline of the cassette. This has resulted in the concept of 'right-handed' and 'left-handed' boards, indicative of the direction in which the components protrude away from the cassette centerline when viewed from the front. Analysis of the AFE board design has resulted in the realization that a single 'non-handed' design – that is, a single layout which can be used in both orientations- is possible, so long as certain minor restrictions in the fiber placement at the top of the cassette are observed.

Each successive layer of fibers from innermost ('A') to outermost ('H') has more fibers than the last; in addition, there are two preshower detectors, the Central Preshower ('CPS') fibers are positioned outside the H layer, and a Forward Preshower detector which covers regions of high rapidity. Preshower fibers are imbedded in scintillator strips so there are relatively few PS fibers, but these produce significantly more light and impose different requirements on the electronics. The TriP-t and in fact the AFEII are designed to meet the requirements of the fiber tracker and the preshower detectors.

The CFT is subdivided into 80 sector of 4.5deg each. Each sector of the CFT/CPS consists of 480 'axial' fibers and an additional 480 'stereo' fibers. Each sector contains

- 32 ‘A’ layer fibers
- 40 ‘B’ layer fibers
- 48 ‘C’ layer fibers
- 56 ‘D’ layer fibers
- 64 ‘E’ layer fibers
- 72 ‘F’ layer fibers
- 80 ‘G’ layer fibers
- 88 ‘H’ layer fibers
- And projects to an additional 32 ‘CPS’ layer fibers

Only the ‘axial’ fibers are used in trigger formation, so all ‘axial’ fibers are routed into one set of AFE boards and all ‘stereo’ fibers are routed into different AFE boards. The Preshower is handled separately so there are 480 axial fibers per sector required to form the trigger. The arrangement is shown in Figure 1.

Note that in figure 1, some 30 boards are marked with an asterisk (*). This indicates that these 30 boards are called out twice in the diagram because they handle fibers from two different sections of the detector. The actual board total is 76 + 32 + 60 + 30 = 198 boards.

For further details of the detector arrangement, please check the DZero RunII NIM paper.

All channels of analog data seen by the AFE boards pass through discriminators. Each discriminator creates one bit of data per input channel, creating a bitmap of fibers whose charge was above threshold. This pattern is sent to trigger system every crossing of the beam (every 396 nsec) by high-speed serial data links. There is a single Digital Front End (DFE) for every pair of AFE boards used in track finding. These Digital Boards take the bit pattern of which fibers were above or below threshold to find potential particle tracks. To obtain sufficient bandwidth, each AFE board must drive four digital links to a given DFE.

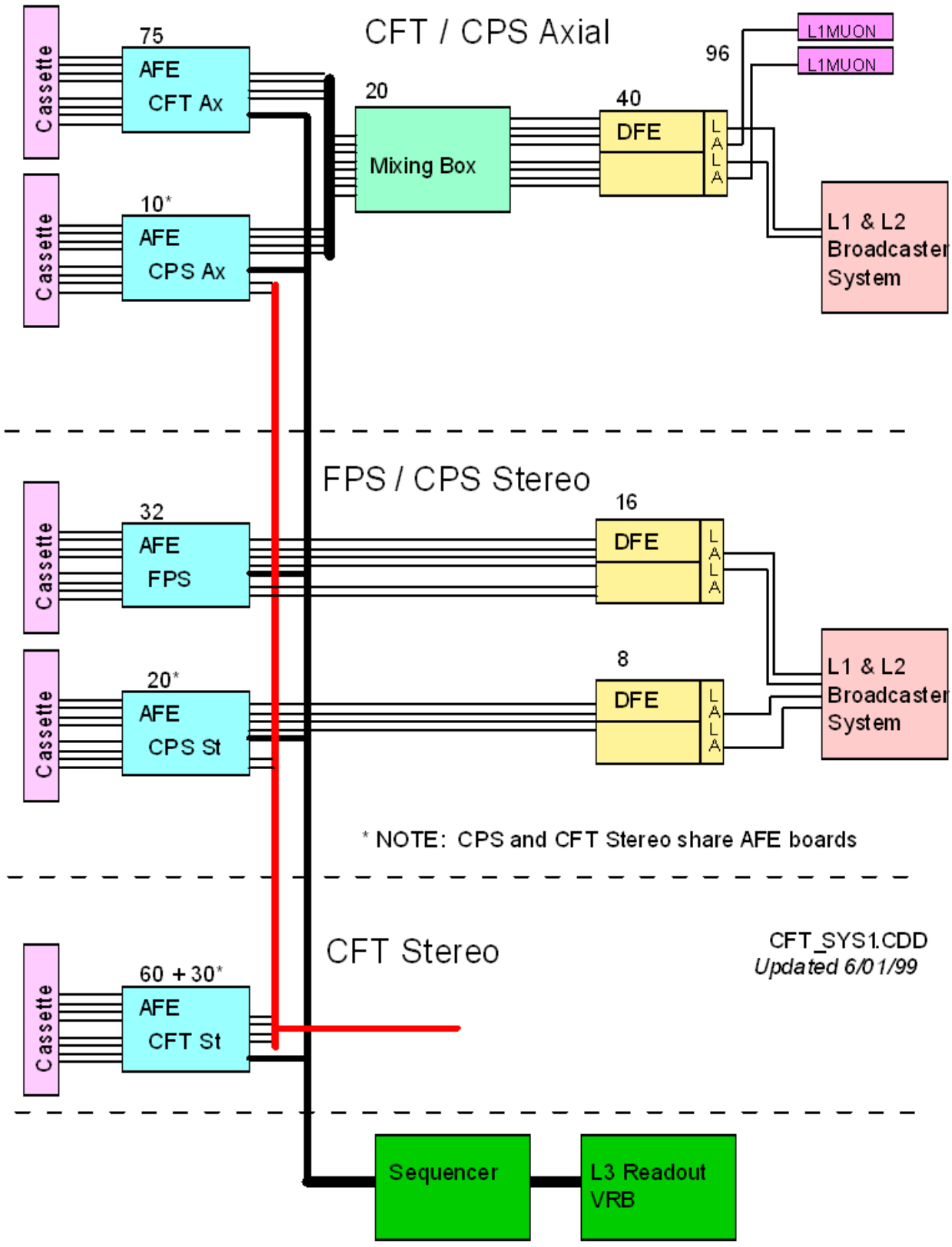
CFT / CPS Axial
Cassette
75
AFE
CFT Ax
Cassette
10*
AFE
CPS Ax
20
Mixing Box
40
DFE
LALA
96
L1MUON
L1MUON
L1 & L2
Broadcaster
System
FPS / CPS Stereo
Cassette
32
AFE
FPS
16
DFE
LALA
Cassette
20*
AFE
CPS St
8
DFE
LALA
L1 & L2
Broadcaster
System
* NOTE: CPS and CFT Stereo share AFE boards
CFT Stereo
CFT_SYS1.CDD
Updated 6/01/99
Cassette
60 + 30*
AFE
CFT St
Sequencer
L3 Readout
VRB

Figure 1

1.2. Description of AFEII & How It Fits Into the System

The AFE board is a 10 layer printed circuit board which is 9U (14.435 inches) high and 19.25 inches deep. Each AFE slides into guide rails on a mechanical cassette which houses the cryogenic photodetectors (VLPCs). As the AFE is installed into the cassette, it plugs into a backplane from which it derives power and control connections.

The cassette is a complex mechanical assembly. One AFE is mounted on each side of the cassette. Each AFE has its components on the outside, so the AFE boards must be either left or right handed so that it may be plugged into either side of the cassette. The VLPCs require operation at cryogenic temperatures, so relatively long and specially designed cables bring the low-level analog signals from the bottom of the cassette (held at about 9 Kelvin) to the room-temperature AFE. A set of flexible printed circuits connected to the AFE along the bottom edge deliver the analog input signals.

1.3. List of Component Requirements

- Mirror-image left to right board design
- Mechanically compliant with cassette design
- Must accept 512 low-level charge signal inputs
- Must discriminate all 512 channels every 396 nsec
- Must deliver digital result of all 512 channels to DFE boards and/or Mixer System within 132 nsec via multiple high-speed LVDS links
- Pass SCL control information to the DFE/Mixer boards.
- Relatively low power (less than 50 Watts) due to limited airflow
- Controlled by MIL-STD 1553 interface
- Able to provide test pattern data in lieu of real data for readout to the trigger or offline
- Interfaces to SVX Sequencers for readout of analog information upon receipt of trigger signal from L1 system.
- Buffers all discriminator data for redundant readout of discriminator pattern to Level 3 system.
- Able to act as closed-loop temperature controller for VLPCs
- Provides appropriate bias voltage for VLPCs

2. THEORY OF OPERATION AND OPERATING MODES

2.1. Basic Features & Operation

The AFEII is very similar in overall design to the AFEI and contains a number of subsystems. Figure 2 gives the overview. The essential subsystems are as follows:

- Interface to MIL-STD 1553 (RT1553)
- The PIC microprocessor (and HELPER FPGA)
- A clock generation system to develop all required timing
- An interface to the SVX Sequencers, including the Virtual SVX (VSVX) - an FPGA which reformats the data for compatibility with the current SVX Sequencers
- High speed data multiplexing system which takes all discriminator data and sends it via LVDS links to the DFE/Mixer system.
- Eight modules or slices (for historical reasons referred to as MCMs) that perform discrimination and digitization of the analog signals.
- Analog monitoring and control for the VLPC temperature and bias.

2.2. MCM

The heart of the AFEII are eight identical slices or MCMs (Multi-Chip Modules) which each contain two TriP-t chips, two AD9201 ADCs, two Xilinx Spartan2 XC2S100 FPGAs and some associated power supply and filtering circuits. Each MCM services 64 channels of charge input. More detailed description of the analog inputs and the TriP-t are given below in 2.2.1 and 2.2.2. Every beam crossing, the TriP-t provides one bit of discriminator output per channel, where a '1' indicates that the charge was above a predetermined threshold. The charge collected by each channel is also stored in a 48 deep switched-capacitor array for possible readout at a later time. In addition, the discriminator output is connected to a simple time to amplitude converter (TAC) which outputs an analog voltage which is proportional to the time between the start of a beam crossing and the firing of the discriminator. This voltage is also stored in an analog pipeline for possible readout. Level 1 Trigger signal initiates a readout of a particular row of the analog pipeline providing amplitude and time information for the event.

The discriminator outputs are routed to one of the FPGAs (DFPGA for digital or discriminator FPGA) where the bits are serialized and send to the DFE/Mixer system via LVDS links (described in more detail in section 2.7 below). These bits are also stored in memory, for readout during after a trigger was received. This information can then be used to check the functioning of the CTT.

Analog signals are digitized (there are two dual channel AD9201 ADCs in each slice) and the analog information (which corresponds to the amplitude and time of the hits) is digitally processed to remove pedestal variation and apply zero suppression in the AFPGA (analog FPGA) and readout through the sequencer interface. This is described in more detail in section 2.5. A block level diagram of the MCM is shown in Figure 3.

2.2.1. Analog input

The analog inputs of the AFEII are AC coupled and biased to about 8V. The coupling capacitor is a 1nF and uses high frequency NP0 dielectric. Each Trip-t handles 32 channels plus two "dummy" channels. The inputs are small charge pluses, typically from a few fC to a few hundred fC. The input capacitance as seen by the front end is about 35pF. Typical discriminator thresholds are as low as 10fC. This corresponds to a voltage of about 300 micro Volts at the TriP-t input.

2.2.2. TriP-t

The TriP-t is the fully custom, mixed signal ASIC that is at the heart of the AFEII board. It is the design and architecture of this chip that overcomes the limitations of the AFEI. More detailed documentation may be found in the "Bench Tests of TriP-t Report", D0Note-xxxx. The majority of the circuitry on the AFEII board merely provides support of the operation, configuration and readout of TriP-t. The requirements for the TriP-t are listed in Appendix A. It has two basic functions: is required to give a prompt (within a 100ns or so) discriminator output which is used in the formation of the Level1 trigger, and on demand, timing and amplitude information about all hits which occurred during an earlier event. Internally, the Trip-t chip is composed of a number of functional blocks

- Preamp on every channel which integrates the charge to a voltage
- A discriminator on every channel. A simple current source charging a capacitor which can be interrupted by the firing of the discriminator, thus giving an analog voltage which is proportional to the time the discriminator fired. The output of the discriminator is also connected to the clock input of a flip-flop, which latches if the discriminator fired
- A pipeline composed of switch capacitor arrays. There are two caps per channel per time slice. One capacitor stores the analog information from the preamp, the other, the timing information from the discriminator timing circuit. This pipeline has a depth of 48 time slices.
- A discriminator mux which outputs, in turn the lower and upper 16 discriminator channels. This is required to keep the number of pins on the TriP-t down.
- An analog mux which can cycle through every channel for analog readout. There are two analog outputs on the chip- one gives the amplitude of the channel, the other a voltage proportional to the time the discriminator fired.
- A serial programming interface which controls a number of internal DACs and some digital parameters. The DACs control bias currents and voltages (for example the threshold voltage of the discriminator). The digital parameters control such things as the delay setting of the pipeline, the gain of the preamp and other internal amps.
- Test injection circuitry. This allows an external voltage pulse to be differentiated across a small 200pF capacitor and injected into any channel. The choice of which channels to inject is set through the programming interface.

2.3. MIL-STD 1553 Interface

The MIL-STD 1553 serial link is used as the main control connection to the AFE board. Each AFE has its own Remote Terminal (RT) interface which is implemented in a Spartan2 FPGA. The AFEII implementation of the control system is fully compatible with the original AFE. Two subaddresses, decimal 16 and 17 (0x10 and 0x11) act as an address pointer and a data port. A few locations in the RAM are reserved as a 'command queue' which is loaded by the 1553 controller with eight-bit command values. The queue is filled with commands and, when the list is ready, a terminal value is written to a special flag address which causes the on-board microprocessor to execute the list. The rest of the RAM is allocated to status information and command parameters. All RAM locations are available to the 1553 interface, which may interrogate them at any time. An important difference in the AFEII relative to the AFEI is that RAM used for the 1553 RT is internal to the FPGA. There are no external memory chips. The 1553 interface of the AFEII is compatible with the VME-to-1553 interface used throughout DZero, originally designed by the Accelerator Division Controls group. A detailed document describing the memory map of the AFEII from the point of view of the 1553 interface is in preparation. It is based on Engineering note A1000612 by John Anderson.

2.4. PIC microprocessor and HELPER

A Microchip PIC 18F452 microcontroller is used on the AFE. This is a high performance 8bit RISC cpu with linear program memory addressing 32K bytes of FLASH and 1.5K bytes of onboard RAM. This is an important difference from the microprocessor used on the AFEI which required complicated "banking" to access a sufficient amount of program memory. The microprocessor provides supervisory and diagnostic control functions in the AFEII but is not directly involved with the high-speed data acquisition functionality. The basic jobs handled by the microprocessor are the following:

- Poll the dual-port RAM and respond to commands from the 1553 bus;
- Load analog control voltages to the DAC subsystem over the I^2C bus;
- Perform read back of ADC voltages, board temperature, board power supply voltages and cryostat temperature over the I^2C bus;
- Act as local closed-loop PI temperature controller for the VLPC chips.

The microprocessor firmware is coded entirely in assembly language and is programmed on board via the Microchip ICD (in circuit programmer and debugger). Remote downloads of firmware are not supported.

A 'helper' FPGA demultiplexes the microprocessor I/O lines and provides the necessary support to address the many different chips on the board. Each FPGA on the board has 2 strobes: and "instruction" strobe and a "data" strobe. By using these two strobes in combination with the single data bus, complete communications with the FPGA is possible. The microprocessor clock is derived from the on-board 1553 interface clock, so that the micro will run even if the AFE is disconnected from the rest of the fiber tracker system. A detailed document describing the memory map and command structure of the PIC is in preparation. It is based on Engineering note A1000612 by John Anderson.

2.5. SVX Sequencer Interface

The SVX Sequencer was designed (as its name implies) to initialization, control and readout the SVX IIe chips. Since the SVXIIe chips are absent from the AFEII, the Sequencer is in some sense obsolete in the case of the AFEII. However, since the sequencer provides the readout path for data to Level 3, the AFEII is required to interface to it. A ribbon cable connection (often referred to as the grey cable) from the SVX Sequencer to the AFE was used to provide the bidirectional data bus, required control signals and clocks to the AFEI. Most of this functionality is not required for the AFEII. One cable actually contains two SVX control buses, and the backplane splits the signals such that each SVX cable services two adjacent AFE boards. Each SVX bus connection provides the following signals:

- 8-bit bidirectional SVX data bus. However, on the AFEII this bus is used only from the AFE to the Sequencer, allowing better termination
- DVALID signal driven from AFE to SVX Sequencer. This simply becomes one of the bits of the SVX data bus.
- Differential SVX Clock. This is not used by the AFEII
- Differential Crossing Clock. This is used to generated ALL the clocks on the AFEII
- CHANGE_MODE, MODE0 and MODE1 control lines to SVX. These lines are used to signal to the AFEII when to switch between initialization mode and acquire mode. They also indicate when the Sequencer is ready to accept data from the AFEII.
- FIRST_CROSSING, SYNC_GAP, L1ACCEPT and CFT_RESET control signals

Most of the control functionality of the Sequencer is obsolete for the AFEII, except that the signals listed in the last line above must be passed on to the DFE system and are used to synchronize the AFEII with beam collisions. Also, since the master timing of the AFE board is derived from the crossing clock as supplied on this cable, for the board to work this link must be present and at least the crossing clock must be present. The SVX Sequencer was designed by Mike Utes and documentation for this module may be found at

http://d0server1.fnal.gov/users/utes/default.htm

Recent studies indicate that there is a significant amount of cross talk in the grey cable between D1 (second bit of the 8bit data on the bus) and the DVALID signal (which is used to clock the data into the FIFO on the Sequencer). This crosstalk has been identified a major cause of the current readout rate limitation for the AFEI. Design goal was 53 Mhz, currently operating at 40 Mhz. In order to fix this problem, a change in the assignment of the signals to conductors of the grey cable has been proposed. This is transparent from the point of view of the AFEII, because DVALID and D0..D7 are symmetrical – treated identically and easily reassigned inside the FPGA that generates them.

2.6. Analog Monitoring and Control

To achieve optimal performance, VLPCs require operation at a stable temperature and must have a stable, accurate bias. A carbon resistor is used to sense the temperature of the VLPCs. The value of this resistor is approximately 300 ohms at the normal operating temperature of about 9 Kelvin. This resistor is excited using a constant current source generated by a pair of op-amps and a voltage reference in every MCM. The voltage drop developed across this resistor is measured using an instrumentation amplifier (using a 4-wire topology) and this voltage is sensed by the A/D converter. The temperature of the VLPCs is kept constant using the microcontroller as a digital loop controller (PI) to command a DAC which drives a power op-amp to drive a heater resistor near the VLPCs. The cryostat is operated in such a way that by slightly varying the power in the heater resistor, the VLPCs are kept in a very narrow range of temperature (within 40 mK of set point). A bias voltage is also required for the VLPCs themselves, and this is driven by an op-amp from a DAC output. The voltage applied to the VLPCs is brought back to the ADC, as is a measurement of the current being drawn by the VLPCs. Although the analog monitoring system for the AFEII is nearly identical to the one used on the AFEI, there are some notable improvements:

- The AFEII uses a higher accuracy ADC, giving an effective resolution of about 13 bits, as opposed to 11 bits effective resolution of the AFEI
- The AFEII uses precision voltage references where a known voltage is required (such as for the reference of the DACs and the current sources) as opposed to using the output of a LDO regulator (with an accuracy of about 2%) making these circuits more precise and stable.
- The AFEII carries three precision resistors on board, connected with simple jumpers, which allow the temperature measurement circuitry to be checked and calibrated without the use of a special calibration test stand, as was required for the AFEI. If this jumper is inadvertently left on when the AFEII board is inserted into the detector, the readback of temperature will give an unphysical value which will cause the heaters to shut down – a fail safe feature.

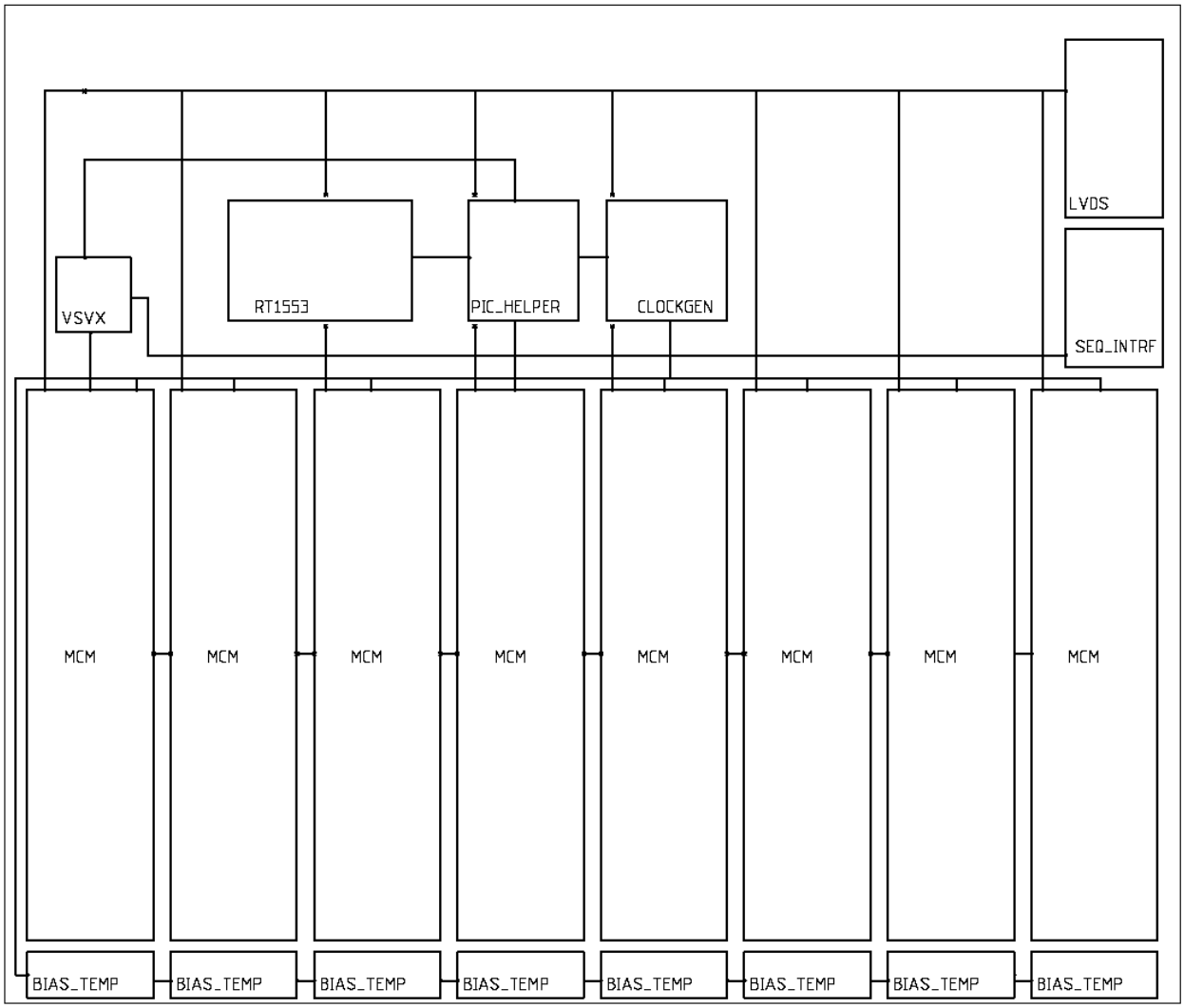

Figure 2: A block diagram of the AFEII showing the major functional subsystems.

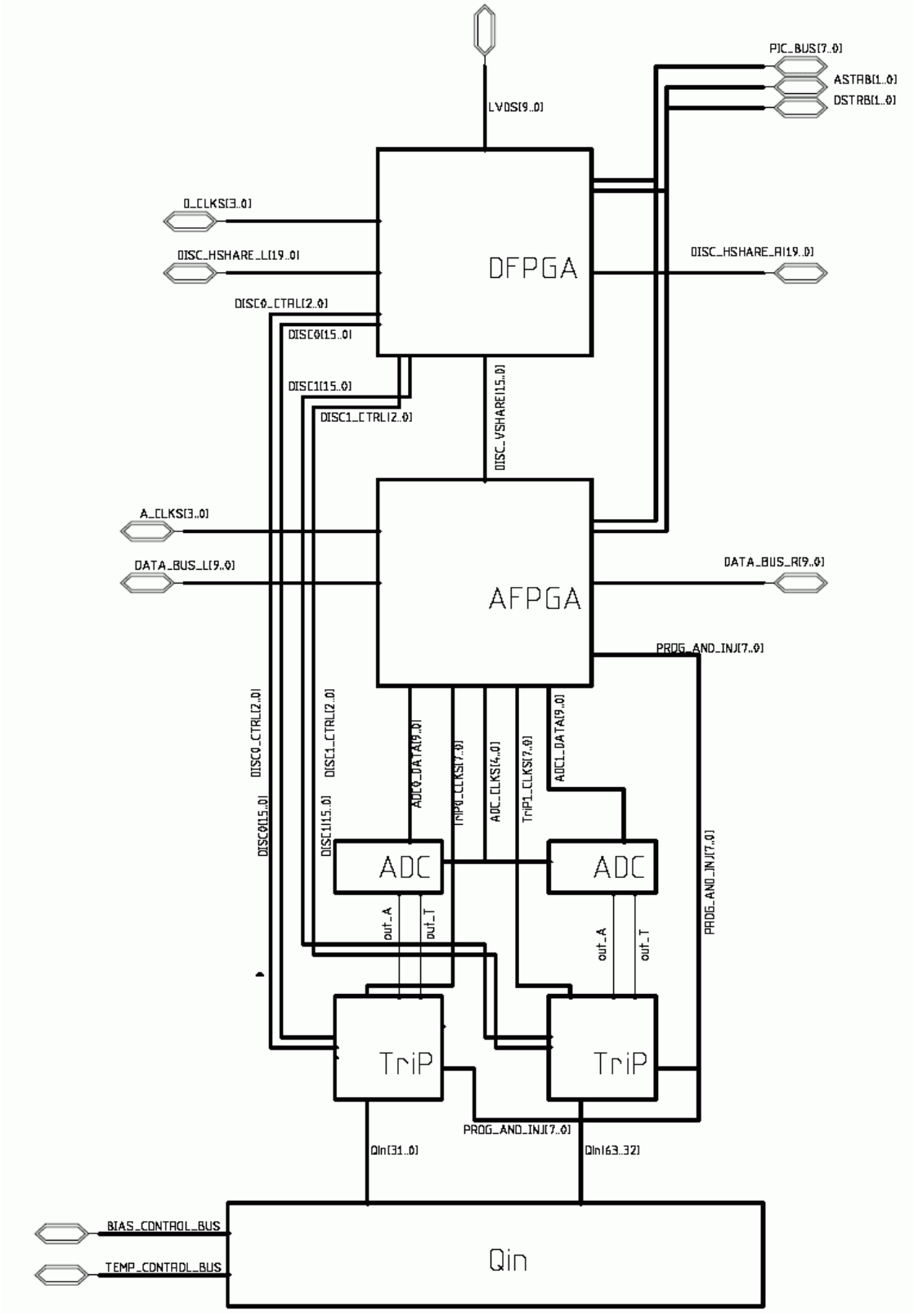

Figure 3: A block diagram of one slice or MCM.

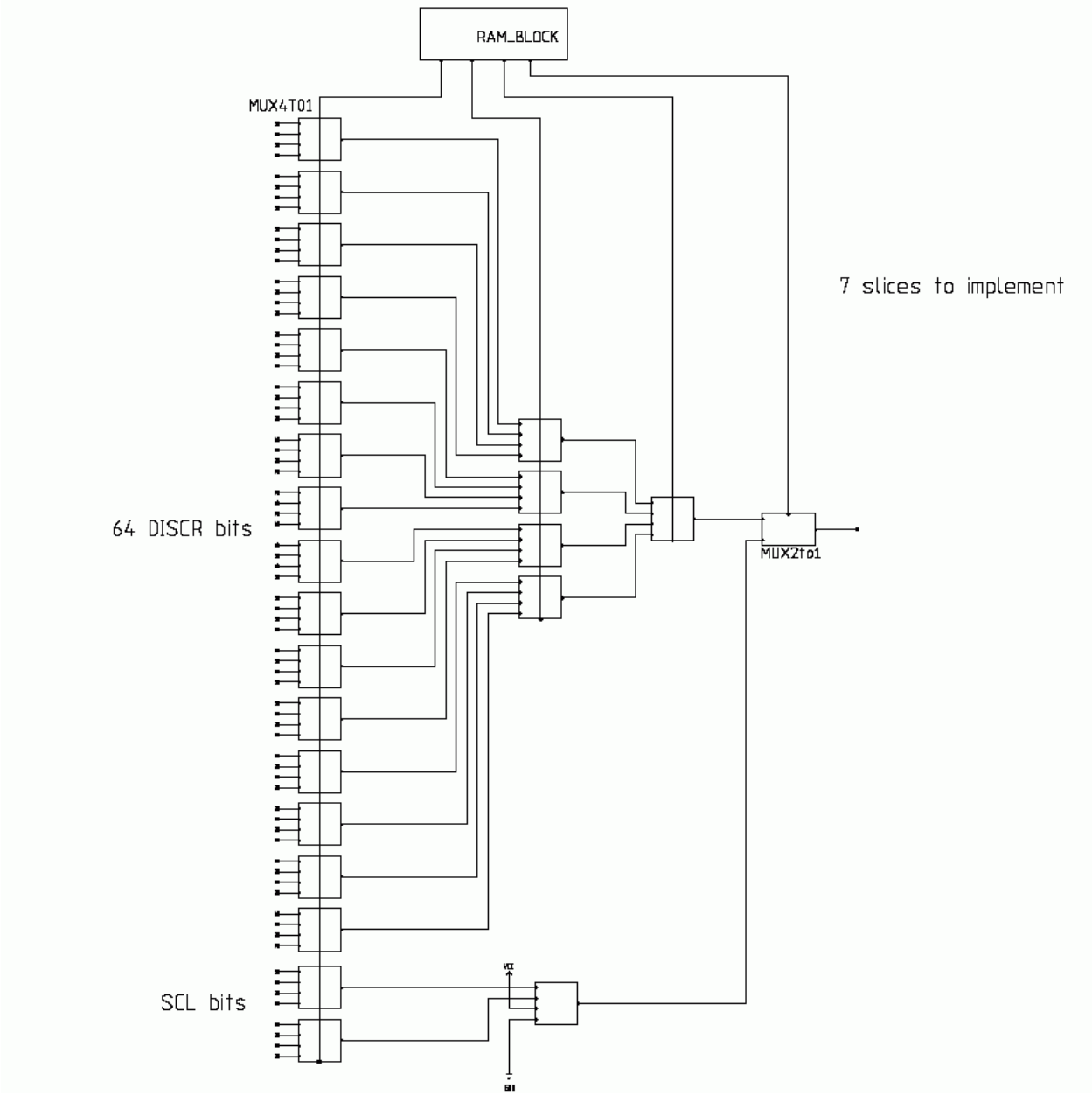

Figure 4: Schematic diagram of LVDS mux structure for one LVDS output bit. The DFPGA contains ten such blocks plus other logic.

2.7. Data Multiplexing and Serial Links

The 512 bits of discriminator data obtained every crossing must be transmitted a few feet to the DFE system. Obviously, a massively parallel cable would be most impractical. To accomplish this transfer, a dual serialization scheme is employed. At each of the eight MCMs an FPGA (called DFPGA for digital or discriminator) takes the 64 bits of data and, using the 53 MHZ clock, creates seven 10-bit words every 132 nsec. The extra six bits are filled with SCL and diagnostic information. On the AFEI this is done by a Lattice CPLD which is programmed to output groups of 10 bits in seven consecutive time slices. The details of the architecture are not important- the important point is that once the CPLD is configured, the routing of the bits is fixed and cannot be changed except by reprogramming the chip. In the FPGA this same functionality is achieved by using a 70:1 mux, with the select lines driven by internal RAM of the FPGA for each of the ten bits. This structure is then repeated 10 times to give the 10-bit words for transmission to the DFEs. The logic necessary to implement one of the ten multiplexers described is shown in Figure 4. It should be noted that this logic represents 0.8% of the logic resources available in this FPGA. This type of structure means the AFEII board is capable of:

- Being programmed over 1553 for ANY output pattern including fake tracks, or any arbitrary pattern.
- It is guaranteed that there is NO pattern which cannot be "routed" inside the FPGA.
- To keep the efficiency of the trigger high, fibers which are known dead can be treated as fired by the trigger. This architecture can accommodate the "turning on" of a dead fiber while the board is in the detector. The architecture of the AFEI requires that new firmware is created and downloaded to the appropriate board during an access.

The eight 10-bit buses from the eight DFPGAs are combined in pairs to form four 20-bit buses. Each 20-bit bus is connected to an LVDS driver part which internally multiplies the 53 MHz clock by another factor of seven. The driver part takes a 21-bit input at 53 MHZ and sends it out as three data bits (plus a sync clock) at a rate of about 371 MHZ. Thus, each 128 bits of MCM data are transmitted over four differential pairs at this 371 MHZ rate. Four of these high-speed serial links are then capable of transmitting all 512 bits of MCM data, plus 48 bits of status information, every 132 nsec.

The 21st bit of each link is connected to the 7.6 MHz crossing clock so that the receiver of the four links may check synchronization between the links. This is the frame marker bit and allows the DFE system to align the LVDS links properly in time.

2.8. Clock Generation

The AFE board must synchronize to the 7.6 MHz beam crossing clock as provided by the SVX Sequencer boards in order to correctly acquire the data from beam collisions. However, for readout and for internal processing a much faster clock is required. A two tier system which takes advantage of the clock multiplier feature present in the Xilinx FPGA is used: a phase-locked loop is used to multiply the beam crossing clock by 7 to generate 53.104 MHz, the RF clock frequency of the Tevatron. This works because the crossing clock itself is derived by dividing the Tevatron RF clock by 7. As a second tier, we use the DLL present in the Xilinx FPGAs to multiply the clock by 2 again, to allow time sensitive processes to run at 106.208 Mhz. To conserve power, blocks which are not time critical operate at 53.104 Mhz.

AFEII design

The AFEII uses the ispPAC 5510V PLL from Lattice to generate the 53 Mhz clock. This device has 10 differential clock outputs which allows a single line pair to drive the clock to each slice or MCM as well as one to the VSVX subsystem and one to the HELPER. This was simply not possible at the time the AFEI was designed as there were no 10 output PLLs available. Furthermore, this chip allows a fine adjustment of the skew of each clock line independently which means that the clock to each module can be tuned to compensate for differences in the length of the traces allowing for technically sound synchronous design despite the large physical size of the AFEII board. In addition, this chip also boasts adjustable source termination for each output, making it possible to provide the AFEII with a nearly ideal clock distribution scheme.

INTERFACE SPECIFICATIONS

The AFE board talks to the world through its connection to the AFE Backplane. This backplane provides power, connection to the SVX Sequencer, LVDS output and connection to MIL-STD 1553. Inputs to the board are through flex cables that connect at the bottom edge.

2.9. MIL-STD 1553 Interface

This interface has been previously discussed. The MIL-STD 1553 interface is a serial protocol carried on two wires, at a bit rate of approximately one bit per microsecond. Manchester encoding is utilized and decoded via a standard interface chip. An FPGA acts as the serdes and dual-port RAM.

2.9.1. Addressing Modes

The AFE responds only to subaddresses 0x10 and 0x11. Only normal data cycles (no broadcasts) are supported.

2.9.2. Register Descriptions

Subaddress 0x10 is an address pointer register which selects the address of the dual-port RAM which will be read or written by the first access to subaddress 0x11. The dual-port ram has an address range of 0x0000 – 0x1FFF. Any data written to bits 15, 14 or 13 of subaddress 0x10 will be ignored. Having written to subaddress 0x10, reads or writes to subaddress 0x11 access successive locations in the dual-ported memory. The RAM address loaded by the write to subaddress 0x10 is incremented with each data word read or written to subaddress 0x11, such that a 5-word read from subaddress 0x11 after writing a value of 0x100 to subaddress 0x10 would result in the data from RAM locations 0x100, 0x101, 0x102, 0x103 and 0x104 being supplied. Since the 1553 spec allows for up to 32 words of transmission per access to a given subaddress, a single access to subaddress 0x11 may transfer up to 32 words to the RAM.

2.10. SVX Sequencer Bus Interface

The SVX Sequencer communicates with the AFE through a ribbon cable which lands on the AFE Backplane. One cable actually contains two SVX control buses, and the backplane splits the signals such that each SVX cable services two adjacent AFE boards. Each SVX bus connection provides the following signals (this information is a duplicate of what is contained in Sec 2.5 but is reproduced here for ease of reference):

- 8-bit bidirectional SVX data bus. However, on the AFEII this bus is used only from the AFE to the Sequencer, allowing better termination
- DVALID signal driven from AFE to SVX Sequencer. This simply becomes one of the bits of the SVX data bus.
- Differential SVX Clock. This is not used by the AFEII
- Differential Crossing Clock. This is used to generated ALL the clocks on the AFEII
- CHANGE_MODE, MODE0 and MODE1 control lines to SVX. These lines are used to signal to the AFEII when to switch between initialization mode and acquire mode. They also indicate when the Sequencer is ready to accept data from the AFEII.
- FIRST_CROSSING, SYNC_GAP, L1ACCEPT and CFT_RESET control signals

The SVX Sequencer was designed to control the operation of the SVX IIe chips and to provide the readout path for SVX IIe chips. Most of the control functionality is obsolete, except that the signals listed in the last line above must be passed on to the DFE system and are used to synchronize the AFEII with beam collisions. Also, since the master timing of the AFE board is derived from the crossing clock as supplied on this cable, for the board to work this link must be present and at least the crossing clock must be present.

2.11. Front Panel I/O, Test & Monitoring

The AFE has no front panel due to mechanical constraints. Because of the AFE's left-right symmetric design, an AFE inserted on either side of the mechanical cassette will have a pad pattern for an unstuffed backplane connector at the 'front'. Various surface mount LEDs will be visible when the board is installed but none are specifically mounted on the board edge.

2.12. Rear Connector Interface

All AFE I/O occurs through the rear connector, to the backplane. The AFE connects to the backplane using two metric connectors from the series used for Compact PCI (e.g. AMP Z-Pack and/or equivalents from ERNI, FCI, etc.). One connector is a type 'A' which integrates 110 pins of connection with mechanical alignment features to insure the connector is aligned prior to pin mating. The other connector is a type 'B' which forfeits the alignment piece to provide 125 pins. Both connectors utilize top side shields which are used as extra ground returns.

2.12.1. Connector Pin Configurations

Table 1 shows the pinout for the AFE Backplane, for the Right-Handed insertion of the AFE board. The pinout for the Left-Hand insertion is, of course, swapped left-to-right. Different colors are used to highlight different groups of pins. The green pins are all grounds. The analog and digital ground planes of the AFE are tied together to the common backplane ground. The grey pins were reserved for use in the 12-MCM version of the AFE which was never built.

	F (Top Shield)	E	D	C	B	A	Z (Bottom Shld)
1	GND	5.5V	+3.3V	GND	1553-	1553+	GND(BP)
2	GND	5.5V	+3.3V	GND	SLOTBIT1	SLOTBIT2	GND(BP)
3	GND	5.5V	+3.3V	GND	SLOTBIT8	SLOTBIT3	GND(BP)
4	GND	+3.3V	+3.3V	GND	SLOTBIT7	SLOTBIT4	GND(BP)
5	GND	GND	GND	GND	SLOTBIT6	SLOTBIT5	GND(BP)
6	GND	LVDS1_D1+	LVDS1_D1-	GND	LVDS1_D2+	LVDS1_D2-	GND(BP)
7	GND	LVDS1_D0-	LVDS1_D0+	GND	LVDS1_CLK+	LVDS1_CLK-	GND(BP)
8	GND	GND	GND	GND	LVDS1_D3+	LVDS1_D3-	GND(BP)
9	GND	LVDS2_D1+	LVDS2_D1-	GND	LVDS2_D2+	LVDS2_D2-	GND(BP)
10	GND	LVDS2_D0-	LVDS2_D0+	GND	LVDS2_CLK+	LVDS2_CLK-	GND(BP)
11	GND	GND	GND	GND	LVDS2_D3+	LVDS2_D3-	GND(BP)
12	GND	LVDS3_D1+	LVDS3_D1-	GND	LVDS3_D2+	LVDS3_D2-	GND(BP)
13	GND	LVDS3_D0-	LVDS3_D0+	GND	LVDS3_CLK+	LVDS3_CLK-	GND(BP)
14	GND	GND	GND	GND	LVDS3_D3+	LVDS3_D3-	GND(BP)
15	GND	LVDS4_D1+	LVDS4_D1-	GND	LVDS4_D2+	LVDS4_D2-	GND(BP)
16	GND	LVDS4_D0-	LVDS4_D0+	GND	LVDS4_CLK+	LVDS4_CLK-	GND(BP)
17	GND	GND	GND	GND	LVDS4_D3+	LVDS4_D3-	GND(BP)
18	GND	LVDS5_D1+	LVDS5_D1-	GND	LVDS5_D2+	LVDS5_D2-	GND(BP)
19	GND	LVDS5_D0-	LVDS5_D0+	GND	LVDS5_CLK+	LVDS5_CLK-	GND(BP)
20	GND	GND	GND	GND	LVDS5_D3+	LVDS5_D3-	GND(BP)
21	GND	LVDS6_D1+	LVDS6_D1-	GND	LVDS6_D2+	LVDS6_D2-	GND(BP)
22	GND	LVDS6_D0-	LVDS6_D0+	GND	LVDS6_CLK+	LVDS6_CLK-	GND(BP)
23	GND	GND	GND	GND	LVDS6_D3+	LVDS6_D3-	GND(BP)
24	GND	GND	GND	GND	GND	GND	GND(BP)
25	GND	+12V	+12V	GND	-12V	-12V	GND(BP)
1	GND	DVALID B	GND	SYNC_GAP	GND	CROSSING*	GND(BP)
2	GND	GND	1st XING	GND	CROSSING	GND	GND(BP)
3	GND	SVX_DAT0B	GND	VCAL B	GND	PRIORITY_OUTB	GND(BP)
4	GND	GND	DIR B	GND	SVX_DAT2B	GND	GND(BP)
5	GND	SVX_DAT5B	GND	HDI_EN B	GND	SVX_DAT1B	GND(BP)
6	GND	GND	SVX_DAT3B	GND	SVX_DAT6B	GND	GND(BP)
7	GND	MODE1 B	GND	SVX_DAT7B	GND	SVX_DAT4B	GND(BP)
8	GND	GND	PRIORITY_INB	GND	CLK* B	GND	GND(BP)
9	GND	CFT_RESET	L1 ACCEPT	CLK B	GND	MODE0 B	GND(BP)
10	GND	CLAMP	GND	SPARE	CHG_MODE B	GND	GND(BP)
11	GND	+5V	+5V	+5V	+5V	+5V	GND(BP)
12							
13				KEY AREA			
14							
15	GND	DVALID B	GND	SYNC_GAP	GND	CROSSING*	GND(BP)
16	GND	GND	1st XING	GND	CROSSING	GND	GND(BP)
17	GND	SVX_DAT0B	GND	VCAL B	GND	PRIORITY_OUTB	GND(BP)
18	GND	GND	DIR B	GND	SVX_DAT2B	GND	GND(BP)
19	GND	SVX_DAT5B	GND	HDI_EN B	GND	SVX_DAT1B	GND(BP)
20	GND	GND	SVX_DAT3B	GND	SVX_DAT6B	GND	GND(BP)
21	GND	MODE1 B	GND	SVX_DAT7B	GND	SVX_DAT4B	GND(BP)
22	GND	GND	PRIORITY_INB	GND	CLK* B	GND	GND(BP)
23	GND	CFT_RESET	L1 ACCEPT	CLK B	GND	MODE0 B	GND(BP)
24	GND	CLAMP	GND	SPARE	CHG_MODE B	GND	GND(BP)
25	GND	+5V	+5V	+5V	+5V	+5V	GND(BP)

Table 1

2.12.2. Signal Descriptions

The various LVDS +/- signals are 370 MHz, Low-Voltage Differential Signaling standard, differential current source signals. They drive differential transmission lines and expect to see a termination equal to the characteristic impedance (typically 100 ohms) across the pair at the receiving end. The SLOTBIT signals are either left floating or tied to GND in order to give each AFE board a unique address for purposes of 1553 communication. The bits are a combination of slot position and a backplane address such that every AFE in the Central Fiber Tracker has a unique 1553 RT address. All SVX signals are TTL level signals.

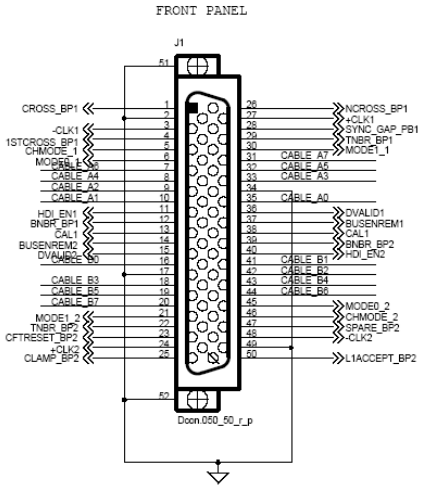

Figure 5: SVX Sequencer connector

3. ELECTRICAL & MECHANICAL SPECIFICATIONS

3.1. Packaging & Physical Size

The AFE is 14.435 inches high by 19.25 inches wide. It is a bare circuit board with no front panel. Components are mounted on both sides. Due to mechanical restrictions, component height above the board may be no more than 0.431" on the component side and no more than 0.050" on the solder side. Ten layer FR4 construction is used. Some gold plating is on the component side where the flex cables land. Build to IPC Class3 standard. Board will have handles attached to the front for use in mounting on the cryostat.

3.2. Power Requirements

The AFEI measurements indicate a power consumption of about 46 Watts split between +5V, +3.3V, and ± 12V. By using local power regulation at each FPGA and TriP-t chip, the AFEII guarantees minimal sensitivity to supply voltage fluctuations. The estimate for the AFEII indicates that it will dissipate about the same amount of power as the AFEI if the power supplies are not changed. However, by reducing the voltage of the supplies (almost all the power used by the AFEII is at 2.5V) or using POL DC-DC converters, the power dissipation can be significantly reduced.

Voltage	Current Required per board	Actual measured current per backplane	Current available from PS per backplane	Power dissipation per AFEI board (rounded up)
+5 Volts	2.75 Amps	22 Amps	40 Amp	14 Watts
+5.5 Volts	2.125 Amps	17 Amps	20 Amps	13 Watts
±12 Volts	0.5 Amps	4 Amps	6 Amps	6 Watts
+3.3 Volts	4 Amps	32 Amps	40 Amps	13.5 Watts
Total				46.5 Watts

Table 2 AFEI power consumption (taken from note A991117A)

Voltage	Current Required per board	Current per backplane (estimated)	Current available from PS per backplane	Power dissipation per AFEII board (rounded up)
+5 Volts	3.5 Amps	28 Amps	40 Amp	18 Watts
+5.5 Volts	2 Amps	16 Amps	20 Amps	12 Watts (1)
±12 Volts	0.5 Amps	4 Amps	6 Amps	6 Watts
+3.3 Volts	3.5 Amps	28 Amps	40 Amps	12 Watts
Total				48 Watts

Table 3 estimates based on testing of the AFEII prototypes.
(1) Note: 5.5V supply is actually operated at about 6V

3.3. Cooling Requirements

50 CFM airflow is provided by fans mounted below the backplane, providing airflow back-to-front. Normal bottom-to-top airflow is unavailable because the bottom is blocked by the

cryostat. Air dams are used on the AFEI boards to direct the airflow to the regions of the board of greatest power dissipation.

4. SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

Typical protection features such as temperature monitoring and power supply fusing are present on the AFE. The critical analog components are further insulated from power supply transients by the use of on-board linear regulators. Power dissipation has been minimized such that no component will dangerously overheat (e.g. to points of combustion) even if the fans fail; unassisted convection tests of physical heat models show that the air exit out the front is wide enough to accomplish this.

4.1. Module Fusing & Transient Suppression

All power supplies entering the AFE from the backplane are fused and have transient suppressors.

4.2. Other Safety & Quality Assurance

A built-in temperature sensor and continuously reports the temperature of the board. Bulk power supplies are remotely sensed at the backplane. JTAG boundary scan is being investigated for use in board checkout. A number of additional test points are being added to assist board testing and debugging.

Appendix A

Proposed list of modification relative to AFEII prototype

1. MCM design

1.1. TriP interface

There seems to be no need for the level translators from 3.3V to 2.5 because the FPGA will be run at 2.5V VCCO. Reduces board chip count by 16.

1.2. LVDS

The LVDS mux will be changed from a Lattice CPLD to a Xilinx FPGA. This will simplify the board design by making the board more homogeneous and reducing the skill set required to maintain the board. It will also make it possible to specify the LVDS personality via software. There exists a conceptual architecture for doing this, but it needs to be implemented in VHDL to check timing. The estimate here is about 1 week of work. Also reduces chip count by 32!

1.3. Analog Control FPGA

We will change the muxing of the ADCs to allow all 10bits of the ADC to go to the FPGA on individual pins from both ADCs. Also the control scheme for the TriP needs to be redone. Since there is no longer any need for the level translators, some IO pins will become free. Many more IO pins can become free if the DISCR outputs are not routed to this chip at all. This is possible if the LVDS mux is replaced with an FPGA. This will allow all the DISCR functions currently performed in this chip to be moved to the LVDS mux. The LVDS mux would make the required DISCR data available to this chip during DIGITIZE mode. In addition, the PIC DATA bus will share the slave parallel configuration lines, freeing additional IO. Some of this additional IO will be used to make the “SVX” data bus a “string-of-pearls” topology which will allow this bus to run at a much faster frequency.

1.4. 53Mhz Readout

The main change here is the change in the topology of the readout bus, as described above from a “bus” to a “daisy chain” topology, where every FPGA in the readout chain acts as a FIFO. This will clearly allow the bus to run at a much higher frequency and remove concerns about 53MHz readout. There is also no need for a “VSVX” chip on this bus any longer, since every FPGA is a virtual SVX, but we will use a small FPGA to drive the grey cable buffers for added flexibility and control.

2. Slow control

2.1. 1553

This circuit appears to be very simple at first glance, but in fact continues to exhibit intolerance to slight component variation. Even taking the measure of transistor beta matching has not made this circuit as robust as desired. On the other hand, the simplicity of this circuit and the vast experience of people with it makes it easy to debug and repair. In other words, while we wish we had a more reliable alternative, barring additional engineering resources, this circuit will stay as is, with screening of the key components (transistors, transformers) done before being shipped to assembly house.

2.2. Temperature control

We wish to find a method of calibrating the resistance reading without the use of external hardware (AFE-TM). This seems easily possible by adding precision resistors of the right value to the board itself, selectable by jumpers.

2.3. Bias

The presence of -12V on the mux can destroy other chips if inadvertent shorts are encountered, but this is minor. Simply using ground instead of -12 will solve this very minor problem.

2.4. Flash

There is an issue which is not understood, which seems to cause the flash to lose some of its programming when the board is inserted into the backplane. Is this caused by a minor static shock? This is an open issue.

2.5. PIC

The PIC has been change to the 18F452 rather than the present 16F877A. This is a trivial modifications as the two chips are pin compatible. Also, the PICDATA bus right now has a fanout of 33. This is not fatal, but it is a concern. Perhaps this bus can be split!

2.6. Helper

In order to make the board more homogeneous, we will replace this CPLD with a Xilinx FPGA. This is probably overkill, but it will also allow the chip to act as a level translator between the 5V PIC and the 2.5V FPGAs.

2.7. Power supplies

Power supply design is a key ingredient of making the AFEII a reliable, useful board. The AFEII does not differ significantly from the AFEI in the total power dissipation or the required voltage levels, but it differs significantly in the patterns of current draw. That is, the AFEI would draw a roughly constant amount of power from the moment it was turned on to any moment in operation. The power consumption of the AFEII changes by two orders of magnitude in current consumption between applying power to the board and full board operation. This is caused mainly by the fact that FPGAs are volatile devices. The proposal for handling these challenges on the AFEII follows. Make sure that all voltages (except the +-12V) are always used with a local regulator. This means that the circuitry of the AFEII will be essentially immune to variation in the supplied voltage. The regulators must be properly sized to allow the full power to be dissipated, but the currents are small enough that this should not present a significant problem, especially if the regulators are distributed at each chip (i.e. each FPGA has its own regulator, each TriP-t, each ADC, etc.) By spreading the power between the 5V rail and the 3.3V rail and putting the maximum amount of power on the 3.3V rail, we can minimize the total power consumption of the system.

2.8. Clock distribution scheme

The AFEII requires a well thought out clock distribution scheme. The key is point to point distribution of the clock to the FPGAs using adjustable phase delay outputs to correct for differences in trace length across the board. Proper termination and attention to trace impedance and routing are also important. The solution to this is to use the Lattice ispClock 5610 chips. This scheme is currently being worked out in detail.

AFEII performance specifications summary

This summary is intended as a convenient reference for quantitative information about the performance specifications of the AFEII for a reader already familiar with the function, architecture and operational principles of the AFEII.

1. GENERAL BOARD REQUIREMENTS

The AFEII board shall be plug compatible with the AFEI. It shall be capable of operating in the same position on the cryostat, with the same power supplies, dissipating the same amount of power, with the same interface to L1 and L3. It may however, ignore the SEQ to SVX download behavior of the AFEI. It may also vary in some of the interfaces of the 1553. It may require some 1553 downloading.

2. MCM

The MCM shall have 64ch. There shall be one prompt discriminator output per channel. Each channel shall also have its amplitude digitize after the receipt of the L1ACCEPT signal (this signal is a post trigger with a latency of about 4.1uS). The MCM shall also be capable of measuring the time at which the discriminator fired relative to the signal integration gate.

2.1.1. DISCRIMINATORS

Every discriminator shall be settable to a threshold of no more than 10fC (measured at the 50% point.) The discriminators will not be required to have a per channel threshold setting, but the allowed spread on the discriminators is 4fC or less (measured at the 50% point). The noise of the discriminators (as measured by a Gaussian fitted to the turn on curve) shall be about 1fC with a 35pF input load. The 64 discriminator outputs will be sent to the LVDS transmitter at 53Mhz, 10 bits per clock per MCM, with the 1st output bits available within five 53Mhz clocks of the close of the signal integration window.

2.1.2. AMPLITUDE

The MCM shall be able to digitize the amplitude of the VLPC signals with an effective precision of 6.6 bits. The dynamic range of the MCM shall be settable between a max of 100fC (~1fC/LSB) at highest gain to 3000fC (~30fC/LSB) at lowest gain with at least eight intermediate values.

2.1.3. TIME MEASUREMENT

The MCM shall also be capable of measuring the time at which the discriminator fired relative to the beam crossing clock with 6 bit accuracy and a dynamic range of about 120ns. In other words, when operating with a dynamic range of 120ns, the accuracy of the digitized time stamp shall be within 2ns of the true time.

3. CLOCK

The AFEII receives two clocks: the crossing clock (XING) and the SVX clock. The XING clock is always available. The frequency of the XING is RF/7 (~53Mhz/7). This clock is used as a reference to a PLL to reconstruct the 53Mhz RF clock. This 53Mhz is distributed to all eight MCMs, the VSVX and the LVDS transmitters. The clock distributed to the MCMs shall have a chip to chip skew of 500ps or less. The clock distributed to the VSVX, the LVDS transmitters or any other chip may have any phase, as needed for proper function.

The SVX clock is not a constant clock. It is used only by the VSVX and only during the READOUT mode, such that the rate of L3 readout may be set to a value other than 53Mhz. This is required for compatibility with the existing system.

4. VLPC bias and temperature control

The AFEII shall set bias with an absolute accuracy of +-25mV of desired voltage in the range from 5 to 9 V. It shall be able to set any voltage from 0 to 9V. The bias voltage read back shall be accurate to 10 bits. The current read back shall be accurate to 10 bits in the range from 0 to 100nA.

The AFEII shall measure the temperature sense resistor with an accuracy of 0.15 ohm RMS. The sense current shall not exceed 15 uA . The board shall be able to keep the temperature of the VLPCs in the 4 cassette test cryostat within 50 mK of set point.

5. Slow control and monitoring

For slow control and monitoring, the AFEII shall implement those parts of the AFEI interface which are functionally unchanged (using the same 1553 locations, commands and parameters): VLPC temperature control and monitoring, VLPC bias voltage setting, read back and VLPC current measurement. All other functions may be modified, deleted or added as required.

6. L3 readout

For Level3 readout, the AFEII shall be capable of behaving exactly as the AFEI

- Suppressing the timing information
- Reading out amplitude data using the same format and the same channel numbering and ordering.
- Perform zero suppression
- Inserting “VSVX” discriminator data before the amplitude data, same as AFEI

For any readout detail not specified herein, the definition of “behaving the same as AFEI” shall be construed to mean that the AFEII is capable of being read out on the CTS with no modification to sequencers/ sequencer controller or any other board, except that the AFEII may require a different download procedure.

7. L1 readout

The LVDS readout of the board is covered in section 2.1.1 . The AFEII shall interoperate with the existing L1 system with no modifications to the firmware of any board in the L1 chain.