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Scintillation Counter and Wire Chamber Front End Modules for High Energy Physics Experiments

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Abstract

This document describes two front-end modules developed for the proposed MIPP upgrade (P-960) experiment at Fermilab [1]. The scintillation counter module was developed for the Plastic Ball detector [2] time and charge measurements. The module has eight LEMO 00 input connectors terminated with 50 ohms and accepts negative photomultiplier signals in the range 0.25…1000 pC with the maximum input voltage of 4.0 V. Each input has a passive splitter with integration and differentiation times of ~20 ns. The integrated portion of the signal is digitized at 26.55 MHz by Analog Devices AD9229 12-bit pipelined 4-channel ADC. The differentiated signal is discriminated for time measurement and sent to one of the four TMC304 inputs [3]. The 4-channel TMC304 chip allows high precision time measurement of rising and falling edges with ~100 ps resolution and has internal digital pipeline. The ADC data is also pipelined which allows deadtime-less operation with trigger decision times of ~4 μs. The wire chamber module was developed for MIPP EMCal detector charge measurements. The 32-channel digitizer accepts differential analog signals from four 8-channel integrating wire amplifiers. The connection between wire amplifier and digitizer is provided via 26-wire twist-n-flat cable. The wire amplifier integrates input wire current and has sensitivity of 275 mV/pC and the noise level of ~0.013 pC. The digitizer uses the same 12-bit AD9229 ADC chip as the scintillator counter module. The wire amplifier has a built-in test pulser with a mask register to provide testing of the individual channels. Both modules are implemented as a 6Ux220 mm VME size board with 48-pin power connector. A custom europack (VME) 21-slot crate is developed for housing these front-end modules.

I. MIPP Scintillation Counter Module

1. Introduction

The MIPP Scintillation Counter Module is designed to provide charge and timing measurements of a photomultiplier signal. The original Plastic Ball detector was built using 2-inch 10-stage 2202 Amperex phototubes. Each detector element consists of a photomultiplier attached to a plastic scintillator 35.6 cm long. A 4 mm slice of CaF_2(Eu) crystal is mounted on the top of the plastic scintillator. The main component of the decay time of the plastic scintillator is ~10 ns. The CaF_2 scintillator decay time is approximately 1 μs. The slow and fast components of the signal are to be separated and respective integrated charge and arrival time independently measured. Any other photomultiplier based detector signal requiring charge only or time only measurement can be processed as well.

2. Module description

The upgraded MIPP DAQ requires trigger rates up to 3 kHz with minimum interval between triggers of 16 μs and trigger decision time of 2 μs [4]. The extracted beam spill may be up to 6 seconds long. This requires for the front-ends to store up to 20000 events per spill. Stored events are to be read out during between spill intervals of 54 seconds. The specified interval between triggers of 16 μs allows implementation of deadtime-less front-end electronics design

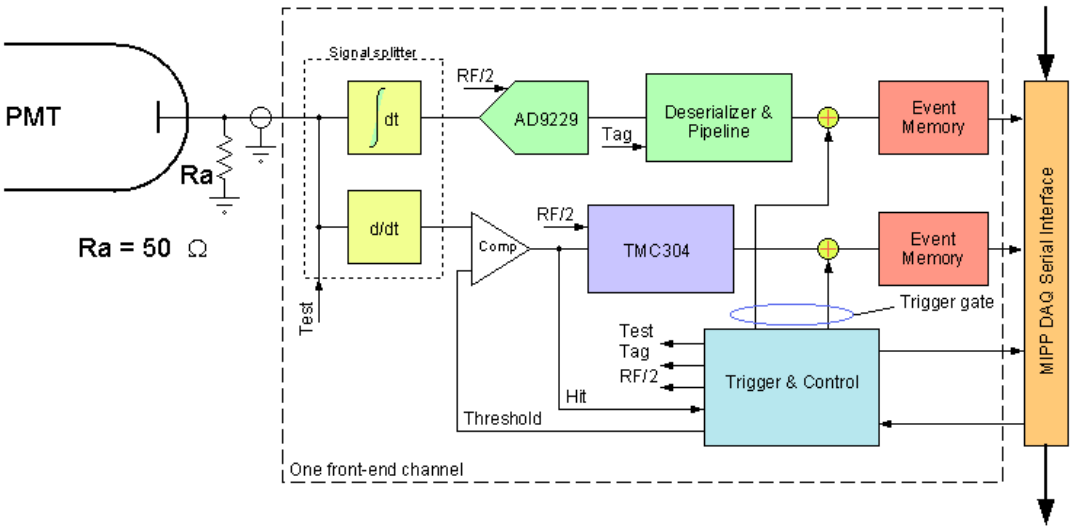

Figure 1: Block-diagram of the module

similar to the D0 Muon Electronics readout [5]. Such an approach requires continuous digitization of the detector signal and allows using reliable digital pipelines to compensate for trigger decision time. As one can see, the module could also be run in a continuous mode as well, reading out events after each single or multiple trigger occurrences.

A block-diagram of the Scintillator Counter Module is shown in Figure 1. The photomultiplier signal is split by a passive splitter with integration and differentiation times of ~20 ns. The differentiated signal is discriminated for time measurement and sent to one of the

four TMC304 inputs [3]. The TMC chip allows high precision time measurement of rising and falling edges with ~100 ps resolution and has internal digital pipeline. The TMC chip has multi-hit capabilities with the minimum time between hits of one clock interval. The integrated portion of the signal is digitized at the 26.55 MHz clock frequency by Analog Devices AD9229 12-bit pipelined 4-channel ADC. The ADC output is de-serialized and delayed by an external digital pipeline. The ADC samples taken at the clock frequency can be used for calculation of a charge or signal shape analysis. When the trigger signal arrives it generates a trigger gate which controls ADC and TMC data transfer to the external event memory.

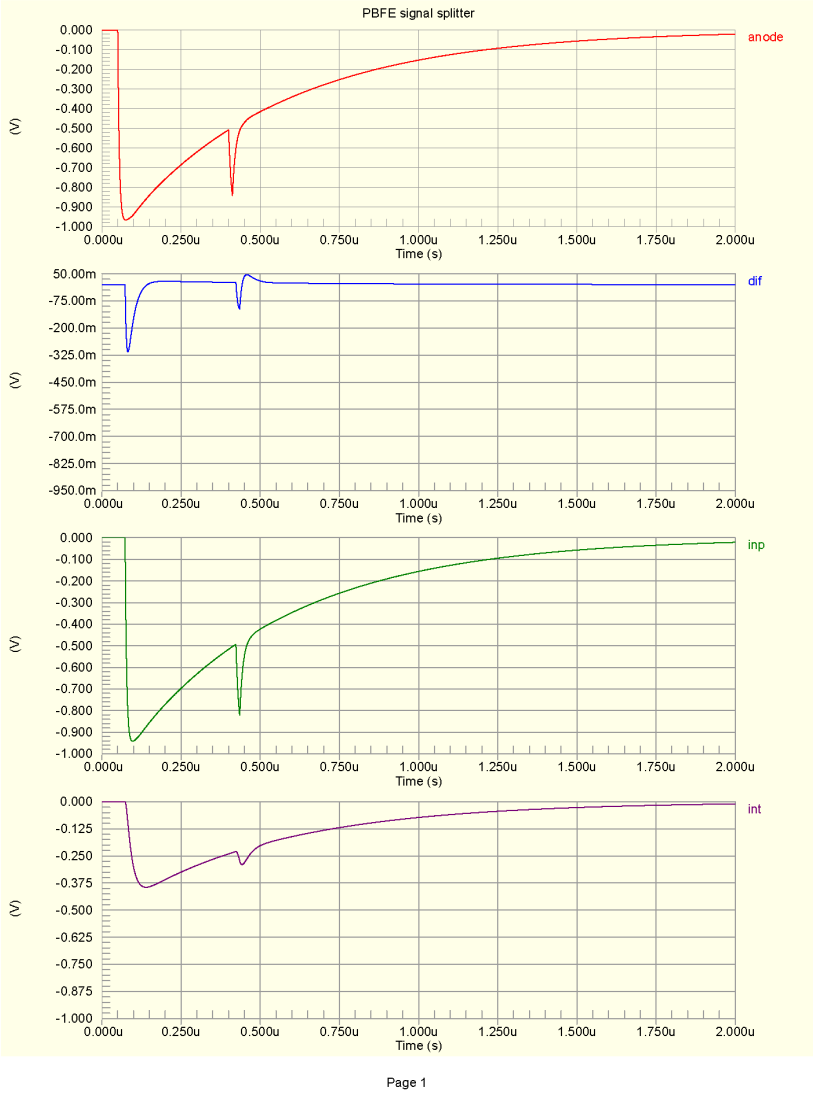

Figure 2: SPICE simulation of the passive signal splitter

A SPICE simulation of the passive signal splitter outputs with differentiation and integration time of 20 ns and 5 meters of RG-174 cable is shown in Figure 2. The photomultiplier signal was simulated by a current source with a rise time of 10 ns and fall times of 10 ns and 500 ns. The plots labeled *dif* and *int* show differentiated and integrated outputs of the splitter respectively. The plot labeled *inp* shows the signal at the splitter input. Additional study with the actual detector signal is necessary to select the value of the time constant of the splitter.

3. Details of the design

A detailed block diagram of four front-end channels is shown in Figure 3. The outputs of the splitter are buffered with separate amplifiers. The differentiated signal is discriminated by a comparator with a programmable threshold. The TMC chip has an internal pipeline of 128 cells which provides maximum delay of 4.8 µs at the clock frequency of 26.55 MHz. The pipeline for the ADC data is implemented in a FPGA. At the arrival of a trigger signal the digitized data from the TMC and ADC pipeline outputs is temporarily stored in FIFO memories. The duration of the trigger signal determines how many data words are written to the memory. Zero suppression is performed during this process using a hit bit for the TMC data and internally generated tag bit for the ADC data. The channel data is stored only if the corresponding comparator was fired.

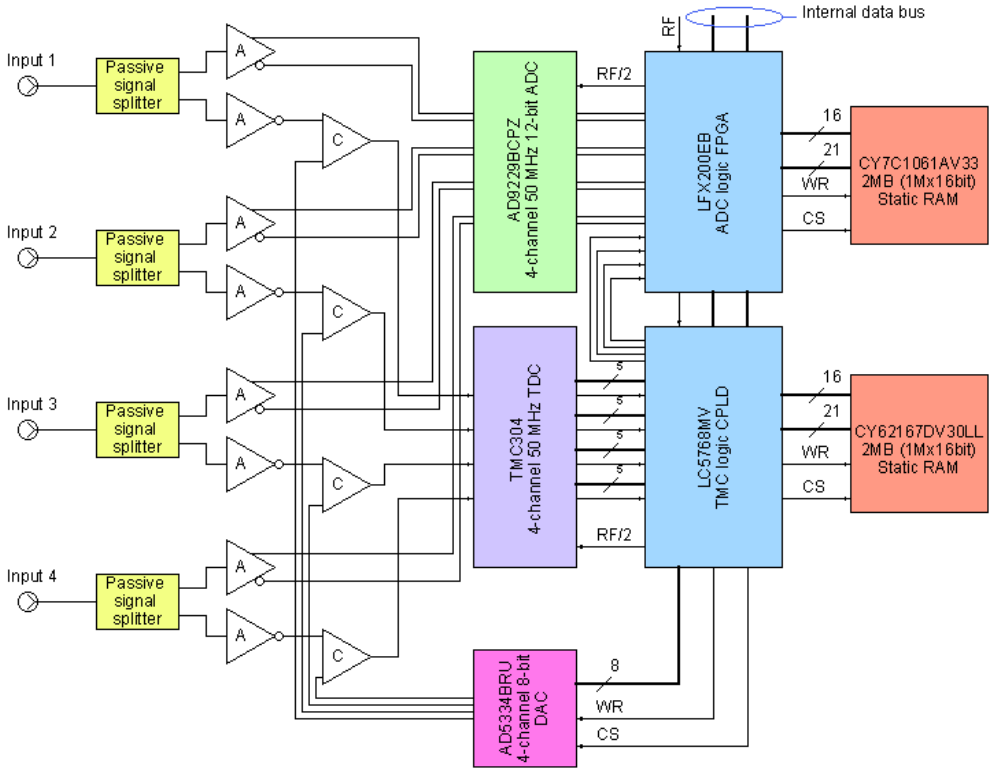

Figure 3: Detailed block-diagram of four channels

The ADC tag bit is generated individually for each channel by a programmable one-shot (see Figure 4). Using this procedure, only non-zero data words are stored in FIFOs. At the end of the trigger gate an event sequencer writes event data from FIFOs to the external RAMs. Writing event data to RAMs takes less than specified minimum interval between triggers, and the front-end is ready for the next trigger before it may arrive. This guarantees deadtime-less operations of the front-end. The module has read/write 16-bit registers to control delay and width of the trigger gate and ADC pipeline delay. The TMC read and write pointers are programmed via internal TMC registers [3].

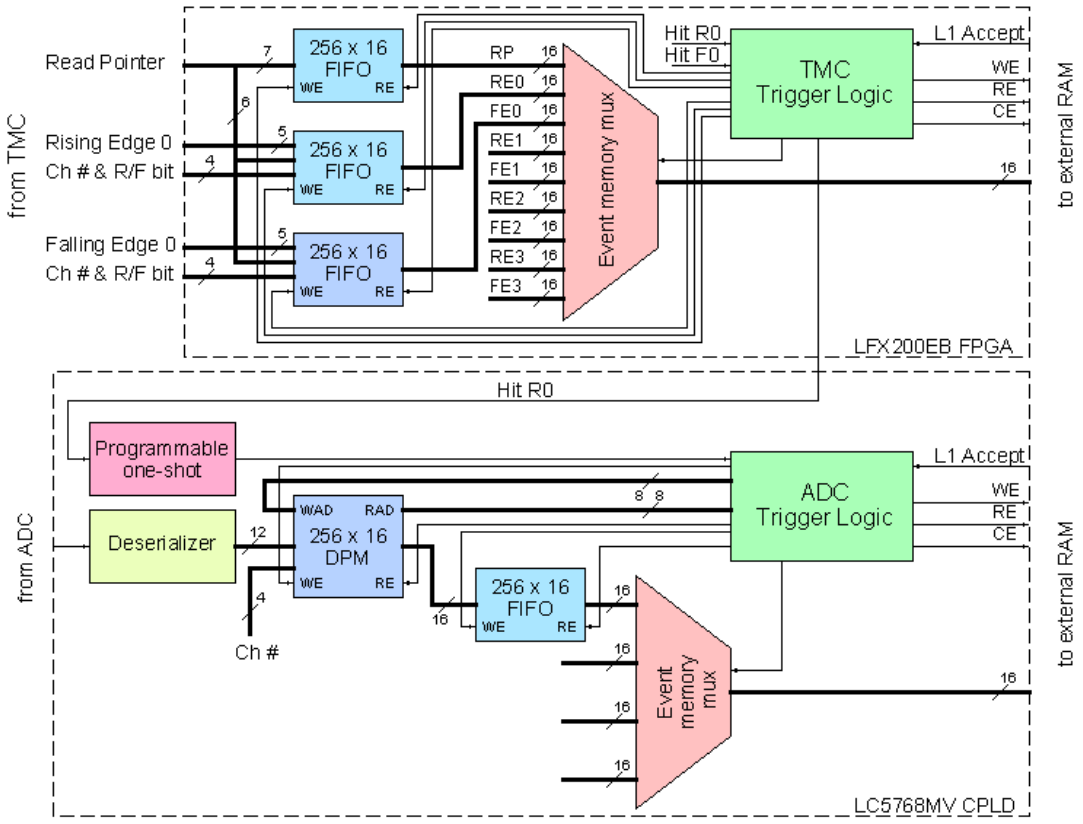

Figure 4: Details of the trigger logic

For the MIPP experiment events are read out via serial DAQ interface at the end of the spill. The interface uses transformer isolated LVDM receivers and transmitters on four twisted pairs of the standard networking cable CAT-5e. Two of the pairs are bussed and the other two are chained. The bussed pairs are terminated at the far end of the cable. The chains start at the far end and are terminated at each front-end and the readout controller. Each front-end board has two RJ-45 connectors to facilitate chain connectivity. One of the bussed pairs is used to transmit timing messages and a clock signal. The other pair is used to transmit command messages. The

responses of the front-end to a command and event data are received by the readout controller via two cable chains. The information is transmitted on all wire pairs in 20-bit frames. Each frame is FM encoded at 26.55 MHz and consists of a start bit, two control bits, 16 data bits and a parity bit [6]. When there is no data transmission, undisturbed clock signal is sent instead. The module also has an USB interface for debugging and test purposes. The FTDI UM245R daughter card can be installed in the board socket to facilitate this feature. The UM245R uses 8-bit wide data and mimics functionality of the standard serial interface. A different version of the control firmware is required for the UM245R interface.

An event is formed by the event sequencer upon readout request from the DAQ controller. The sequencer reads the event length from each RAM and calculates total event length. The event then is transmitted via serial interface. The event format includes leading word count, event header, variable segments of ADC and TMC data for each channel that has a valid hit, and a global checksum. The event header includes 32-bit time stamp and status information. Each front-end has a time stamp counter which is sampled at the arrival of the trigger. The time stamp counter is reset at the beginning of the spill. Figure 5 illustrates ADC data profile collected with on-board test pulser.

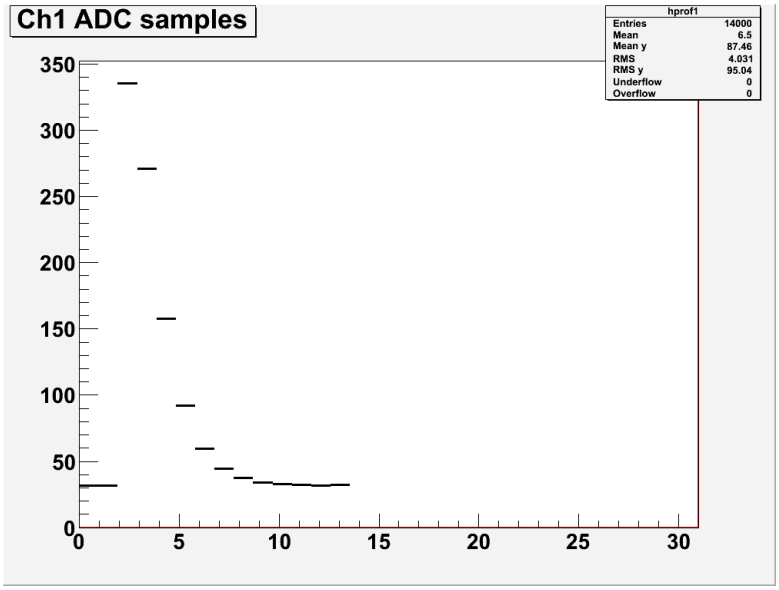

Figure 5: Profile of ADC samples for test signal

4. Module implementation

The Scintillation Counter Module features programmable on-board test pulse generator with an individual 12-bit DAC and a mask bit for each channel. Each channel has an individually programmable 8-bit threshold DAC. The module also has an internal timing sequencer that can

simulate extracted beam timing sequence. The following 16-bit registers are implemented in the USB version of the firmware:

- ADC pipeline setup register (read/write)
- ADC logic status register (read only)
- Test pulse DAC control register (read/write)
- ADC gate width and test pulse mask register (read/write)
- TMC data bus control register (read/write)
- Threshold DAC data bus control register (write only)
- TMC status/control register (read only 0-7, read/write 8-15)
- TMC pipeline setup register (read/write)
- Board temperature ADC register (read only)
- Board status register (read only)
- Lower word of time stamp counter preset register (read/write)
- Upper word of time stamp counter preset register (read/write)
- Trigger gate delay and gate width register (read/write)
- Timing setup register (read/write)
- Spill gate delay and width register (read/write)

5. Specification

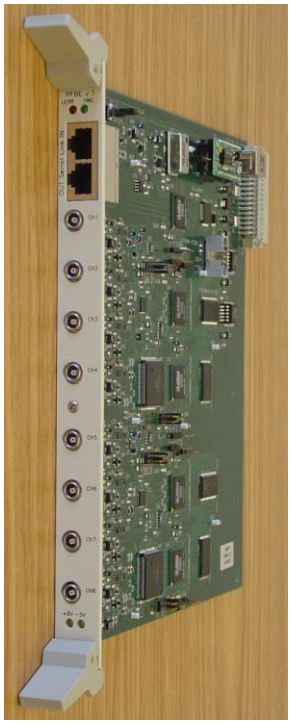

Figure 6: Scintillation Counter Module

Power consumption	- +5V/2.4A, -5V/0.15A
Form factor	- 6U x 220 mm
Main clock frequency	- 53.1 MHz (± 200 ppm)
Number of inputs	- 8
Input signal range	- 0…4V/50 ohm
Programmable threshold	- 0…2048 mV/8 bit
ADC sampling frequency	- 26.55 MHz
Signal sampling accuracy	- 12 bit
Timing bin width	- 1.2 ns
Timing resolution	- 100 ps
Double pulse resolution	- 38 ns
Event memory size	- 2 MByte
Data interface	- serial FM or USB
Interface clock frequency	- 26.55 MHz
Interface connectors	- RJ-45
Interface cable	- CAT-5e or USB
Front panel LED	- Error, Link, +5V, -5V

Two prototype boards are assembled and tested using auxiliary USB interface and serial DAQ controller simulator. The DAQ software was developed in C-language to allow data taking with internal or external triggering.

II. MIPP EMCal Wire Chamber Module

1. Introduction

The MIPP EMCal Wire Chamber Module is designed to provide charge measurement for the EMCal wire chamber detector. The module has similar to the Scintillation Counter Module design and employs the same Analog Devices AD9229 12-bit pipelined 4-channel ADC. The module has 32 inputs and accepts differential analog signals from four 8-channel integrating amplifiers. The 8-channel integrating amplifiers are connected to the module via 26-wire twist-n-flat cables. This cable also provides power and control signals to the amplifier. The design of the amplifier is customized to the specifics of the MIPP EMCal detector, but could be modified as necessary.

2. Integrating wire amplifier

The EMCal Wire Amplifier board (Figure 7) is a charge sensitive amplifier with differential analog output. Each channel consists of ½ Analog Devices ADA4841 and one AD8132 operational amplifier. The integrating constant of the current sensitive first stage is 500 ns (Figure 8). There is a monitoring output, which is a sum of eight output signals, available at the LEMO 00 output connector. The board has a SPI serial interface for setting up the mask register, amplitude of the test pulse and triggering a test pulse generator. The mask register allows selection of individual channels for testing.

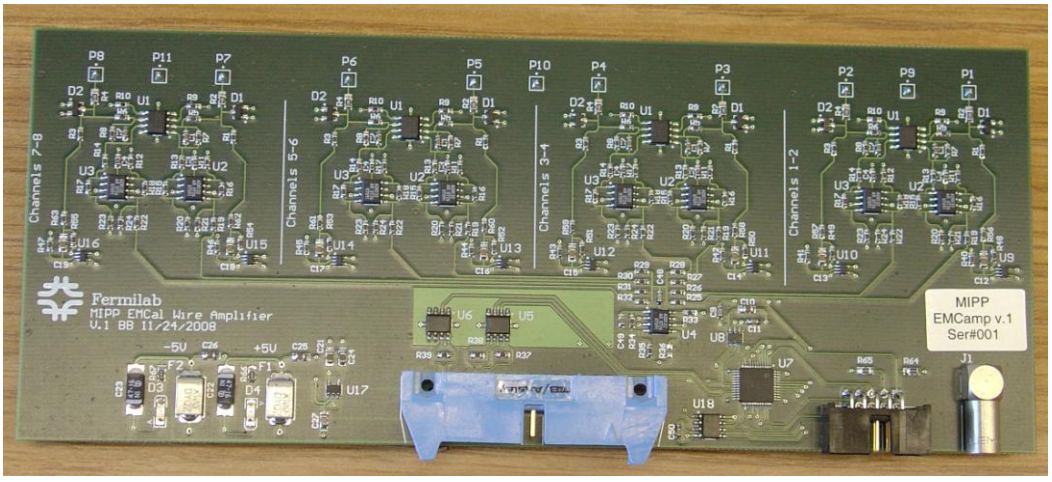

Figure 7: 8-channel integrating wire chamber amplifier

The amplifier board has a 26-pin connector for standard twist-n-flat cable. Eight pairs used for signal transmission, two pairs provide power and ground connection and three pairs are used for communication with the digitizer module. There are three differential signals used for control purposes: SCLK, SDIN and SYNC/Test. The SYNC/Test signal is used for two purposes. Two most significant bits (bit 15 and bit 14) of the serial data control the on-board logic. If any of these bits are non-zero, the data is decoded by the on-board logic. If none of these bits is set a test pulse is generated. There is a 720 ns delay between the first edge of the SYNC signal and the rising edge of the test signal.

The amplifier board receives +5V/-5V power from the 32-channel digitizer board. The power consumption of one board is 140 mA @+5V and 120 mA @-5V. A 10 μA square test pulse of 50 ns wide generates a ~275 mV integrated differential signal at the terminated twisted pair. This corresponds to 275 mV/pC sensitivity. The full differential range of the digitizer's ADC is 2V p-p. Note that the amplitude of the amplifier output depends on the shape of the wire signal and, therefore, additional testing with the actual detector is necessary to adjust the gain. The noise level measured with the scope is 0.013 pC, which corresponds to ~0.8×10^5e. The noise level measured by the module's 12-bit ADC with on-board pulser and open input is 0.015 pC.

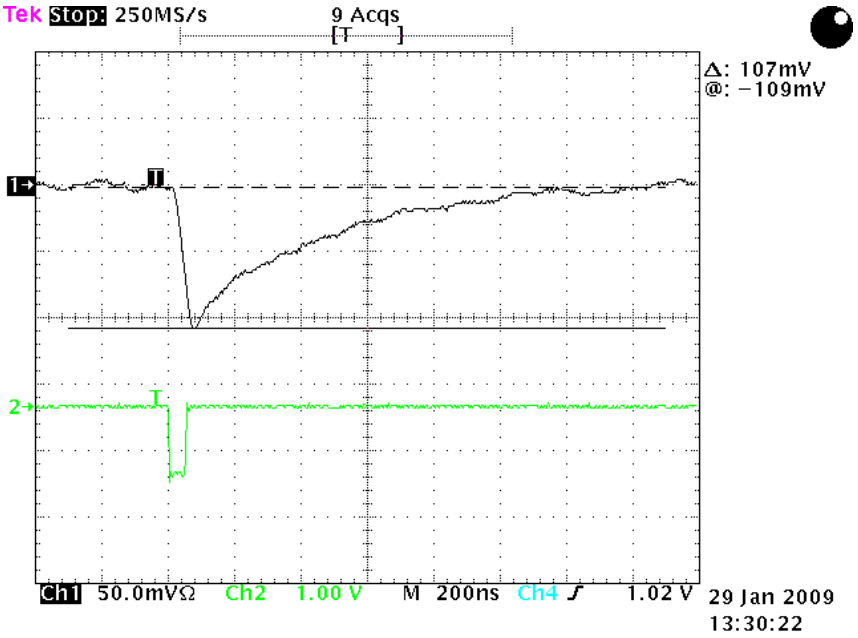

Figure 8: Wire amplifier output (Ch1) vs input (Ch2)

3. 32-channel digitizer

The digitizer module provides continuous sampling of the 32 differential inputs. In order to facilitate zero suppression, a hit tag bit is added to the pipeline input (Figure 9). At the arrival of the trigger signal only ADC data accompanied by the tag bit are written to the FIFO (not

shown). The hit bit pulse is generated by the programmable one-shot fired by the comparator as in the Scintillation Counter Module (see above). Thus duration of the hit bit determines the amount of the ADC data written to the event memory. The event data from each fired channel is transferred sequentially to the common event memory and, therefore, affects the minimum time interval between triggers. The SPI interface with the wire amplifiers can be disabled to improve signal to noise ratio.

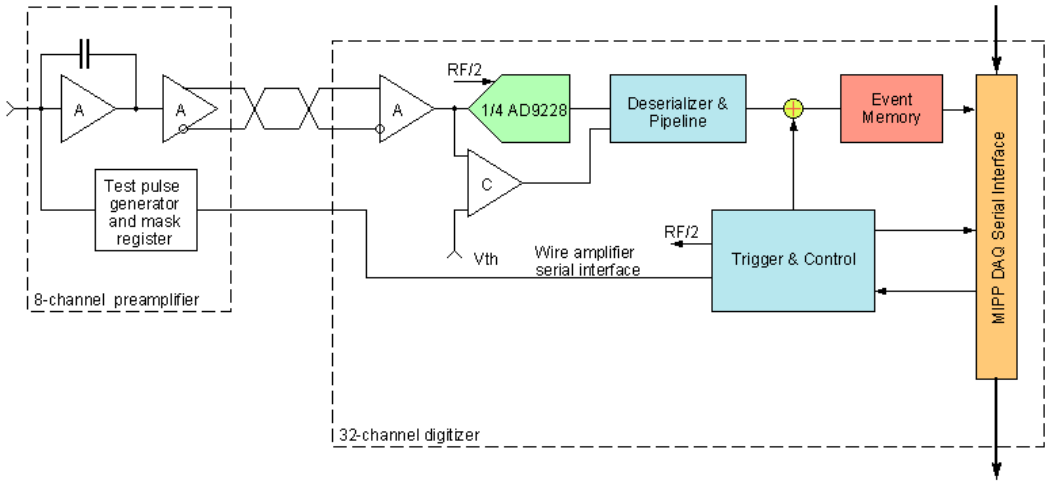

Figure 9: Block-diagram of one channel of the digitizer

The digitizer module provides +5V/-5V power to the wire amplifiers via the same 26-wire cable used for analog signal transmission. Due to the voltage drop on the cable, the length of the cable is limited to ~30 ft. An external power supply is necessary if the cable length exceeds this limit. The digitizer board features an 8-bit threshold DAC for each channel and common for eight channels ADC gate width (tag bit) and channel enable register. This register also has the SPI enable bit which has to be enabled when communicating with the wire amplifier board. As with the case of the Scintillation Counter Module, there are two versions of the firmware developed for this board: serial and USB. The module also has an internal timing sequencer that can simulate extracted beam timing sequence. The following 16-bit registers are implemented in the USB version of the firmware:

- ADC pipeline setup register (read/write)
- ADC logic status register (read only)
- EMCal wire amplifier mask or test pulse DAC or ADC channel threshold DAC control register (write only)
- ADC gate width and channel enable register (read/write)
- Board temperature ADC register (read only)
- Board status register (read only)

- Lower word of time stamp counter preset register (read/write)
- Upper word of time stamp counter preset register (read/write)
- Trigger gate delay and gate width register (read/write)
- Timing setup register (read/write)
- Spill gate delay and width register (read/write)

Two prototype boards are assembled and tested using auxiliary USB interface and serial DAQ controller simulator. The DAQ software was developed in C-language to allow data taking with internal test pulser.

4. Specification

Power consumption	- +5V/5.8A, -5V/0.6A
Form factor	- 6U x 220mm
Main clock frequency	- 53.1 MHz (± 200ppm)
Number of inputs	- 32
Input signal range	- 0…2Vp-p
Programmable threshold	- 0…2.5V/8 bit
ADC sampling frequency	- 26.55 MHz
Signal sampling accuracy	- 12 bit
Event memory size	- 2 MByte
Data interface	- serial FM or USB
Interface clock frequency	- 26.55 MHz
Interface connectors	- RJ-45
Interface cable	- CAT-5e or USB
Front panel LED	- Error, Link, +5V, -5V

Figure 10: Wire chamber module

III. Custom europack (VME) crate

A custom 21-slot crate was designed to house 6Ux220 mm modules. The crate is based on the VME mechanical standard and utilizes a custom backplane to distribute power. The backplane is built using 48-pin DIN connectors. Due to the higher power dissipation the Wire Chamber Module cannot be used without forced air cooling.

Figure 11: Custom europack crate

Two sets of power supplies could be used with the crate. For the Scintillation Counter Module +5V/60A and -5V/10A power supplies provide enough power for a full crate. For the Wire Chamber electronics +5V/120A and -5V/20A power supplies would be enough to run 21 modules.

IV. References

[1] Rajendran Raja, et al., “Proposal to Upgrade the MIPP Experiment,” MIPP Document Database #1046-v1, Fermilab, October 2010.

[2] B.Baldin. "Plastic Ball Electronics, " MIPP Document Database #173-v1, Fermilab, April 2007.

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