Experimental System for Monitoring and Diagnosis of a Static Power Converter

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***Abstract*—The evolution of the computer aided design and control technologies in the field of static power converters leads also to diagnosis systems which include modules based on artificial intelligence. In order to achieve satisfactory reliability, the static power converters must even be assembled by using high reliability devices and/or be conceived as redundant topologies.**

The paper presents a dedicated monitoring and diagnosis system of the static power converters. It can be used both for the diagnosis of the transistors within an inverter as well as for the analysis and diagnosis of a power bridge rectifier.

The diagnosis system dedicated to the power rectifiers uses the fault tree method. Based on the symptoms observed in the behavior of the power rectifiers, the diagnosis and the functional test performed by the developed system is based on consideration of the abnormal comportments and the faults which determine these. The experimental system dedicated to the bridge rectifiers analyses and identifies the causes of the faults which occur during the operation and reduces the displayed results if two sets of values of the sources which determine the same answer, differ by a single input.

***Index Terms*—Fault diagnosis, Static power converters, Redundancy, Reliability theory, Monitoring.**

I. Introduction

The paper continues the work of the authors in the field of monitoring and diagnosis systems.

In the first part of the paper, general aspects about reliability and redundancy are presented, related to the static converters reliability improvement. The experimental system developed around a microcontroller (Dallas DS87C550) was used for the off-line diagnosis of an inverter [4]. The paper presents improvements of the experimental system so it can perform an on-line diagnosis of the mentioned equipment, the inverter.

In the second part of the paper a diagnosis system dedicated to a power rectifier is presented. This system is based on the fault tree method, applied by the way of a software fully object oriented - CLIPS.

Fault tree analysis technique is as one of the primary methods of performing reliability and safety analysis. Fault trees graphically represent the interaction of failures and other events within a system. It is presented and applied for different electric systems in [1]. The same technique is analyzed and improved in [23], [24] for power rectifiers. The analyses start from several symptoms and identify the causes which generated them independently [23] and simultaneously [24].

In the present paper the causes which determine the simultaneous occurrence of three main faults are identified. In addition, sequentially new information concerning the devices state is introduced. This information will eliminate some causes and consequently will reduce the number of combinations to be analyzed and further the execution time of the application.

The ability of a system to accomplish the functionality for which it was designed defines the term of availability. In order to carry out the total availability, a system must allow the redundancy of its elements. Partial availability can be achieved by activating partial doubled systems.

In order to attain acceptable reliability, the static converters must be realized by using high reliability components and/or redundant topologies.

When an element or equipment can substitute another failed equipment or element, one can speak about redundancy.

There are two types of redundancy: active one and passive one [3].

A. Active redundancy

For this type of redundancy, when a fault occurs, the outputs are not affected, the error being locally amended or during the path of its propagation toward output.

In practice, the active redundancy implies the multiplication of specially designed voting circuits. The principle diagram is the one depicted in Fig. 1.

The notations denote the following: the system inputs are I_1, I_2 and I_3; the outputs are E_1, E_2, E_3; M_1, M_2 and M_3 are the identical modules and V is the voter.

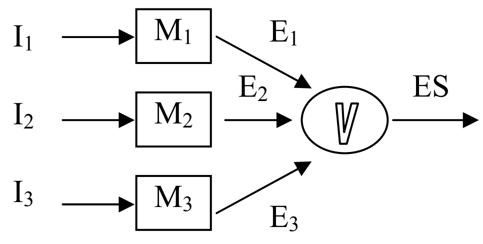


Figure 1. The principle of the active redundancy

This type of protection can be applied in a wide range of system, from integrated circuits to functional modules or even entire subsystems.

B. Passive redundancy

This type of redundancy is achieved by adding of “stand by/reserve” components which are used only if it is necessary (Fig. 2). The “stand by” components became operational even by a manual command, if the system functionality allows a temporary deferment, or by an automatic commutation.

Digital Object Identifier 10.4316/AECE.2013.02018

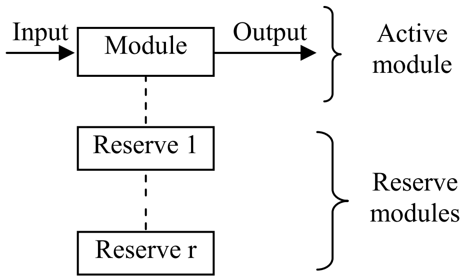


Figure 2. The principle of the passive redundancy

Within the systems designed to complete the active redundancy, the corrective action occurs instantaneously. The systems which use the passive redundancy have the advantage that they allow to send out warnings about the fault state of the entire system. In order to congregate in a single diagram the advantages of the two types of redundancy, a hybrid solution was conceived, depicted in Fig. 3, where: FDD-fault detection device; SS-switching system; V-voting circuit.

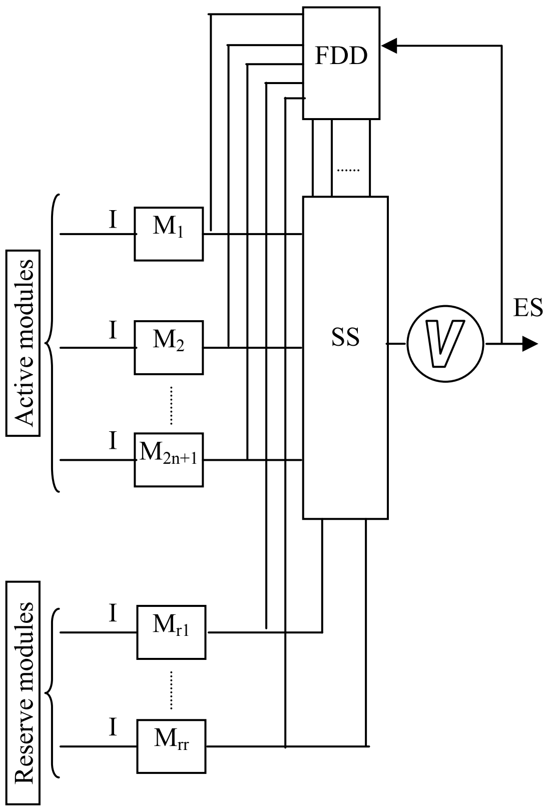


Figure 3. Block diagram of the hybrid redundancy

The output of the system (ES) will have the correct logical value, no matter if the output of a module M_i will have a false value. The output signal ES is applied to the Fault Detection Device (FDD), concurrently with information about the output of the active modules ($M_1 \ldots M_{2n+1}$) and stand by ones ($M_{r1} \ldots M_{rr}$).

If a fault occurs within one of the active modules, the fault detection device will activate a signal directed to the Switching Scheme (SS). This device will block the information emanated by the module in fault towards the voting circuit and will allow the signals originated from the reserve modules to be applied to the voting circuit.

II. Diagnosis System for the Power Devices of an Inverter

In order to obtain high performance equipment to meet present requirements, both in terms of reliability and availability, we performed an experimental system which is based on an algorithm for online verification of each component of the inverter.

The general structure of an experimental system is shown in Fig. 4.

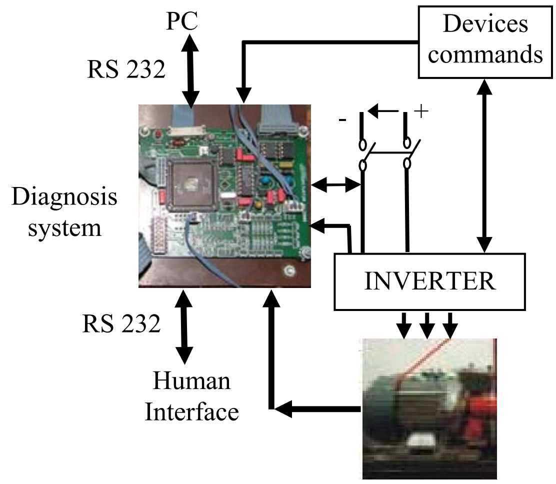


Figure 4. Experimental system for the inverter diagnose

The experimental system is used for the diagnosis of the power switches within an inverter by using the passive redundancy. On one hand, the redundancy can be achieved at the equipment level, where, if a fault is detected, the entire inverter is replaced. On the other hand, the redundancy can be achieved at the component level, where, if a fault is detected, only the element in fault is replaced (Fig. 5).

When one semiconductor of the bridge is in fault, the diagnosis system identifies the arm in fault. Even a single semiconductor of the arm is in fault, the entire arm is replaced by the reserve one, by applying a proper command to the switches $K_1 \ldots K_{10}$. During normal operation, only three of the switches $K_1 \ldots K_4$ will be ON, together with only three of the switches $K_5 \ldots K_{10}$ (Fig.5).

The experimental system monitors, analysis and transmits the result concerning the state of the devices within the inverter. The diagnosis system can access the command terminals of the inverter's semiconductors and the DC bus bars (+, -).

The diagnosis system analyses the state of the bridge (ON or OFF), depending on the commands applied to the semiconductor devices.

The analyzed faults which can occur at the devices level can be of two types: the device can be interrupted (open circuit) or the device can be in short circuit [19], [20].

The operation algorithm of the diagnosis system follows step by step the verification of the state of the inverter's devices. All the devices on every leg are checked to be not interrupted.

Then, the short circuit fault of the semiconductor devices is controlled, by commanding ON each device on the bridge and controlling the state of the bridge ON or OFF.

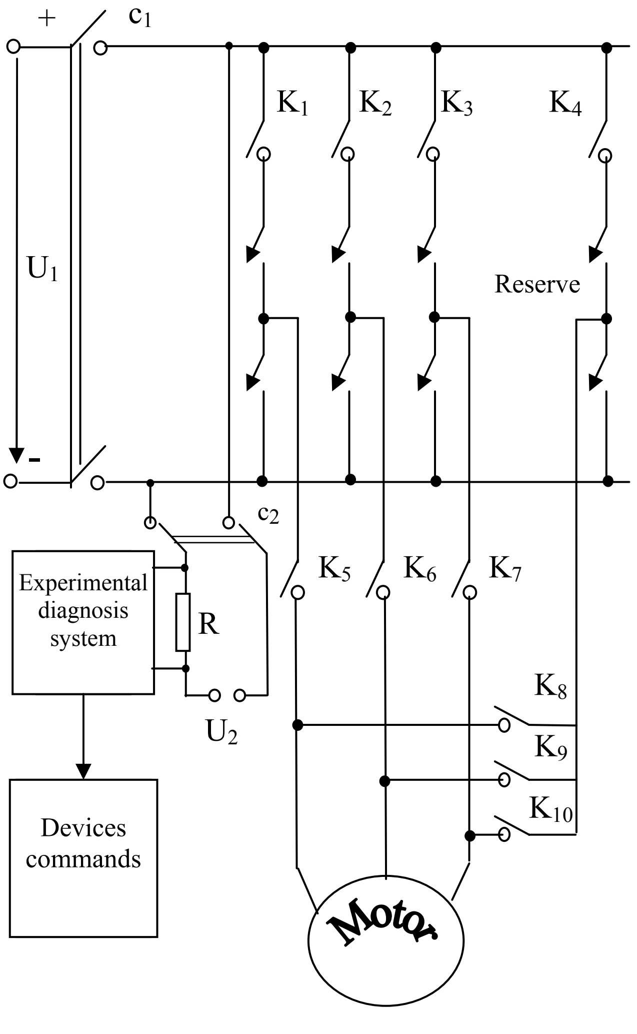


Figure 5. Redundancy obtained by an additional arm

In the first instance, the developed system was used only for the off line inverter diagnosis [4]. As the on-line diagnosis was of interest, the present paper presents this type of diagnosis. The output of the diagnosis system is real time updated in the inverter's control system. A specific problem occurred in this case was related to the response time of the diagnosis system so that no interruptions to occur in the inverter's operation. The delays necessary for the commutation of the reserve elements when faults occur were included in the microcontroller program (Dallas DS87C550) and presented in the paper. The graphical interface was also adapted.

The diagnosis system interacts with the user by the mean of a graphical interface made by using GUI from Matlab [18], [21].

For explaining the diagnosis algorithm, will be considered as example, the short circuit fault of the transistor T_4. The fault detection can be performed by commanding the ON state of the transistor T_1, and observing the ON state of the bridge due to the short circuit of the transistor T_4, even it was not commanded to be ON. If the transistor T_4 would be in good condition, when only T_1 is commanded ON, the state of the bridge would be OFF (Fig.6).

This program sequence is repeated for the other arms of the inverter (T_3 and T_6, T_5 and T_2 respectively) [4].

Another type of fault which can occur is the interruption of the transistor. For the considered transistor (T_4) this fault can be detected by commanding simultaneously only T_1 and T_4 to be ON. In normal operation, the bridge must be ON. If the bridge state is OFF, it results that one or both transistors (T_1 and T_4) are interrupted (Fig.6).

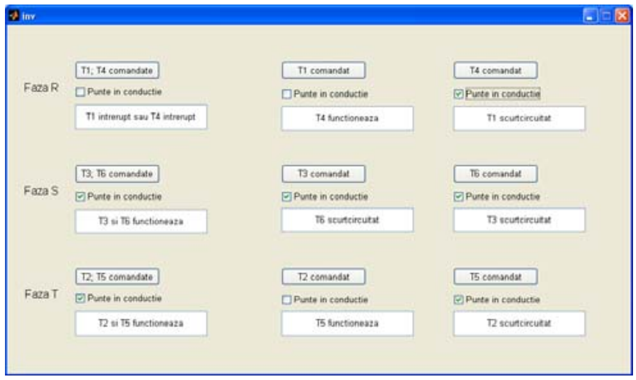


Figure 6. Fault detection of the semiconductor devices interruption/ short circuit

This type of fault highlights one of the limitations of the diagnosis system, the fault can not be anytime located with high precision respectively.

III. Experimental System for Power Rectifier Diagnosis

Having in mind the abnormal symptoms and the faults noticed during the power rectifiers operation, an experimental system for the diagnosis and the functional testing was developed.

The diagnosis system is based on the fault tree method [7]-[10].

In order to characterize the system, the functional diagram of the system is used. The subsystems and elements are identified, as well as the functional connections between them.

The realization the fault tree is an ample process. During this process the analyst must prove good and deep knowledge of the studied system. The fault tree is developed hierarchically starting from the top level which is the considered critical event. Then the secondary level is developed, in accordance with the desired level of detail.

The method of the fault tree has as main disadvantage the difficulty to build the fault tree for highly complex systems. For this kind of systems, the methodology based on the fault tree may be quite difficult to be performed manually [5].

A diagnosis system for the diagnosis and functional testing of the power rectifiers is developed, starting from the anomalous behaviors, noticed during the operation, and the faults which determine these.

The notion of "fault" of a certain device has a different significance if the fault is analyzed taking into account the effects of the fault on the other components of the system. Therewith, a complete fault of device within a bridge rectifier can be the cause of a partial fault of the subsystem which contains the device [1], [2].

The functional scheme of the diode bridge rectifier is depicted in Fig. 7.

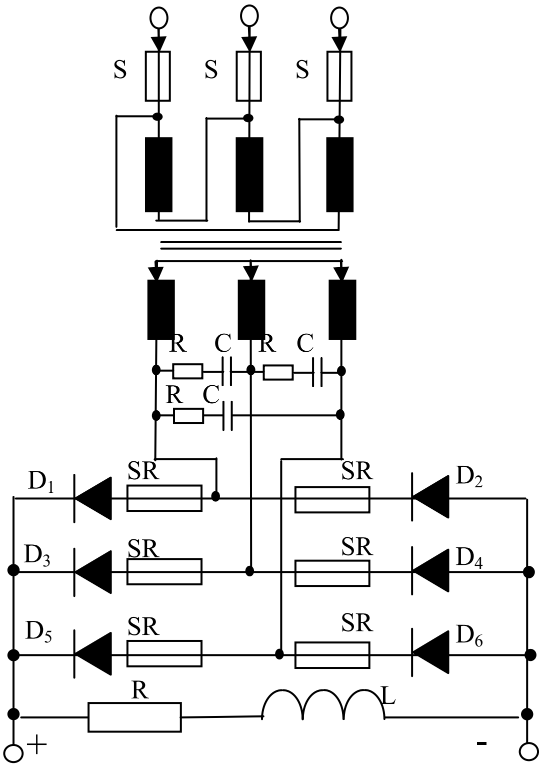


Figure 7. The scheme of a diodes bridge rectifier

A. Qualitative evaluation

For the qualitative analysis of the faults, the fault tree is developed, based on three symptoms, considered to be the most frequent ones during the operation of the power rectifiers: absence of the output voltage (S_1); low level of the output voltage (S_2); high level of the output voltage (S_3).

For diodes bridge rectifier the different faults and their possible causes are analyzed [6], as follows:

S_1 - Absence of the output voltage and possible causes: broken connection to the grid (C_{11}); broken fuses at input (C_{12}); transformer in fault (C_{13}); all fuses broken or all diodes interrupted (C_{14}); failure of one or two phases (C_{15}).

S_2 - Low level of the output voltage: absence of power on one phase (C_{21}); one fuse is broken (C_{22}); one diode is interrupted (C_{23}); random voltage oscillations (C_{24}).

S_3 - High level of the output voltage: grid voltage is higher than the rated one (C_{31}); the load operates as generator (C_{32}); voltage resonance (C_{33}); random voltage oscillations (C_{24}).

The causes which produce a fault can be determined by using the strategy called back linkage. The method consists in identifying the causes which produced a fault, starting from the symptoms [16], [17].

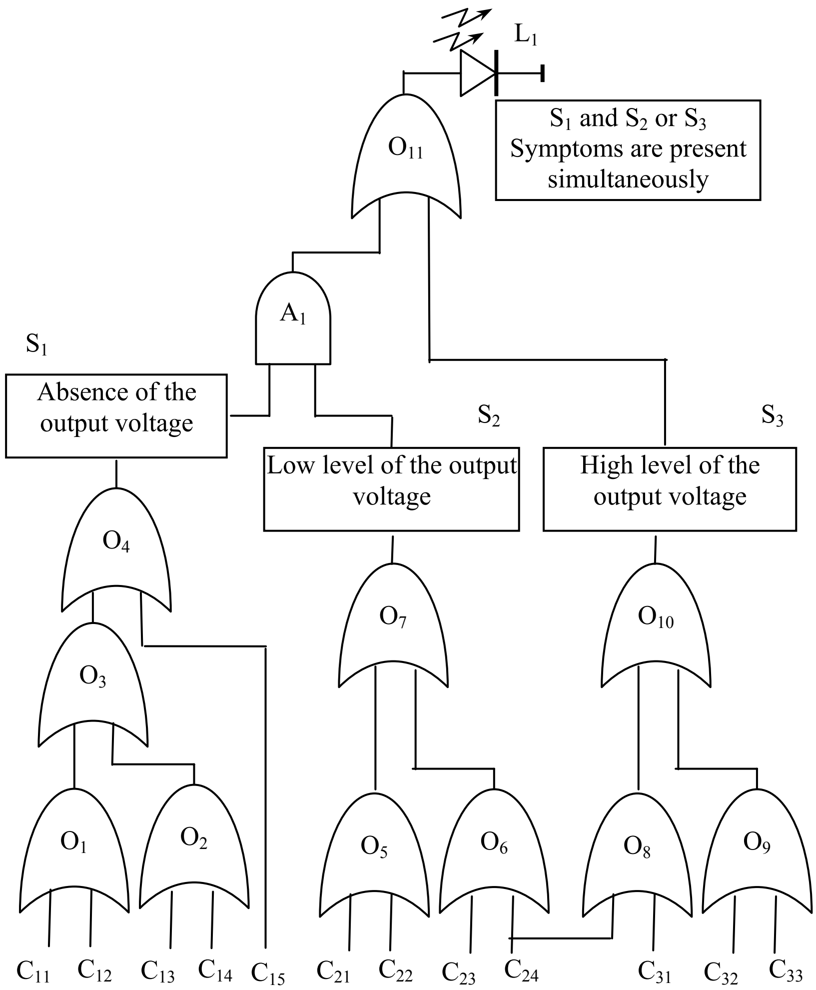


Figure 8. Fault tree of the symptoms S_1 and S_2 or S_3

For example, the symptom S_1 “absence of the output voltage” has as causes: “broken connection to the grid” or “broken fuses at input” or “transformer in fault” or “all fuses broken or all diodes interrupted” or “failure of one or two phases”. In order to identify the cause which produced the fault, other “facts” must be considered as: “supplying cable in good shape”, “all fuses and all diodes are new”, “all input fuses are new”.

For the analyzed case, the fault tree is developed for all the three nominated symptoms. The three symptoms can occur as independent events or simultaneously. In this last case, the identification of the causes which produced faults is a laborious operation.

The paper intends to analyze the following case: symptoms are present *simultaneously,* absence of the output voltage (S_1) and low level of the output voltage (S_2) or high level of the output voltage (S_3).

Based on the faults and their possible causes, the fault tree of the diagnosis system was developed being the one depicted in Fig. 8 [23], [24].

The implementation of the fault tree is performed with logic gates. Each possible fault which influences the considered critical event is represented by a source. The logic 1 of each source means existence of the corresponding fault [11]-[15].

In order to reduce the true table of the tree corresponding to the considered fault, an expert system was developed, by using the programming language CLIPS [22]. The application will exemplify the use of the most usual procedures available in CLIPS software and the interesting possibility to integrate them with the rules.

The specific algorithm developed in CLIPS language simplifies the table of truth for a logical complex circuit with more inputs (sources) and outputs.

By using the Gray code, all possible combinations of inputs are iterated. By using the Gray code, only one source is modified at each step, in order to determine the answer in the table of decisions (by using the Gray code, the execution time is minimized).

During the determination of the responses, a rule checks if two sets of inputs which are different by a single input determines the same answer. If YES, this single input can be replaced by „*” (it signifies that the value of that input has no importance for obtaining the same answer).

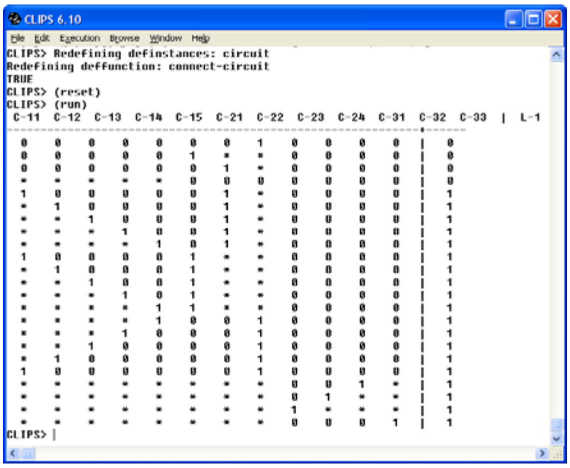
The results obtained following the program running highlight important simplification of the true table. The 2^{12} (4096) possible combinations are reduced to 23 distinct ones (Fig. 9), the execution time being 26.77s.

One notice that there are four cases when, even some of the causes exist, the considered fault does not arises.

If we consider the simultaneous occurrence of the symptoms S_1 and S_2 or S_3, in order to identify the causes which determined the arising of this fault, other facts (events) must be also taken into consideration: “supplying cable in good shape”, “all input fuses are new”, “all ultra fast fuses are new”, “all diodes are new”.

The evaluation of the fault probability of a system is an analyze technique used for the computation of the probability that a certain combination of events which determine the system fault has to occur. Generally, in this evaluation, several hypotheses are considered:

- the hypothesis of the independency of the elements’ faults;
- the hypothesis of the constant intensity of the elements’ faults.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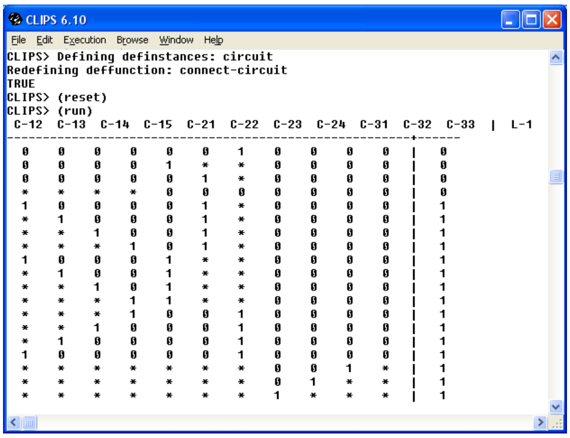
CLIPS 6.10
File Edit Execution Browse Window Help
CLIPS> Redefining definstances: circuit
Redefining deffunction: connect-circuit
TRUE
CLIPS> (reset)
CLIPS> (run)
 C-11  C-12  C-13  C-14  C-15  C-21  C-22  C-23  C-24  C-31  C-32  C-33  |  L-1
--------------------------------------------------------------------+------
  0     0     0     0     0     0     0     1     0     0     0     0   |   0
  0     0     0     0     0     1     *     *     0     0     0     0   |   0
  0     0     0     0     0     0     1     *     0     0     0     0   |   0
  *     *     *     *     *     0     0     0     0     0     0     0   |   0
  1     0     0     0     0     0     1     *     0     0     0     0   |   1
  *     1     0     0     0     0     1     *     0     0     0     0   |   1
  *     *     1     0     0     0     1     *     0     0     0     0   |   1
  *     *     *     1     0     0     1     *     0     0     0     0   |   1
  *     *     *     *     1     0     1     *     0     0     0     0   |   1
  1     0     0     0     0     1     *     *     0     0     0     0   |   1
  *     1     0     0     0     1     *     *     0     0     0     0   |   1
  *     *     1     0     0     1     *     *     0     0     0     0   |   1
  *     *     *     1     0     1     *     *     0     0     0     0   |   1
  *     *     *     *     1     1     *     *     0     0     0     0   |   1
  *     *     *     *     1     0     0     1     0     0     0     0   |   1
  *     *     *     1     0     0     0     1     0     0     0     0   |   1
  *     *     1     0     0     0     0     1     0     0     0     0   |   1
  *     1     0     0     0     0     0     1     0     0     0     0   |   1
  1     0     0     0     0     0     0     1     0     0     0     0   |   1
  *     *     *     *     *     *     *     *     0     0     1     *   |   1
  *     *     *     *     *     *     *     *     0     1     *     *   |   1
  *     *     *     *     *     *     *     *     1     *     *     *   |   1
  *     *     *     *     *     *     *     *     0     0     0     1   |   1
CLIPS>
```

Figure 9. The results of the program running

The developed experimental diagnosis system introduces important simplifications which bypasses the first hypothesis. Thus, the presented system analyses all the possible situations by considering that all the causes which can determine a certain fault are present. The information obtained from the equipment which is the subject of diagnosis can eliminate some causes and consequently determine the response time of the diagnosis system.

The system was filled up with an equipment which collects information concerning the supplying cable state. If the cable is not interrupted, the result obtained from the expert system is the one presented in Fig. 10.

In this case 2^{11} (2048) possible combinations are analyzed, finally being presented 20 variants. The execution time is a little greater than 10s.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CLIPS 6.10
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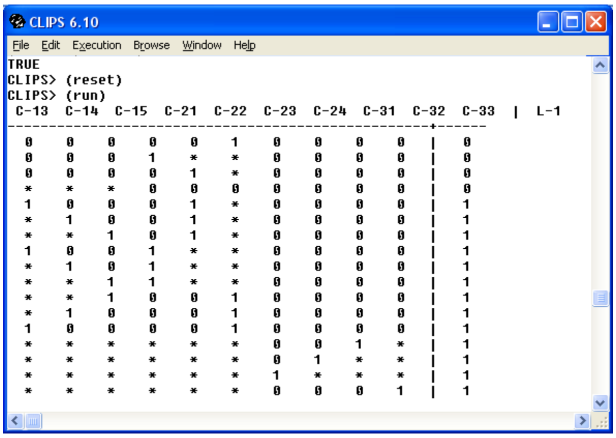
Redefining deffunction: connect-circuit
TRUE
CLIPS> (reset)
CLIPS> (run)
 C-12  C-13  C-14  C-15  C-21  C-22  C-23  C-24  C-31  C-32  C-33  |  L-1
--------------------------------------------------------------+------
  0     0     0     0     0     0     1     0     0     0     0   |   0
  0     0     0     0     1     *     *     0     0     0     0   |   0
  0     0     0     0     0     1     *     0     0     0     0   |   0
  *     *     *     *     0     0     0     0     0     0     0   |   0
  1     0     0     0     0     1     *     0     0     0     0   |   1
  *     1     0     0     0     1     *     0     0     0     0   |   1
  *     *     1     0     0     1     *     0     0     0     0   |   1
  *     *     *     1     0     1     *     0     0     0     0   |   1
  1     0     0     0     1     *     *     0     0     0     0   |   1
  *     1     0     0     1     *     *     0     0     0     0   |   1
  *     *     1     0     1     *     *     0     0     0     0   |   1
  *     *     *     1     1     *     *     0     0     0     0   |   1
  *     *     *     1     0     0     1     0     0     0     0   |   1
  *     *     1     0     0     0     1     0     0     0     0   |   1
  *     1     0     0     0     0     1     0     0     0     0   |   1
  1     0     0     0     0     0     1     0     0     0     0   |   1
  *     *     *     *     *     *     *     0     0     1     *   |   1
  *     *     *     *     *     *     *     0     1     *     *   |   1
  *     *     *     *     *     *     *     1     *     *     *   |   1
```

Figure 10. The result of the system if the supplying cable is in good shape

If additional information is added, such about the new input fuses, the system response is much simplified. The 2^{10} (1024) possible combinations are reduced to the 17 distinct combinations presented in Fig.11. The execution time in this case is less than 4s.



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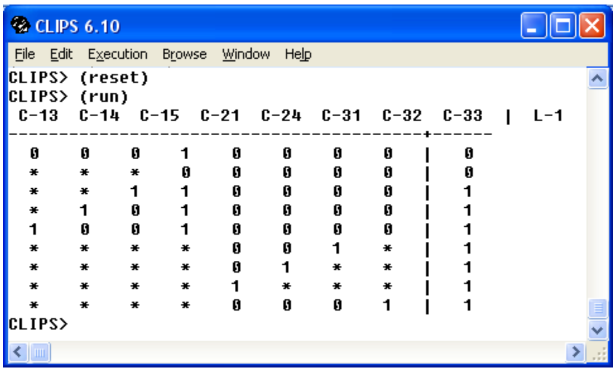
CLIPS 6.10
File Edit Execution Browse Window Help
TRUE
CLIPS> (reset)
CLIPS> (run)
 C-13  C-14  C-15  C-21  C-22  C-23  C-24  C-31  C-32  C-33  |  L-1
---------------------------------------------------------+------
  0     0     0     0     0     1     0     0     0     0    |   0
  0     0     0     1     *     *     0     0     0     0    |   0
  0     0     0     0     1     *     0     0     0     0    |   0
  *     *     *     0     0     0     0     0     0     0    |   0
  1     0     0     0     1     *     0     0     0     0    |   1
  *     1     0     0     1     *     0     0     0     0    |   1
  *     *     1     0     1     *     0     0     0     0    |   1
  1     0     0     1     *     *     0     0     0     0    |   1
  *     1     0     1     *     *     0     0     0     0    |   1
  *     *     1     1     *     *     0     0     0     0    |   1
  *     *     1     0     0     1     0     0     0     0    |   1
  *     1     0     0     0     1     0     0     0     0    |   1
  1     0     0     0     0     1     0     0     0     0    |   1
  *     *     *     *     *     *     0     0     1     *    |   1
  *     *     *     *     *     *     0     1     *     *    |   1
  *     *     *     *     *     *     1     *     *     *    |   1
  *     *     *     *     *     *     0     0     0     1    |   1
```

Figure 11. The result of the system if the input fuses are new

If we consider the simultaneous occurrence of the symptoms S_1 and S_2 or S_3, in order to identify the causes which determined the arising of this fault, other facts (events) must be taken into consideration: "supplying cable in good shape", "all input fuses are new", "all ultra fast fuses are new", "all diodes are new" (Fig.12). The execution time in this case is less than 1s (0.47s).



```
CLIPS 6.10
File Edit Execution Browse Window Help
CLIPS> (reset)
CLIPS> (run)
 C-13  C-14  C-15  C-21  C-24  C-31  C-32  C-33  |  L-1
---------------------------------------------+------
  0     0     0     1     0     0     0     0    |   0
  *     *     *     0     0     0     0     0    |   0
  *     *     1     1     0     0     0     0    |   1
  *     1     0     1     0     0     0     0    |   1
  1     0     0     1     0     0     0     0    |   1
  *     *     *     *     0     0     1     *    |   1
  *     *     *     *     0     1     *     *    |   1
  *     *     *     *     1     *     *     *    |   1
  *     *     *     *     0     0     0     1    |   1
CLIPS>
```

Figure 12. Results of the program, taking into account additional events

One notice that the analyzed fault occurs no matter the causes: "transformer in fault" (C_{13}); "all fuses broken or all diodes interrupted" (C_{14}); "failure of one or two phases" (C_{15}) and absence of power one phase (C_{21}).

The qualitative analysis performed by using the experimental diagnosis system give useful information for the identification of the causes which produced a certain fault, based on the symptoms which occur when a particular fault appears. In addition, the expert system takes into account additional information concerning the equipment state. Hereby the response time is significantly reduced thanks to elimination of certain combinations.

B. *Quantitative evaluation of the fault tree*

The aim is to make available the information concerning the causes which have determined a certain fault, as complete as possible, in order to eliminate the causes. In line with this purpose, the proposed diagnosis system also performs a quantitative analysis of the fault tree for each considered critical event.

For achieving this function, the causes' occurrence probabilities of each critical event are considered. Depending on the propagation path through the logic gates of the fault tree, the probability of occurrence of each critical event is determined.

The structural logic function is:

$$E_{cr} = f_l\left(E_1, E_2, ..., E_i, ...E_n\right) , \quad (1)$$

where,

E_{cr} is the critical event of the system, expressed in terms of the primary events E_i (i=1, 2,…,n), considered as independent between them.

Starting from the logic function (1) it can be expressed the algebraic one:

$$E_{cr} = \mathrm{B}_a\left(E_1, E_2, ..., E_i, ...E_n\right) \quad (2)$$

Even the method described above is systematic, it is quite complex because it requires writing and processing the structural function corresponding to the fault tree of the analyzed system.

For the analyzed fault tree, (2) becomes:

$$S_{cr} = \mathrm{B}_a(C_{11}, C_{12}, C_{13}, C_{14}, C_{15}, ... \\ C_{21}, C_{22}, C_{23}, C_{24}, C_{31}, C_{32}, C_{33}), \quad (3)$$

In order to avoid writing the relatively complex structure function, in practice the probability of the critical event occurrence is written step by step, starting from the basic levels of the primary events and continuing toward the critical event.

Following will be presented the relations which allow to highlight the propagation of the tree events by the way of the fundamental logic gates (AND, OR) [25].

For a two inputs AND gate, we have:

$$P(1 \cap 2) = P(1) \cdot P(2) \quad (4)$$

For a two inputs OR gate, we have:

$$P(1 \cup 2) = P(1) + P(2) - P(1) \cdot P(2) \quad (5)$$

For small enough fault probabilities (in practice $P<10^{-2}$, which is quite usual), it can be used the approximate expression:

$$P(1 \cup 2) = P(1) + P(2) \quad (6)$$

In order to quantitatively analyze the tree from Fig. 8, it is better to avoid writing the structural logic function, because it would be too difficult to process it. The probability of occurrence of the critical event can be evaluated by computing step by step, considering the equation (4) and (6).

This approach is presented in Fig. 11, where is computed the probability of occurrence of the critical event (S_1 and S_2 or S_3), staring from the probabilities of occurrence of the primary events. The initial data for the probabilities of the primary events can be obtained from the datasheets of the components.

IV. Conclusion

This paper presents applications of the diagnosis system which, in first instance monitors, analyzes and transmits a result concerning the state of the devices within an inverter transistors bridge and in the second instance diagnosis a power rectifiers.

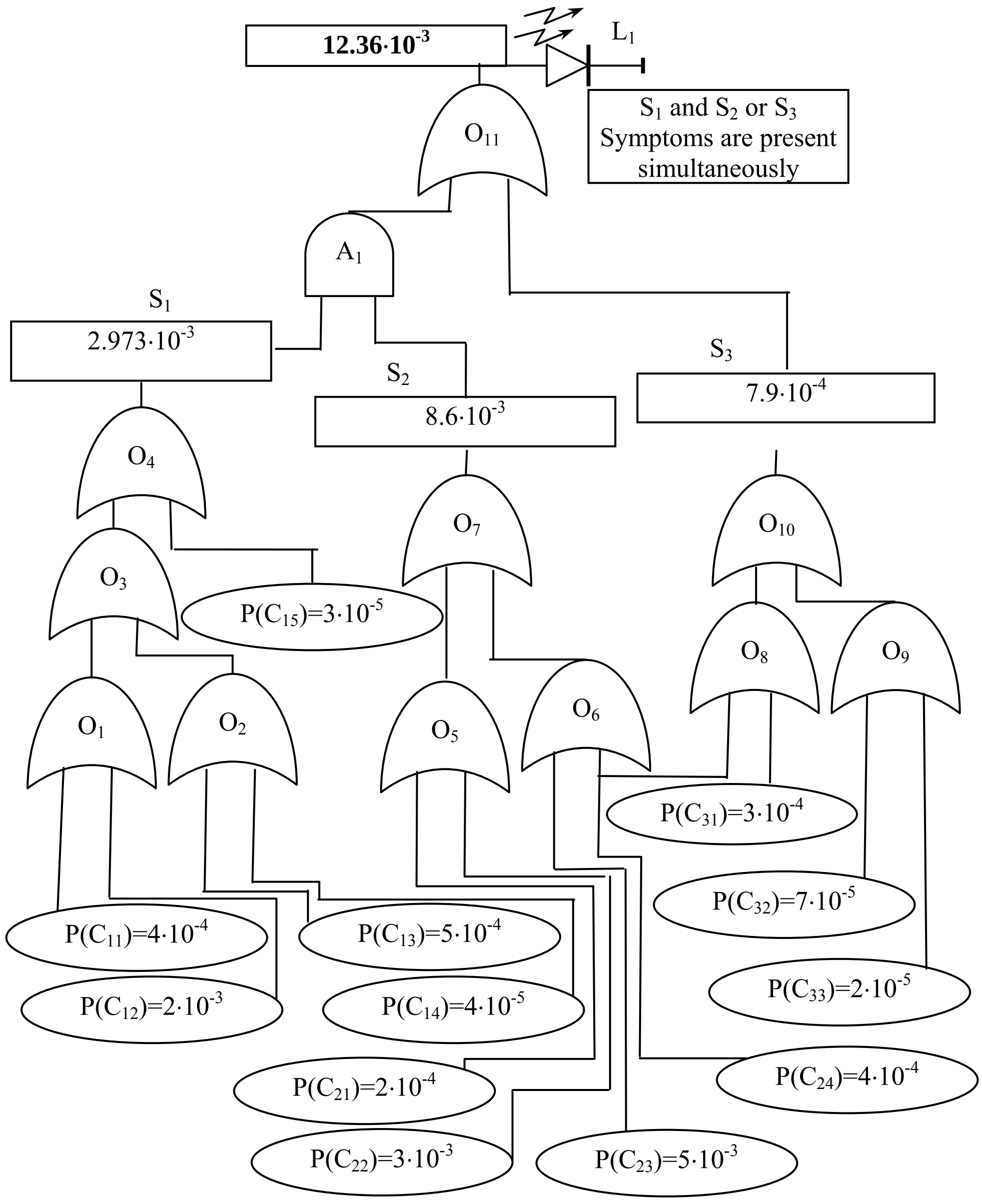


Figure 13. The fault tree for calculate the probability of occurrence of the critical event

The developed experimental system for inverter's diagnosis operates on-line and takes decisions in real time for elimination of the devices in fault.

In order to achieve the result, quantitative and qualitative evaluation of the fault tree is used. The results of the program running highlight important simplification of the true table.

In addition, the experimental system combines the advantages of the fault tree method, generally used for systems reliability analysis, with the performances of CLIPS software, which is probably the most used tool for the expert system, thank to its speed and efficiency. In addition, it is free and incorporates a programming language completely object oriented.

Further, the fault tree is used in systems analysis for computing the probability of a critical event occurrence. This can be performed even by writing the relatively complex structure function, or by writing it step by step, starting from the base levels, considering the probability of occurrence of the primary events and continuing toward the critical event. The second approach is presented in the paper.

The diagnosis system of the inverter is useful for the redundant systems, but also for the non redundant systems, for the maintenance activity.

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