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An anti-harmonic MDLL for phase-aligned on-chip clock multiplication

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Abstract: This paper presents a new anti-harmonic fractional-ratio multiplying delay-locked loop (FMDLL) based clock frequency multiplier for phase aligned on-chip clock generation. With the adoption of a new harmonic lock detector (HLD), the proposed FMDLL solves the harmonic lock problem in conventional MDLLs. The proposed FMDLL is capable of multiplying the input clock with fractional ratio (= N/M), unlike the traditional MDLL which can only multiply with integer ratio (= N). With the new FMDLL, it is possible to quickly change the output frequency or the multiplication factors during operation without a reset. Fabricated in a 65-nm CMOS process, the harmonic-free FMDLL occupies an active area of 0.013 mm^2, operates from 2 GHz to 4 GHz with programmable ratios of N/M, where N = 4, 5, 8, 10 and M = 1, 2, 3. At 4 GHz with N/M = 10/1, the measured p-p output clock jitter and RMS jitter are 25.6 ps and 2.62 ps, respectively. The proposed FMDLL consumes 7.16 mW at 4 GHz.

Keywords: multiplying delay-locked loop, MDLL, frequency multiplier, clock generation, clock multiplication

Classification: Integrated circuits

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1 Introduction

Today, most digital system-on-a-chip (SoCs) are designed with on-chip clock generators that have dynamic frequency scaling (DFS) capability for low power and high performance operations. These clock generators usually employ a phase-locked loop (PLL) circuit for providing high frequency clock signals from a lower frequency external source. To achieve N times frequency multiplication, a typical PLL circuit consists of a voltage controlled oscillator (VCO), a phase detector, a loop filter, a charge pump, and a divide-by-N frequency divider. The characteristics of the analog components of PLLs make it difficult to design and to cope with process changes.

Multiplying delay-locked loops (MDLLs) [1, 2, 3, 4, 5, 6, 7, 8] have recently been introduced as a replacement for PLL-based clock multipliers in some applications. A typical MDLL generates an output clock frequency that is N times the input clock frequency, based on a ring oscillator that periodically switches back and forth from being in open-loop and closed-loop. Due to the clean external clock that comes periodically every N clock cycles, the MDLL has less accumulated jitter than PLLs, and therefore, better jitter characteristics can be obtained.

However, most conventional MDLLs have a harmonic lock problem which may produce output clock frequencies that are different from the target frequency when the initial output frequency is lower than the desired target frequency [8]. Although [8] adopted harmonic lock detectors to avoid the problem of harmonic locking, both have large power and area overhead. Also, [8] can only provide integer-ratio (= N) frequency multiplication, which limits their applications when fractional-ratio multiplication is required. Although [9] was introduced because its 3-to-1 MUX based simple architecture is capable of providing frequency resolution of N/M, the harmonic lock problem still exists.

To illustrate the harmonic lock problem, Fig. 1(a) shows the block diagram of a traditional MDLL [2]. Ideally, the output frequency of the MDLL is N times of the input clock frequency, $f_{OUT} = N \times f_{IN}$. As shown on the left of Fig. 1(b), when the $(N+1)^{th}$ rising edge of CLK_{OUT} comes earlier than the ideal locking point A

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(= the second rising edge of CLK_{IN}) in the initial operation, the output CLK_{OUT} is ideally N (= 4) times the frequency of CLK_{IN} and is synchronized to CLK_{IN} in zero phase with no phase difference after locking. However, as shown on the right of Fig. 1(b), if the initial propagation delay of the VCDL is large and therefore the $(N+1)^{th}$ rising edge of CLK_{OUT} comes later than the ideal locking point A, the CLKout will be synchronized to the harmonic locking point B, so that the frequency of the CLKout has the wrong value of $N/2 \times f_{IN} = 2 \times f_{IN}$ instead of $N \times f_{IN.} = 4 \times f_{IN}$ after locking, where N = 4 in this example.

As can be seen in this example, in order to avoid harmonic locks, conventional MDLLs place a minimum delay constraint on the VCDL at the beginning of the operation. This constraint on the initial VCDL delay increases the locking time. Worst of all, this initial minimum delay requirement makes it impossible to change the input frequency of the MDLL from low to high frequency during operation [7, 8].

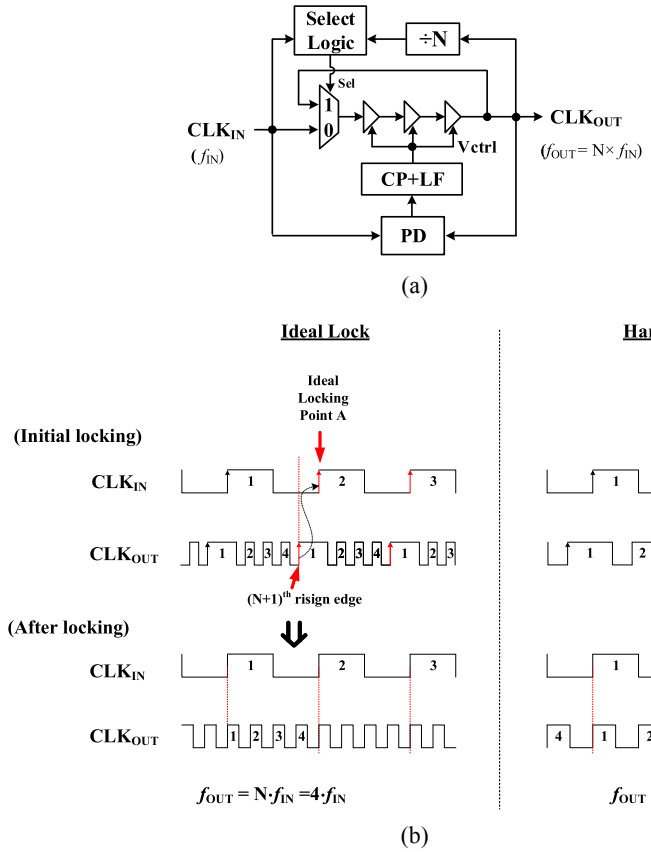

Fig. 1. (a) Block diagram of conventional MDLL (b) Harmonic lock problems in conventional MDLLs

In this paper, we propose a new anti-harmonic lock, fractional-ratio MDLL (FMDLL) clock frequency multiplier that solves the harmonic lock problem in conventional MDLLs. The proposed FMDLL is capable of multiplying the input clock with fractional ratio (= N/M), unlike the traditional MDLL which can only multiply with integer ratio (= N) [9]. Also, the proposed FMDLL clock multiplier has the ability to align or de-skew phases with which the skew between the output clock and the input clock can be removed. Furthermore, with the addition of a new

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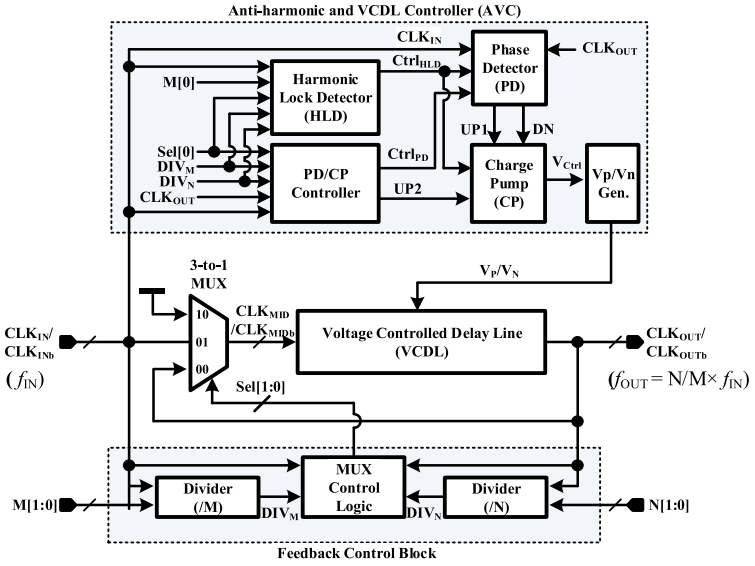
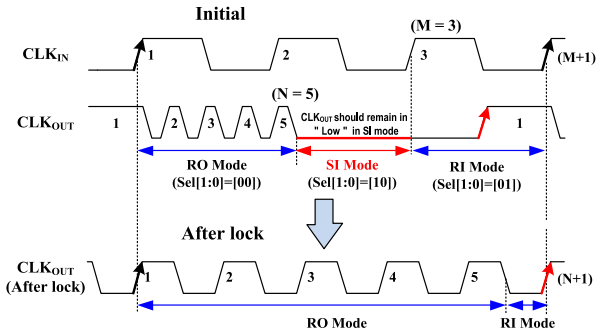
harmonic lock detector, it is possible to change also the input/output frequency and the frequency multiplication factors (N, M) during operation without the need to reset. Recently, a fractional-N MDLL [10] employing dual digital-to-time (DTC) converters paths for clock injection has been introduced for applications in RF systems. However, [10] has a very large area overhead due to its complex structure and the harmonic lock problem was not considered either. The main area of application for the proposed FMDLL is low-power digital VLSI design using DFS for power reduction. Hence, comparisons with complex fractional-N MDLLs for RF systems have been omitted in this paper.

The contents of the paper are organized in the following way. In section 2, the architecture of the proposed harmonic-free MDLL clock frequency synthesizer is described. The measurement results are described in Section 3. Finally, the conclusions are summarized in Section 4.



(a)



(b)

Fig. 2. (a) Proposed anti-harmonic fractional-ratio MDLL (FMDLL) clock frequency multiplier (b) locking operation

2 Circuit design

Fig. 2(a) shows a block diagram of the proposed anti-harmonic FMDLL clock frequency multiplier. It consists of a 3-to-1 multiplexer (MUX), a voltage-con-

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trolled delay line (VCDL), a feedback control block, and an anti-harmonic and VCDL controller (AVC). The feedback control block includes two programmable frequency dividers /M and /N, where M and N are integer and programmable. The proposed FMDLL provides phased aligned and multiplied fractional-ratio output clock $f_{OUT} = N/M \times f_{IN}$. The AVC includes a harmonic lock detector (HLD), a phased detector (PD), a dual-path charge pump (CP), a Vp/Vn generator, and a PD/CP controller. The feedback control block comprises a MUX control logic, an input frequency divider (÷M), and a feedback side frequency divider (÷N). When compared to the phase detection and control block of [9], the proposed AVC employs a new HLD to detect and correct harmonic lock situation and achieves a faster locking time through the adoption of a new PD/CP controller and a dual-path CP. The proposed FMDLL architecture has three operating modes: the ring oscillator (RO) mode, the reference injection (RI) mode, and the supply injection (SI) mode [9]. Depending on the Sel[1:0] signals of the MUX control logic, the output of the MUX (CLK_{MID}) is selected from among three inputs: CLK_{IN} when Sel[1:0] = [01] in RI mode, CLK_{OUT} when Sel[1:0] = [00] in RO mode, and the supply voltage when Sel[1:0] = [10] in SI mode.

Fig. 2(b) shows the detailed locking operation. The proposed FMDLL starts at RO mode. Here we assume that M = 3 and N = 5 as an example. At this moment, the N^{th} rising edge of CLK_{OUT} comes earlier than the M^{th} rising edge of CLK_{IN}. In order to achieve N/M frequency multiplication with zero skew, the RO mode is finished after the N^{th} rising edge of CLK_{OUT}, and the SI mode is enabled to make the CLK_{OUT} remain in low state. This SI mode is maintained until the M^{th} rising edge of CLK_{IN}. Then the FMDLL enters the RI mode, injecting the clean edge of CLK_{IN}. This operating mode transition from RO → SI → RI is repeated at every M reference cycle until the VCDL delay is increased to reach the moment when the N^{th} rising edge of CLK_{OUT} comes after the M^{th} rising edge of CLK_{IN}.

After locking, the $(N+1)^{th}$ rising edge of CLK_{OUT} is aligned with the $(M+1)^{th}$ rising edge of CLK_{IN} without skew, and the mode transition from RO → RI repeats at every M reference input cycle.

Fig. 3 shows the building blocks of the proposed FMDLL. Fig. 3(a) shows the VCDL, which consists of a 2-stage current-starved inverter based pseudo-differential delay cell and a buffer stage. Fig. 3(b) shows the simplified schematic of the dual-path charge pump (CP) which generates the Vctrl signal. The Vctrl signal is then used to generate the V_P and V_N signals through the V_P/V_N generator. The CP consists of dual current paths. The first path is used for regular locking and the second path can be turned on for both fast locking and rectifying harmonic lock situations. The propagation delay of the delay cell is controlled by the V_P and V_N signals. At the beginning of the operation, the proposed VCDL operates with the minimum delay, so the FMDLL starts at the highest operating frequency. As the level of Vctrl rises, the V_N signal is lowered and the V_P signal is elevated, increasing the VCDL propagation delay. The linear operating frequency range of the VCDL is from 1 GHz to 4 GHz.

Fig. 4 displays the other building blocks. Fig. 4(a) shows the phase detector (PD). When the $Ctrl_{PD}$ signal is high, the PD is enabled and it compares the two input clock signals, CLK_{IN} and CLK_{OUT}, to generate the two CP control signals,

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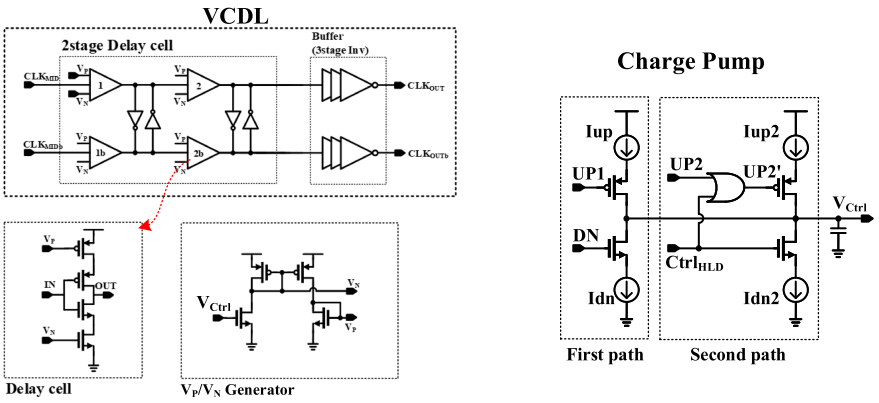

Fig. 3. Building blocks: (a) VCDL and Vp/Vn Generator (b) Simplified dual-path CP

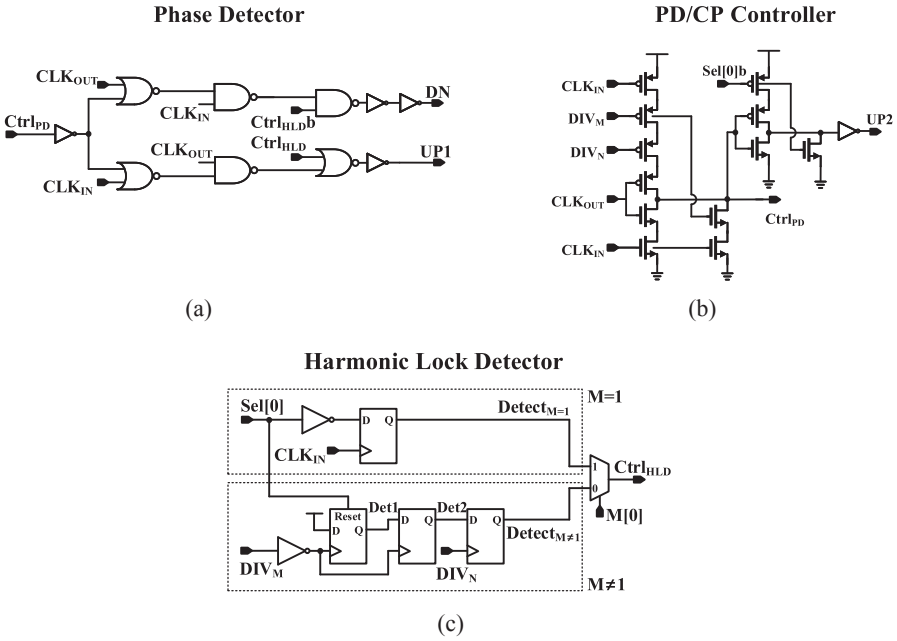

Fig. 4. Building blocks: (a) PD (b) PD/CP controller (c) HLD

UP1 and DN. The PD/CP controller, shown in Fig. 4(b), generates the two control signals, $Ctrl_{PD}$ and UP2. The $Ctrl_{PD}$ signal becomes high when all the CLK_{IN}, CLK_{OUT}, DIV_N, and DIV_M signals are low. The UP2 signal enables fast locking by turning on the fast charging path (Iup2) of the CP. The UP2 pulse changes from high to low when $Ctrl_{PD}$ is low and Sel[0] becomes high. Then the UP2 pulse changes from low to high again when the $Ctrl_{PD}$ signal becomes high. The harmonic lock detector (HLD) is shown in Fig. 4(c). When the harmonic lock situation is detected, the HLD changes the $Ctrl_{HLD}$ signal from low to high. The harmonic lock situation can be detected by monitoring the Sel[0], DIV_N, and DIV_M signals. In Fig. 4(c), if the frequency division factor M = 1, then the upper block is enabled, otherwise, the lower block is enabled.

Fig. 5 illustrates the simplified locking process of the proposed FMDLL showing the detection and correction of harmonic lock for the case when

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N/M = 10/3. For normal operation, since M = 3 in this case, the operating mode of the MDLL must change sequentially from RO → SI → RI by the end of the third input cycle of CLK_{IN}. Therefore, during this interval, the Sel[0] signal must also have a section that changes from low to high. However, as shown in Fig. 5, during this period, the operation mode of the FMDLL abnormally keeps the RO mode, and Sel[0] does not change from the low state. Thus, point A can be a harmonic lock detecting point. At Point A, when Sel [0] is low, Det1 goes high on the first falling edge of DIV_M. At Point B, Det2 goes high on the second falling edge of DIV_M. Then, at the rising edge of DIV_N at point C, $Ctrl_{HLD}$ goes high to detect a harmonic lock situation. The harmonic lock occurs when the initial output frequency is lower than the target frequency. When $Ctrl_{HLD}$ goes high at Point C, the DN signal is activated by the HLD and the CP's discharging path (Idn) is turned on. The Idn current lowers the Vctrl voltage, and the output frequency of the MDLL is forcibly increased during this discharging period. Thus, the proposed FMDLL is able to be released from the harmonic lock.

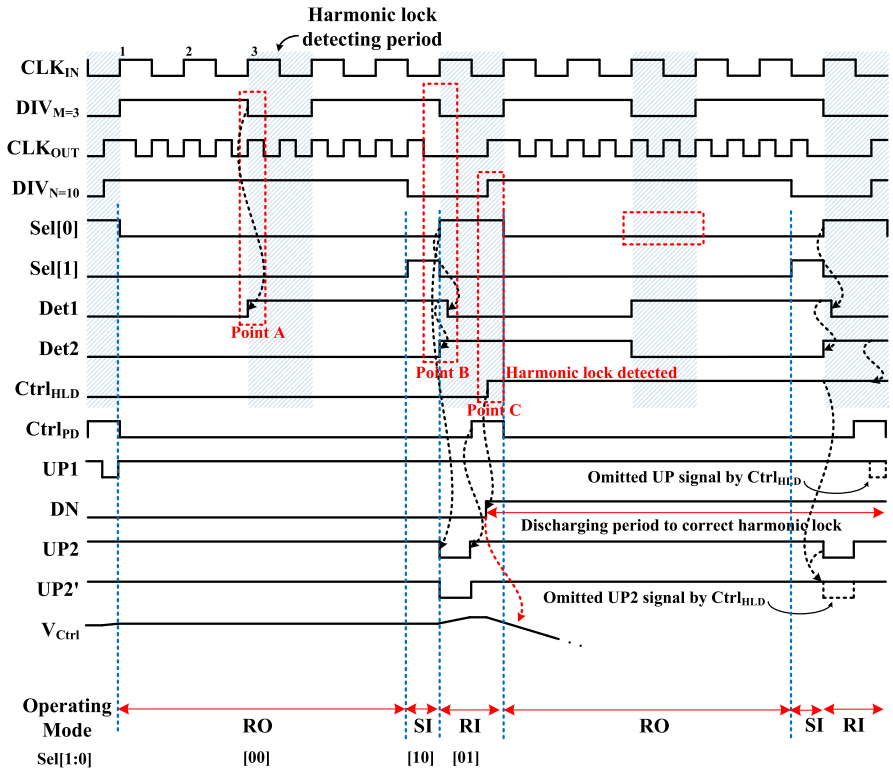

Fig. 5. Simplified locking process of the proposed FMDLL showing the detection and the correction of harmonic lock when N/M = 10/3.

3 Measurement results

The proposed harmonic-free FMDLL is fabricated in TSMC 65 nm CMOS process. Fig. 6(a) displays the die microphotograph and layout of the FMDLL which occupies an active area of only 0.013 mm^2. Fig. 6(b) shows the test chip-on-board (CoB) assembly.

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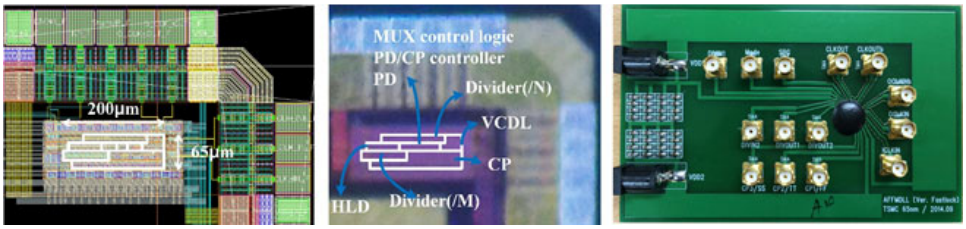
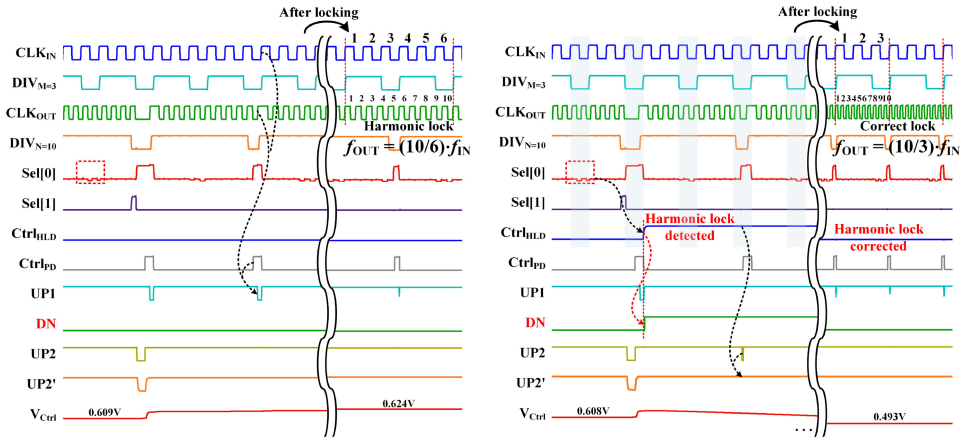


(a) (b)

Fig. 6. (a) Chip layout and die (b) test CoB of the proposed FMDLL



(a) (b)

Fig. 7. Simulated locking process of the proposed FMDLL with N/M = 10/3 (a) when the HLD is not activated, (b) when the HLD is activated.

Fig. 7 is the result of the fractional-ratio (=N/M) frequency multiplication simulation, showing how the locking process works depending on whether the HLD is activated or not. Fig. 7(a) displays the simulation result when the HLD is not activated. Since the frequency multiplication factors are N = 10 and M = 3, respectively, N (= 10) cycles of CLK_{OUT} must be generated during M (= 3) cycles of CLK_{IN} (or one cycle of DIV_M). In Fig. 7(a), however, the initial frequency of CLK_{OUT} is too slow, hence CLK_{OUT} is harmonically synchronized to $2 \times M$ (= 6) cycles of CLK_{IN}. Therefore, the output frequency will have an abnormal $f_{OUT} = N/(2M) \times f_{IN}$ frequency that will be different from the target frequency of $f_{OUT} = N/M \times f_{IN}$.

Fig. 7(b) displays the simulation result when the HLD is activated. Since N = 10 and M = 3, 10 cycles of CLK_{OUT} should be generated for 3 cycles of CLK_{IN}. In the first DIV_M cycle, the Sel[0] signal is monitored to detect the harmonic lock, and in the second DIV_M cycle, the $Ctrl_{HLD}$ signal goes high. As a result, the DN signal becomes high and the CP discharge path is forcibly activated, so that the Vctrl value is lowered and the frequency of the CLK_{OUT} is increased. After locking, it can be confirmed that the frequency of the output CLK_{OUT} has a normal frequency $f_{OUT} = N/M \times f_{IN}$. This simulation result is exactly the same as the harmonic-free fractional-ratio locking process described in Fig. 5.

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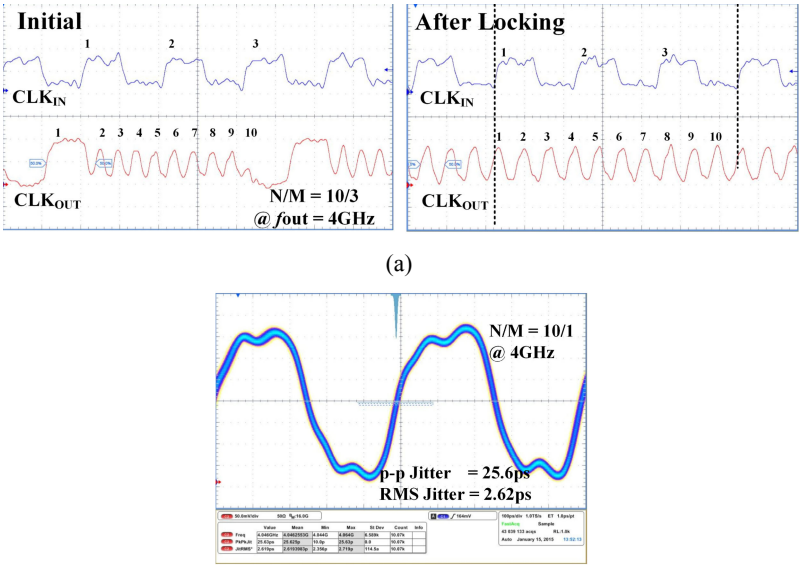

Fig. 8. (a) Measured locking process at 4 GHz with N/M = 10/3 (b) Measured output clock's peak-to-peak jitter with N/M = 10/1 at 4 GHz.

Fig. 8(a) shows measured waveforms of CLK_{IN} and CLK_{OUT} at 4 GHz with fractional-ratio multiplication factor of N/M = 10/3. The figure on the left shows the beginning of the operation. The phase and frequency of CLK_{OUT} are not synchronized to CLK_{IN} yet. The figure on the right shows the operation after locking. The phase and frequency of CLK_{OUT} are well synchronized with CLK_{IN} without any skews, and it can be confirmed that the frequency of CLK_{OUT} is 10/3 times that of CLK_{IN}. Fig. 8(b) shows the measured peak-to-peak (p-p) output clock (CLK_{OUT}) jitter. The p-p jitter of CLK_{OUT} was measured by connecting a 1-m long SMA cable to the CoB shown in Fig. 6(b). At 4 GHz with N/M = 10/1, the measured p-p output clock jitter and RMS jitter are 25.6 ps and 2.62 ps, respectively. The proposed harmonic-free FMDLL consumes 7.16 mW at 4 GHz. The output frequency ranges from 2 GHz to 4 GHz with programmable frequency multiplication ratios of N/M, where N = 4, 5, 8, 10 and M = 1, 2, 3.

Fig. 9 is a simulation result that demonstrate how the proposed FMDLL uses the HLD to freely adjust the output frequency. Fig. 9(a) is a simulation result of continuously increasing or decreasing the input frequency (CLK_{IN}) without resetting. With N/M = 10/3, it can be seen that the frequency of CLK_{OUT} (f_{OUT}) is increased or decreased from 2 GHz to 4 GHz according to changes in Vctrl. Fig. 9(b) is the simulation result of continuously changing the fractional-ratio frequency multiplication factor (N/M) without resetting at CLKin = 1 GHz. From the simulation, it can be seen that the proposed FMDLL quickly locks to the target output frequency within about 300 ns without getting hindered by harmonic lock problems.

Table I compares the proposed harmonic-free FMDLL with state-of-the-art analog MDLL frequency multipliers. Compared with other MDLLs, the proposed FMDLL achieves both small area and low power with the added benefit of the unique harmonic-free fractional-ratio frequency multiplication. Although [8] has

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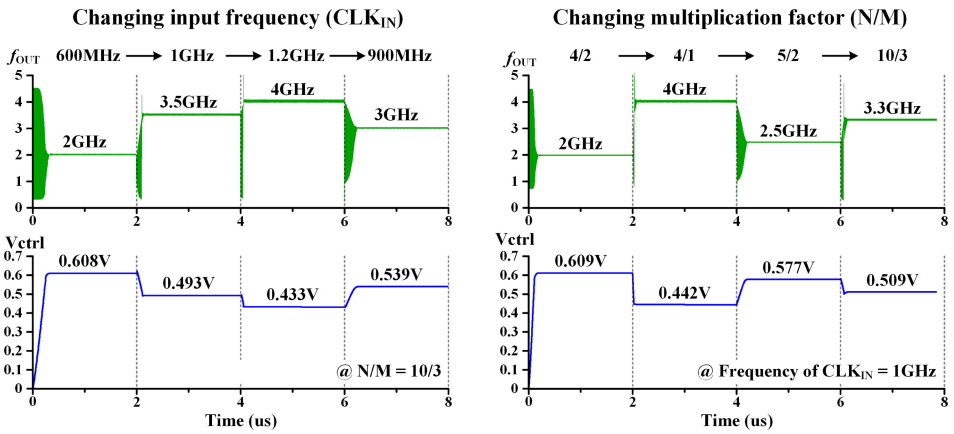

Fig. 9. Simulated FMDLL operation for changing output clock frequency (a) when the frequency of CLK_{IN} is changed, (b) when the frequency multiplication factor (N/M) is changed.

Table I. Performance comparison with state-of-the-art analog MDLLs

	[2] JSSC 02	[5] ISSCC 11	[8] TCAS-II 06	[9] EL 14	This work
Architecture	Analog MDLL	Analog MDLL	Analog MDLL	Analog MDLL	Analog MDLL
Technology	0.18 µm	90 nm	0.18 µm	0.13 µm	65 nm
Supply [V]	1.8	1.2/1.0	1.8	1.2	1.0
Anti-harmonic Capability	X	X	O	X	O
Output Freq. [GHz]	0.2–2	4.6	0.9–2.9	0.85–1.8	2.0–4.0
Multiplication Factor [N]	4,5,8,10	N/A	13–20	4,5,8, 10	4,5,8, 10
Fractional-Ratio Division Capability [M]	X	X	X	O (M = 1,2,3)	O (M = 1,2,3)
Peak-to-peak jitter [ps]	13.11 @2 GHz	17.8@ 4.6 GHz	12.9 @2.16 GHz	27.5 @1.5 GHz	22.2 @4 GHz
RMS jitter [ps] @x-GHz	1.64 @2	2.0 @4.6	-	-	2.28 @4
Power [mW] @x-GHz	12 @2	6 @4.6	19.8 @2.0	9 @1.5	7.16 @4
Chip Area [mm^2]	0.05	0.025	0.07	0.018	0.013

anti-harmonic lock feature, it is incapable of providing phased aligned fractional-ratio frequency multiplication. [9] has fractional-ratio multiplication capability, but it has the problem of harmonic lock problem. Because most of the compared MDLLs have failed to address the harmonic lock problem, there is a limit to how much the output frequency or the division factor can be varied during operation. This makes it difficult to use them for practical applications. However, the advantage of the proposed FMDLL is that the output frequency can be changed

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during operation without the need for a reset. Another merit of the FMDLL is that phase aligned fractional-ratio frequency multiplication is possible.

4 Conclusion

A new anti-harmonic fractional-ratio MDLL frequency multiplier has been presented. The proposed FMDLL takes advantage of a simple structure, has a small area and consumes low power. With the adoption of a new HLD, the proposed FMDLL solves the harmonic lock problem in conventional MDLLs. With the proposed FMDLL, it is possible to quickly change the output frequency or the multiplication factors (N/M) during operation without a reset. The proposed FMDLL achieves de-skewed output clock with programmable N/M multiplication ratios. Therefore, this FMDLL can be very useful as a clock generator IP that requires DFS function.

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