

Energy-efficient, area-efficient, high-accuracy and low-complexity switching scheme for SAR ADC

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Abstract: An energy-efficient, area-efficient, high-accuracy and low-complexity switching scheme for successive approximation register (SAR) analogue-to-digital converter (ADC) is proposed. In the proposed switching scheme, both the first and the second comparisons don't consume switching energy, and all the rest of comparisons consume little switching energy. As a result, the proposed switching scheme achieves a 95.34% switching energy reduction and a 75% area reduction compared with the conventional method. In addition, only the least significant bit (LSB) is depended on the accuracy of V_{cm} . Moreover, only two reference voltages are used for each capacitor, which lowers complexity of digital control logic.

Keywords: SAR ADC, switching scheme, energy-efficient, area-efficient, high-accuracy, low-complexity

Classification: Integrated circuits

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1 Introduction

In recent years, successive-approximation register (SAR) analogue-to-digital converters (ADCs) have been preferred for low-power applications [1, 2, 3]. Among the building blocks in a SAR ADC, a capacitive DAC always consumes a significant part of the total power consumption [3, 4, 5]. Recently, several energy-efficient techniques have been developed to improve the power efficiency of DAC capacitor arrays [6, 7, 8, 9, 10, 11]. Compared to conventional technique [12], Split Capacitor [6], Set-and-down [7], Wang [8], Tri-level [9], VMS [10], Hybrid [11] reduce the switching energy by 37.48%, 81.26%, 90.61%, 96.89%, 97.66% and 98.83%, respectively. Tri-level [9], VMS [10] and Hybrid [11] are great energy efficient with switching energy reduced by more than 95%. However, these schemes [9, 10, 11] have various drawbacks such as very high dependency on the accuracy of the middle reference voltage (V_{cm}) and high-complexity digital control logic. In this Letter, an energy-efficient and area-efficient switching scheme is proposed to reduce dependency on the accuracy of V_{cm} and lower complexity of digital control logic.

2 Proposed switching scheme

To explain the operation of the proposed switching scheme, a 4-bit SAR ADC is used. The operation can be performed in four phases: 1st comparison, 2nd comparison, 3rd to $(N - 1)$ th comparison and N th comparison, as shown in Fig. 1.

1st comparison: the input signal is sampled on the top-plates of all capacitors via sampling switch, with the bottom-plates of the largest capacitors connecting to V_{ref} and other capacitors to gnd . After sampling, the sampling switches are turned off. Then, the comparator performs the first comparison without consuming any switching energy ($E_1 = 0$).

2nd comparison: Once the D_0 (MSB) is obtained, the largest capacitor on the higher voltage potential side is switched to gnd and the other one (on the lower

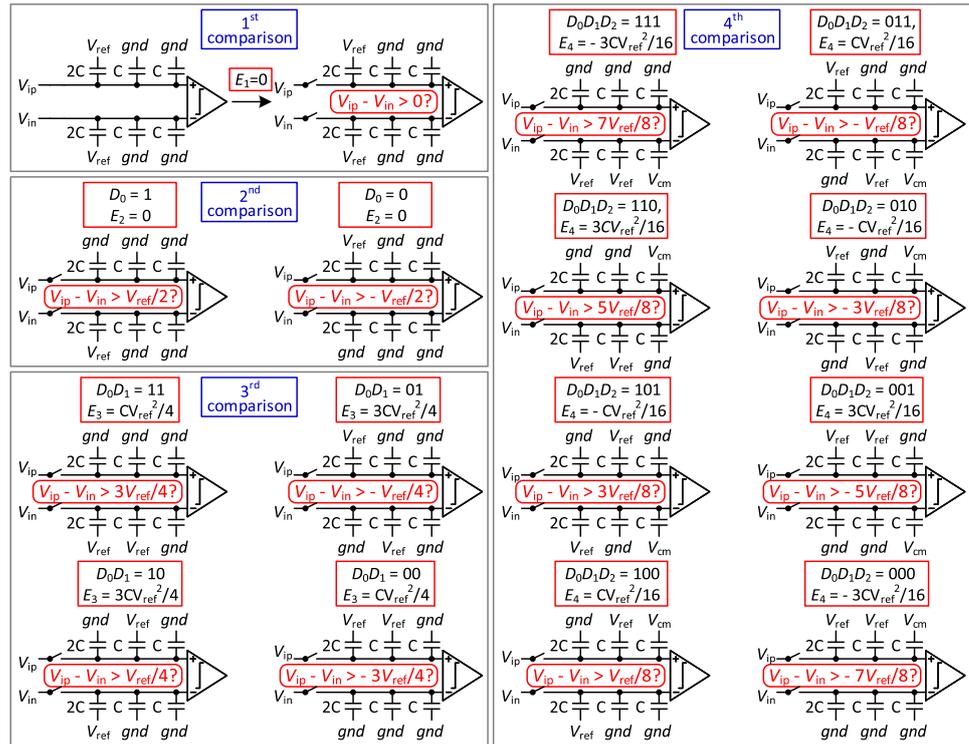


Fig. 1. Switching procedure of 4-bit SAR DAC.

side) remains unchanged. As a result, the voltage of the higher side is decreased by $V_{ref}/2$ without consuming switching energy ($E_2 = 0$). Then, the comparator performs the second comparison.

3^{rd} to $(N - 1)^{th}$ comparison: According to the comparator output, the corresponding capacitor on the lower side is switched from gnd to V_{ref} and the other one (on the higher side) remains unchanged. For example, in the third comparison, the second largest capacitor on the lower side is switched from gnd to V_{ref} while the other one (on the higher side) remains unchanged. The ADC repeats the procedure until the $(N - 1)^{th}$ comparison is completed. During the switching procedure, there is only one capacitor switch for each comparison, resulting in less switching activity and lower energy. Based on the switching energy calculation method in [6], the switching energy of each comparison from 3^{rd} to $(N - 1)^{th}$ is derived as

$$E_i = \left\{ \begin{array}{l} 2^{N-i-1} - 2^{N-2i} - D_{i-2} \sum_{j=1}^{i-2} D_{j-1} 2^{N-j-i-1} \\ -(1 - D_{i-2}) \sum_{j=1}^{i-2} (1 - D_{j-1}) 2^{N-j-i-1} \end{array} \right\} CV_{ref}^2 \quad (1)$$

N^{th} comparison: In the N^{th} comparison, the last capacitor on the lower side is switched from gnd to V_{cm} while the other one (on the higher side) remains unchanged. When $D_0 D_{N-2} = 00$ or 11 , the switching energy in the N^{th} comparison is negative. If the negative value is regarded as zero, the switching energy in the N^{th} comparison is found to be

$$E_N = \left\{ \begin{array}{l} D_0(1 - D_{N-2}) \left[\begin{array}{l} 2^{-2} - 2^{-N} \\ - \sum_{j=1}^{N-2} (1 - D_{j-1})2^{-j-1} \end{array} \right] \\ + (1 - D_0)D_{N-2} \left[\begin{array}{l} 2^{-2} - 2^{-N} \\ - \sum_{j=1}^{N-2} D_{j-1}2^{-j-1} \end{array} \right] \end{array} \right\} CV_{ref}^2 \quad (2)$$

For the case of N -bit resolution, the average switching energy of proposed switching scheme is:

$$E_{average} = \overline{\sum_{D_0 D_1 \dots D_{N-1} = 00 \dots 0}^{11 \dots 1} \left(\sum_{i=1}^N E_i \right)} \quad (3)$$

$$= \begin{cases} 0 & N = 1, 2 \\ (2^{N-4} - 2^{-1} + 2^{-4})CV_{ref}^2 & N \geq 3 \end{cases}$$

For example, when $N = 4$, according to Eq. (3), the average switching energy is:

$$E_{average} = (2^{4-4} - 2^{-1} + 2^{-4})CV_{ref}^2 = 9CV_{ref}^2/16 \quad (4)$$

For Fig. 1, there are 8 switching cases, and the switching energy of each case is as follows:

$$E = \begin{cases} (1/4 + 0)CV_{ref}^2 & D_0 D_1 D_2 = 111 \\ (1/4 + 3/16)CV_{ref}^2 & D_0 D_1 D_2 = 110 \\ (3/4 + 0)CV_{ref}^2 & D_0 D_1 D_2 = 101 \\ (3/4 + 1/16)CV_{ref}^2 & D_0 D_1 D_2 = 100 \\ (3/4 + 1/16)CV_{ref}^2 & D_0 D_1 D_2 = 011 \\ (3/4 + 0)CV_{ref}^2 & D_0 D_1 D_2 = 010 \\ (1/4 + 3/16)CV_{ref}^2 & D_0 D_1 D_2 = 001 \\ (1/4 + 0)CV_{ref}^2 & D_0 D_1 D_2 = 000 \end{cases} \quad (5)$$

The average switching energy is the average of these 8 switching cases:

$$E_{average} = \frac{\left[\begin{array}{l} (1/4 + 0) + (1/4 + 3/16) \\ + (3/4 + 0) + (3/4 + 1/16) \\ + (3/4 + 1/16) + (3/4 + 0) \\ + (1/4 + 3/16) + (1/4 + 0) \end{array} \right] CV_{ref}^2}{8} = 9CV_{ref}^2/16 \quad (6)$$

Therefore, Eq. (3) and Fig. 1 are consistent.

Based on the proposed switching scheme, a N -bit SAR ADC is proposed, as shown in Fig. 2. V_{cm} is used as reference voltage for the last capacitor which is used for the N^{th} comparison, thus reducing the number of unit capacitors by half. Only two reference voltages are required for each capacitor, which results in simple digital control logic and simplifies the design complexity.

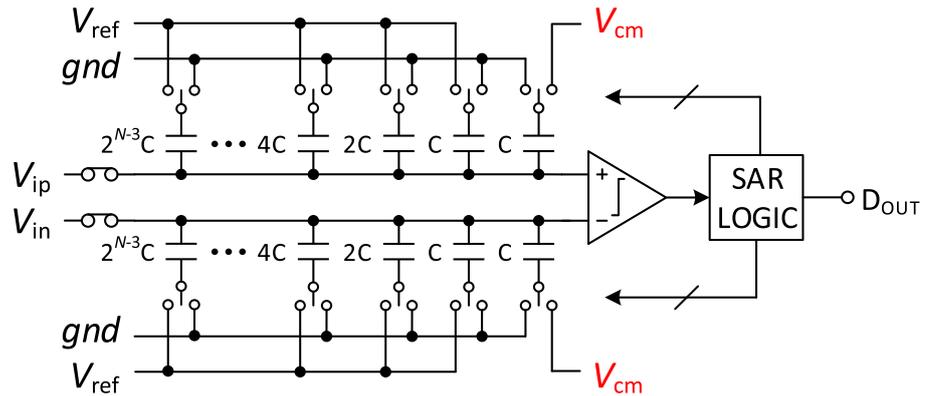


Fig. 2. Architecture of N -bit SAR ADC.

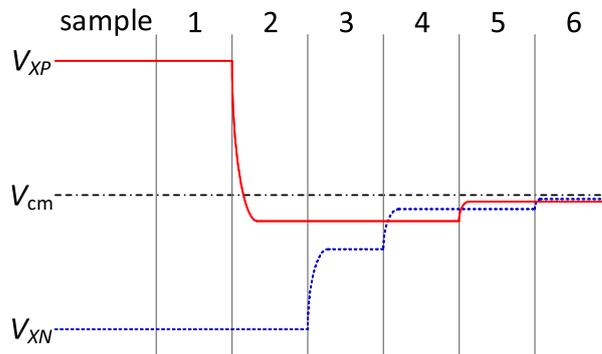


Fig. 3. Waveform of the proposed switching scheme.

Fig. 3 shows the successive approximation waveform of the proposed switching scheme. The common-mode voltage shifts by $V_{ref}/4$ in the second comparison. And then, the common-mode voltage will gradually approach V_{cm} . Because of the change of common-mode voltage of the comparator during bit cycling, high CMRR of the comparator circuit is required.

3 Comparison of switching schemes

The behavioural simulations of several switching schemes for 10-bit SAR ADC are performed in MATLAB. The average switching energy of the proposed switching scheme for 10-bit SAR ADC is $63.56 CV_{ref}^2$ which amounts to a reduction of 95.34% in the switching energy compared with conventional switching scheme [12]. Fig. 4 shows switching energy at each output code for different switching schemes. Table I and Table II show the comparison of several switching schemes for 10-bit SAR ADC. As shown in Table I and Table II, switching schemes [9, 10, 11] show great energy efficiency and area efficiency at the expense of very high dependency on the accuracy of V_{cm} and three reference voltages are required for each capacitor. The use of three voltages for each capacitor makes the digital control logic relatively highly complex. In the proposed switching scheme, only the least significant bit (LSB) is depended on the accuracy of V_{cm} , and moreover, only two reference voltages are used for each capacitor. Furthermore, the common-mode voltage of the proposed switching scheme shifts by $V_{ref}/4$ which is the same as that of VMS [10], and less than those of the switching schemes [6, 7, 8, 9, 11].

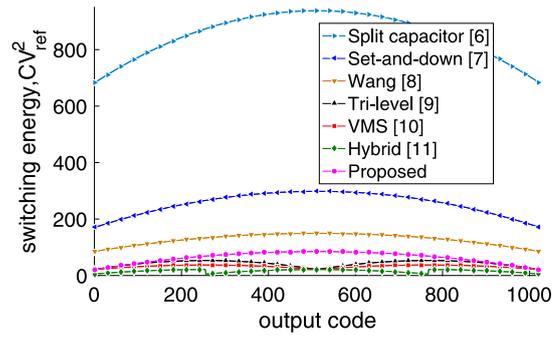


Fig. 4. Switching energy against output codes.

Table I. Comparison of energy saving and area reduction for different switching schemes of a 10-bit SAR ADC

Switching scheme	Average switching energy (CV_{ref}^2)	Energy saving	Number of unit capacitors	Area reduction
Conventional [12]	1363.3	Reference	2048	Reference
Split capacitor [6]	852.3	37.48%	2048	0%
Set-and-down [7]	255.5	81.26%	1024	50%
Wang [8]	128	90.61%	518	74.7%
Tri-level [9]	42.42	96.89%	512	75%
VMS [10]	31.88	97.66%	512	75%
Hybrid [11]	15.88	98.83%	512	75%
Proposed	63.56	95.34%	512	75%

Table II. Comparison of dependency on the accuracy of V_{cm} , logic complexity and common-mode shift for different switching schemes of a 10-bit SAR ADC

Switching scheme	Dependency on the accuracy of V_{cm}	Number of references for each capacitor	Logic complexity	Common-mode shift
Conventional [12]	No	2	Low	0
Split capacitor [6]	No	2	Low	0
Set-and-down [7]	No	2	Low	$V_{ref}/2$
Wang [8]	No	2	Low	$V_{ref}/2$
Tri-level [9]	Very high (all bits except MSB)	3	High	$V_{ref}/2$
VMS [10]	Very high (all bits except MSB)	3	High	$V_{ref}/4$
Hybrid [11]	Very high (all bits except MSB)	3	High	$3V_{ref}/8$
Proposed	Very low (only LSB)	2	Low	$V_{ref}/4$

4 Conclusion

An energy-efficient, area-efficient, high-accuracy and low-complexity switching scheme for SAR ADC is proposed in this Letter. The proposed switching scheme achieves an energy savings of 95.34% and an area reduction of 75% compared with conventional switching scheme. In addition, only the least significant bit (LSB) is depended on the accuracy of V_{cm} , only two reference voltages are used for each capacitor and common-mode voltage shifts by $V_{ref}/4$, resulting in a good trade-off among the energy-efficiency, area-efficiency, accuracy and complexity of the ADC.

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