

# An ultra-low power low cost LDO for UHF RFID tag

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**Abstract:** An ultra-low power low cost LDO (low-dropout voltage regulator) for UHF RFID tag chip is presented. In order to reduce the cost, a low temperature coefficient voltage reference with only 15 K $\Omega$  resistor is proposed, this voltage reference is based on sub-threshold operation and the power consumption is minimized. A pole-zero tracking compensation circuit is used, this scheme generates an internal zero which tracks the pole produced by the load current. The design is based on UMC 0.18  $\mu$ m 2P5M EEPROM process, and the active area is only 0.0146 mm<sup>2</sup>. The LDO has a maximum load capacity of 5 mA while outputs a 1.1 V stable voltage. The measured undershoot and overshoot are 55 mV and 60 mV respectively. With the ultra-low power voltage reference circuit, the total quiescent current is only 370 nA under a 1.2 V power supply. The proposed regulator has been used in UHF RFID tag chips successfully.

**Keywords:** ultra-low power, low cost, UHF RFID, LDO

**Classification:** Integrated circuits

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## 1 Introduction

In recent years, the demand for low-cost and low-power passive UHF RFID tags is significantly increasing, mainly due to its high data rates, small antenna sizes and low costs [1, 2]. Since passive UHF RFID tags are powered up by the electromagnetic field, one of the major challenges of RFID circuits design is the ultra-low power LDO, for the limited received power, the LDO should function properly even under low supply voltage. Most of preexisting regulators focus on transient response, power supply rejection and frequency compensation schemes [3, 4, 5, 6], they consumes dozens of microamperes current, even up to several hundreds of microamperes, these methods are not suitable for passive RFID tag. Few voltage regulators have been proposed to meet the low-power and low-cost requirements, a LDO with fast transient response is proposed with only 0.0133 mm<sup>2</sup> die area [6], but actually it needs a large load capacitor whose capacitance ranges from 470 pF to 10 nF. A voltage reference with ultra-low quiescent current is proposed [7], but it is not favorable to use this bandgap voltage reference in passive RFID tag design because of the very large resistor, up to mega Ohm.

In this paper, a low-power low-cost regulator is proposed to meet the strict requirements of passive UHF RFID tag chip. In order to reduce the cost, a low temperature coefficient voltage reference with only 15 k $\Omega$  resistor is proposed, this voltage reference is based on sub-threshold operation and the power consumption is minimized. By using this regulator, the die area and the power consumption can be both minimized. Therefore, the maximum distance between the tag and the reader can be increased.

## 2 Architecture and circuit design

The structure of proposed LDO is shown in Fig. 1. It consists of a start-up circuit, a current reference, a reference voltage generator, error amplifier (EA), compensation network and feedback network.

The start-up circuit, consisting of MP1, MP2 and C1, is adopted to get rid of the degenerate point. The current reference circuit is made up of transistors MN1, MN2, MP3, MP4, MN4, resistor R1. Except for the NMOS resistor MN4, all the MOSFETs are operated in the subthreshold region, transistor MN4 operates in deep

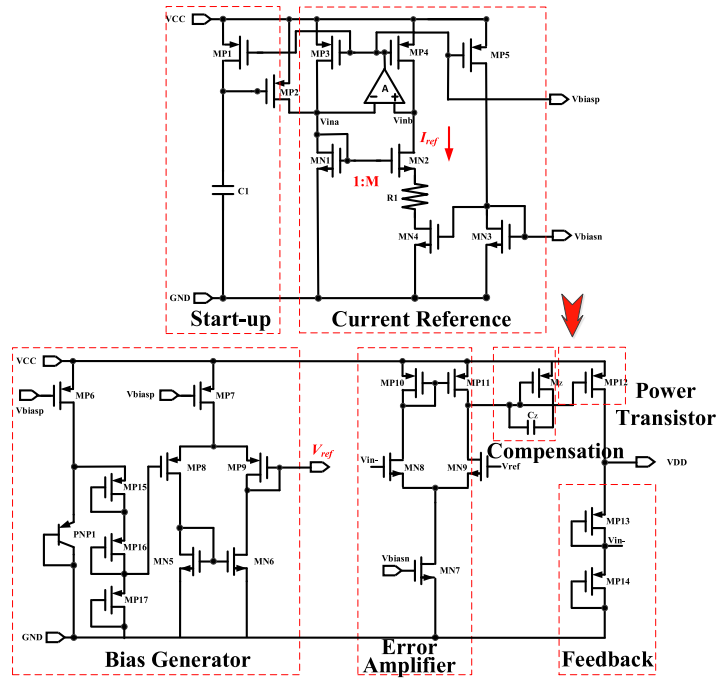


Fig. 1. Structure of the proposed LDO

triode region functioning as a controlled linear resistor to replace the resistors used in the conventional circuits. To save power and simplify the design of the regulator, a single stage differential amplifier is adopted to keep  $V_{ina}$  and  $V_{inb}$  the same. The subthreshold current can be expressed as Eq. (1)–(2).

$$I = I_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (1)$$

$$I_0 = (W/L)\mu C_{OX} V_T^2 (\eta - 1) \quad (2)$$

Where  $I_0$  is the pre-exponential factor,  $\mu$  is the carrier mobility,  $C_{OX}$  is the gate-oxide capacitance,  $V_T$  is the thermal voltage,  $\eta$  is the slope factor in weak inversion. As transistors MN1 and MN2 operate in the subthreshold region, leading to the voltage across R1 and linear resistor MN4 is proportional to the absolute temperature (PTAT).

$$\Delta V_{GS} = V_{GS1} - V_{GS2} = \eta V_T \ln M \quad (3)$$

Where  $M$  is the size ratio of MN2 to MN1. In the circuit, current  $I_{ref}$  is determined by R1 and MOS resistor MN4, so the drain current of MN1 is forced to Eq. (4).

$$I_{ref} = \frac{\eta V_T \ln M}{R_1 + \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_4 (V_{GS4} - V_{THN})}} \quad (4)$$

Resistor  $R_1$  has a positive temperature coefficient (TC), the electron mobility  $\mu_n$  has negative TC and  $V_T$  has a positive TC. Hence, if choose the right size of MN4, the resistor R1, and the size ratio  $M$ , the TC of the  $I_{ref}$  can be equal to zero at a selected temperature because the differential of denominator cancels that of numerator. Reference current flows through bipolar transistor PNP1 which gen-

erates a negative TC voltage  $V_{BE}$ .  $V_{BE}$  is divided by MP15~MP17. For another pair MN8-MN9 operates in the subthreshold region, reference voltage  $V_{ref}$  is equal to Eq. (5).

$$V_{ref} = \frac{1}{3} V_{BE} + (V_{GS9} - V_{GS8}) = \frac{1}{3} V_{BE} + \eta V_T \ln(K_6 K_8 / K_5 K_9) \quad (5)$$

Here  $K_i$  is the aspect ratio of the transistor  $M_i$ . The temperature dependence of the reference voltage can be obtained by differentiating the above with respect to temperature and the result is given by Eq. (6). Note that,  $V_T$  has a positive TC, while  $V_{BE}$  has a negative one, by setting proper aspect ratios, they can cancel each other, and the zero temperature coefficient (ZTC) reference voltage can be achieved.

$$\frac{\partial V_{ref}}{\partial T} = \frac{1}{3} \frac{\partial V_{BE}}{\partial T} + \eta \frac{\partial V_T}{\partial T} \ln(K_6 K_8 / K_5 K_9) \quad (6)$$

In order to achieve low-power and small chip area at the same time, the proposed circuit uses diode-connected PMOS transistors as the feedback network. Comparing with resistive feedback network, this solution decreases the die area effectively. Furthermore, the substrate of PMOS is connected to the source without worrying about body-effect issue, which makes PMOS transistors of feedback network to have accurate potential division and the same level of performance. As LDOs have high output impedance, this impedance, along with the load capacitance, creates a low frequency pole and decreases the overall phase margin. In order to improve the stability of the system, compensation network is needed. The transistor  $M_Z$  acts as a voltage-controlled resistor  $R_Z$ . This transistor operates in deep triode region because there is no current flow to ground and is controlled by the gate of power transistor MP12, the effective resistance of  $M_Z$  can be expressed as

$$R_Z = \frac{1}{\mu_P C_{ox} \left( \frac{W}{L} \right)_{M_Z} (|V_{GS,M_Z}| - |V_{THP}|)} = \frac{1}{\mu_P C_{ox} \left( \frac{W}{L} \right)_{M_Z} (|V_{GS,MP12}| - |V_{THP}|)} \quad (7)$$

While adding the compensation network, the AC gain of EA is given by Eq. (8).

$$\begin{aligned} A(s) &= \frac{g_{MN8}}{\frac{1}{R_{OA}} + s \times C_{MP12} + \frac{s \times C_Z}{1 + s \times C_Z \times R_Z}} \\ &= A \times \frac{1 + s C_Z R_Z}{1 + s C_Z R_Z + s C_{MP12} R_{OA} + s C_Z R_{OA} + s^2 C_Z C_{MP12} R_Z R_{OA}} \end{aligned} \quad (8)$$

It is obvious that compensation network generates an adjusted zero which is on the left half-plane. The output pole  $P_{OUT}$  ( $1/C_L R_L$ ) is cancelled by the tracking zero  $Z_{OA}$ . The zero is controlled by the gate voltage of the power device and varies with the load current. The LDO then becomes an adjustable single-pole system and the dominant pole is generate at the output of EA in Fig. 1.

### 3 Measurement results

The chip altogether with AFE is fabricated in UMC 0.18  $\mu$ m 2P5M EEPROM process and encapsulated in a quad-flat no-lead (QFN) package, the chip die photo

is shown in Fig. 2 and the active area of LDO is only  $0.0146 \text{ mm}^2$ . A  $440 \text{ pF}$  on-chip MOS capacitor follows the regulator to improve transient performance. For the load regulation measurement consideration, a test circuit is used in Fig. 3 to emulate the current load. The current load is set by  $V_{\text{SOURCE}}/R_{\text{SET}}$ , here a *Rohde & Schwarz SMBV 100 V* Signal Generator is used to generate the needed voltage ramp, a TI OPA 354 with  $100 \text{ MHz}$  GBW is used to ensure fast transition. The measured load regulation is shown in Fig. 4. A  $5 \text{ V}$  square wave is injected into OPA and a  $5 \text{ mA}$  current flows to ground through a  $1 \text{ K}\Omega$  resistor. When the load current switches between  $0 \mu\text{A}$  and  $5 \text{ mA}$  with a rising and falling time of  $10 \text{ ns}$ , the overshoot and undershoot are  $60 \text{ mV}$  and  $55 \text{ mV}$  respectively. This transient response and the maximum  $5 \text{ mA}$  load current mean that this regulator can be extended to some SoC applications.

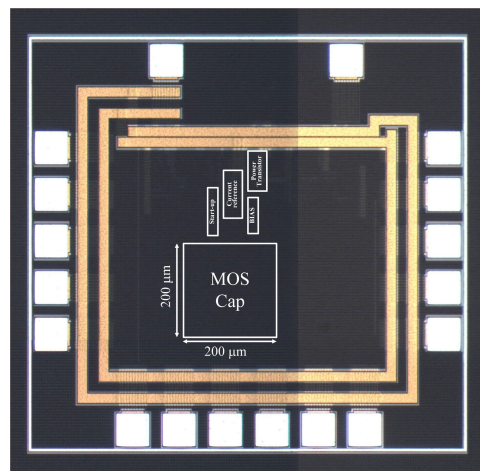


Fig. 2. Chip die photo

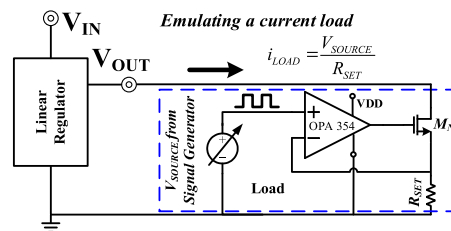


Fig. 3. Load regulation measurement setup

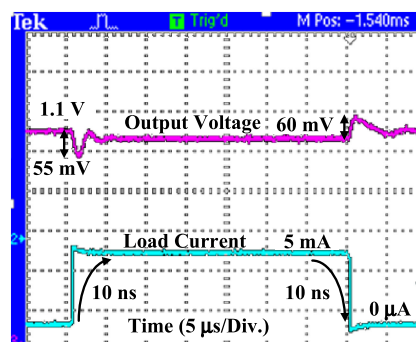
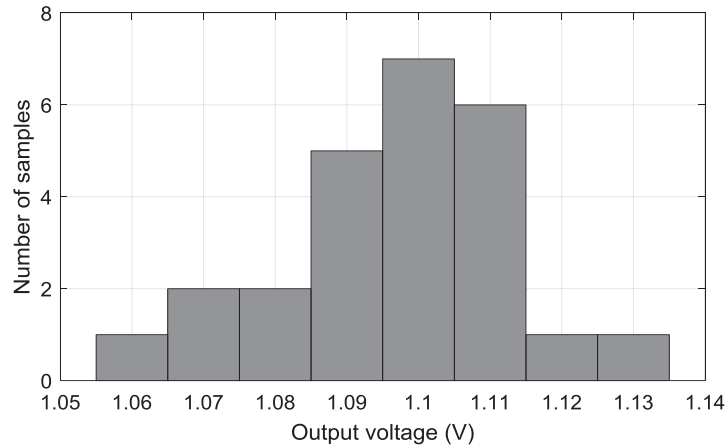


Fig. 4. Measured load regulation of proposed LDO

The 25 samples from the same wafer have been tested and the results are shown in the histogram of Fig. 5. Experimental results show a standard deviation of the regulator output voltage of 4.5%, which is close to the value from process corner variation.



**Fig. 5.** Histogram of VDD for 25 measured samples

Table I compares the proposed LDO with state-of-the-art LDOs. Compared to previous ultra-fast transient response designs [4, 6, 8], this regulator achieves a medium settling time ( $<5\ \mu\text{s}$ ). Furthermore, an ultra-low 370 nA current dissipation is achieved with the sub-threshold bias, while other regulators dissipates at least  $16\ \mu\text{A}$ . No large resistors are used and the active area is only  $0.0146\ \text{mm}^2$  which means less implementation cost. Measurement results also show that the dropout voltage is only 100 mV, leading to a high power efficiency.

**Table I.** Performance comparison with other papers

Reference	3	4	5	6	8	9	10	This Work
Year	2015	2014	2012	2014	2012	2014	2016	2016
Tech. ( $\mu\text{m}$ )	0.065	0.18	0.13	0.065	0.18	0.13	0.18	0.18
$I_{\text{out-max}}$ (mA)	10	50	50	50	5	5	10	5
$I_Q$ ( $\mu\text{A}$ )	50	80	37	15.9~487	120	99	265	0.37
Settling Time ( $\mu\text{s}$ )	$<0.1$	$<6$	0.4	0.4	4.8	1	0.3	$<5$
Load Reg. (mV/mA)	1.1	0.14	N/A	0.18	0.122	10	4	12
$V_{\text{in}}/V_{\text{out}}$ (V/V)	1.2/1	1.8/1.6	1.2/1	0.75/0.55	1.6/1.2	1.2/1	1.8/1.2	1.2/1.1
Active area ( $\text{mm}^2$ )	0.023	0.14	0.018	0.0133	0.16	0.00245	0.079	0.0146

#### 4 Conclusions

An ultra-low power low cost LDO for UHF RFID tag chip is presented. A low temperature coefficient voltage reference with only 15 K $\Omega$  resistor is proposed, this voltage reference is based on sub-threshold operation and the power consumption is minimized. A pole-zero tracking compensation circuit is used and the dominant pole of the regulation loop is set at the output of EA without using an expensive off-chip capacitor. The experiment results demonstrate that the proposed circuits achieve good performance with considerable reduction of die area and power consumption, leading to compact and long-range passive UHF RFID tag. Moreover, this LDO is promising for Body Sensor Network integration because of its low power and fast transient dynamics.