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Design of low-power, fast-transient-response, capacitor-less low-dropout regulator for mobile applications

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Abstract: This paper presents a capacitor-less low-dropout (LDO) regulator for on-chip mobile applications. An additional push-pull current with a capacitive coupling circuit is proposed to significantly enhance the transient response of the LDO regulator. The proposed LDO regulator can deliver an output current of 100 mA with a minimum dropout voltage of 0.4 V. The circuit was modeled and implemented in a 0.35-µm CMOS process with a die area of 0.22 mm^2. The experimental results show that the LDO regulator can be recovered within 0.5 µs at a voltage spike less than 90 mV.

Keywords: capacitor-less low-dropout (LDO) regulator, transient enhancement, regulator, system-on-chip

Classification: Power devices and circuits

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1 Introduction

Recently, power-management circuits have been widely demanded for mobile systems such as cellular phones and biomedical devices where a limited power source is used. Most power-management systems consist of low-drop out (LDO) voltage regulators to supply a stable voltage to each block and isolate sub-systems [1]. Conventional LDO regulators require a large output capacitor with a range of a few microfarads. They guarantee the stability of the open-loop alternating-current (AC) response under a light load and compensate for dramatic variations in the output voltage under a transient load [2]. However, because of the large area of the output capacitor, each LDO regulator occupies a large area of the silicon wafer in a power management integrated circuit (PMIC). Thus, to reduce the cost of the integrated circuit and improve the area efficiency of systems-on-chip, LDO regulators without an output capacitor have recently been investigated in many studies [3, 4, 5].

In the capacitor-less LDO regulator topology, it is very challenging to satisfy both the loop stability and the transient-load response requirements [6, 7]. The slew rate of the error amplifier in a capacitor-less LDO regulator is primarily limited by the Miller compensation and the parasitic capacitor of the pass transistor. Ref. [8] is one of the few works related to enhancing the slew rate of capacitor-less LDO regulators. However, the method proposed therein requires an additional compensation capacitor in the gate of a power positive-channel metal-oxide semiconductor (PMOS). In this letter, an additional push-pull current with a capacitive coupling circuit (APPCC) is proposed to achieve a fast transient-load response in a capacitor-less LDO regulator without any additional capacitor installation.

2 Proposed design and circuit implementation

The transient response of LDO regulators is dominated by both the slew rate of the gate power transistor, SR_G, and the loop gain bandwidth, BW_L [9]. To achieve a high slew rate, a large current must be supplied to the gate of a PMOS. However,

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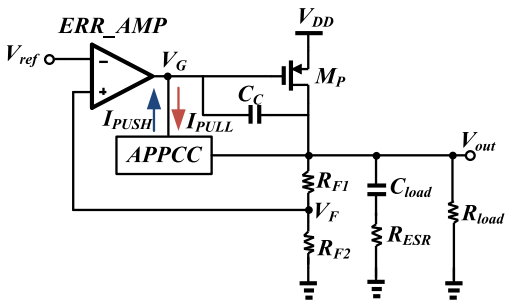

Fig. 1. Proposed capacitor-less LDO regulator.

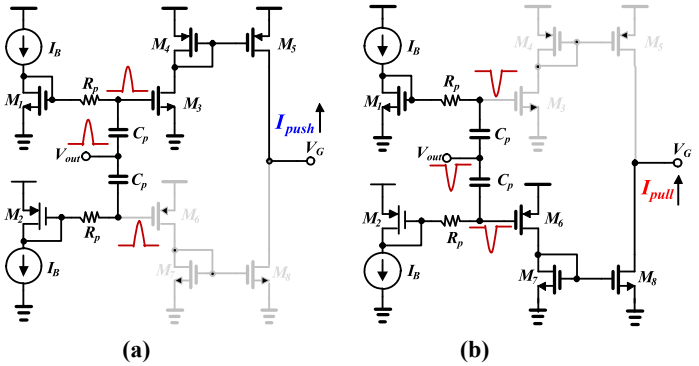

Fig. 2. Operation principle of the proposed APPCC.

this requires a large power consumption and is therefore impractical. That is, this approach is not power-efficient, as the quiescent current of the LDO, i.e., I_q, is high under all loading conditions. An alternative solution is to increase I_q only at the transient interval, as with dynamic biasing [10]. The extra current that flows to the gate of the PMOS pass element remains very low in the steady state and can improve the transient response. Fig. 1 shows a conceptual diagram of the APPCC in the proposed LDO regulator and Fig. 2 shows a detailed schematic of the operation of the APPCC. The circuit is basically formed by two capacitive coupling networks and current mirror. The main idea is to temporarily increase or decrease the bias current that flows to the gate of the power PMOS when the feedback voltage V_F changes rapidly in order to minimize the V_{out} variation in the transient response. Without the variation of the load, V_{out} remains constant, and V_{GS3} and V_{GS6} are defined for $I_{D5} = I_{D8}$, where I_{D5} and I_{D8} are the currents flowing through M_5 and M_8, respectively. However, when V_{out} varies rapidly, and V_{GS3} and V_{GS6} vary almost equally to V_{out}. This causes a push-pull current and improves the transient response.

For the circuit shown in Fig. 2(a), when the V_{out} remains constant, V_{GS3} is defined by V_{GS1}, and $I_3 = I_1$. However, when the amplitude of the V_{out} changes from low to high (ΔV) instantaneously, the rapid voltage change of V_{out} is coupled to the gate of M_3 directly because of the high-pass property of C_P. In addition, R_P is chosen to be large for better isolation between M_1 and M_3 during the changing of the pulse voltage. As a result, when C_P is chosen to be larger than $C_{GS1} + C_{GS3}$, the gate voltage of M_3 is dominated by the coupled signal from C_P at this instant, instead of the direct-current voltage provided by R_P. Thus, V_{GS3} is increased

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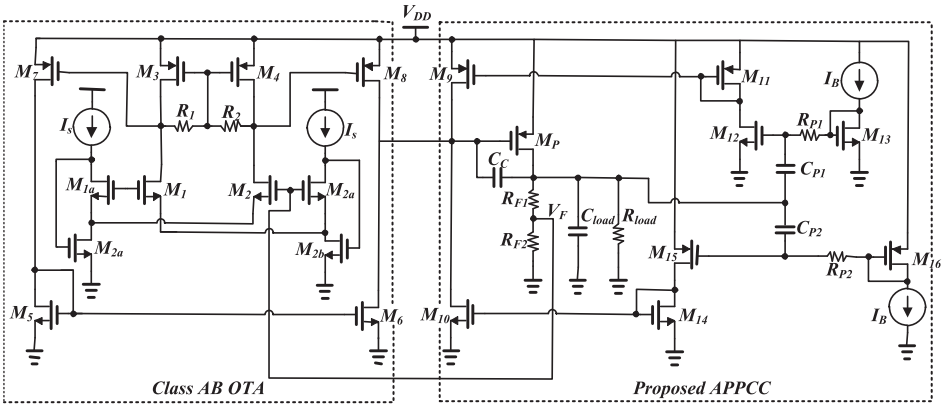


Fig. 3. Detailed schematic of the proposed capacitor-less LDO regulator.

momentarily to increase I_3. The extra current (ΔI_3) can be calculated using Eq. (1), as shown in Eq. (2).

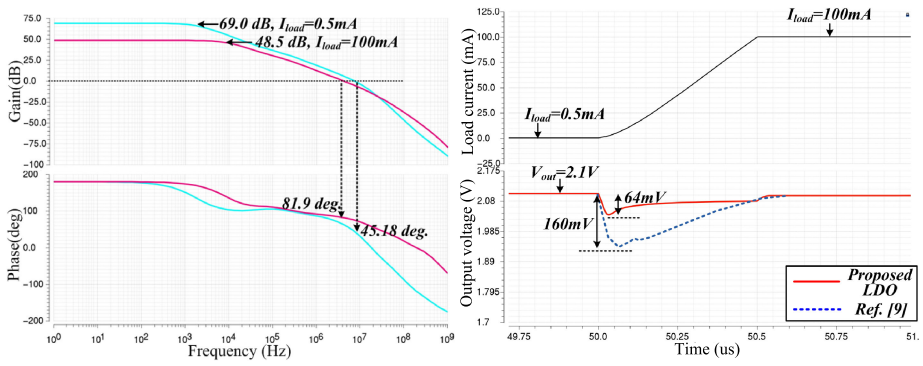
$$I_3 + \Delta I_3 = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_3 \cdot (V_{GS3} + \Delta V - V_{TH})^2. \tag{1}$$

$$\Delta I_3 \approx \mu_n C_{OX}\left(\frac{W}{L}\right)_3 \cdot \left(V_{GS3} + \frac{\Delta V}{2} - V_{TH}\right)\Delta V. \tag{2}$$

Fig. 3 shows a schematic of the entire LDO regulator, including the APPCC. For low-quiescent current consumption, the super class AB OTA was employed as an error amplifier.

3 Simulation and experimental results

Fig. 4(a) shows the Bode-plot simulation results for the proposed LDO regulator. From the simulation results, the proposed LDO regulator is stable for load current values ranging from 0.5 to 150 mA with a phase margin of more than 45°. Fig. 4(b) shows the simulated load transient response of the proposed LDO regulator. When the load current changes from 0.5 to 100 mA, the proposed technique causes a small output-voltage spike of 64 mV, compared with that of 160 mV for previously



(a) (b)

Fig. 4. Simulation results for (a) the AC open-loop analysis for heavy and light loads and (b) the transient-load response with the APPCC.

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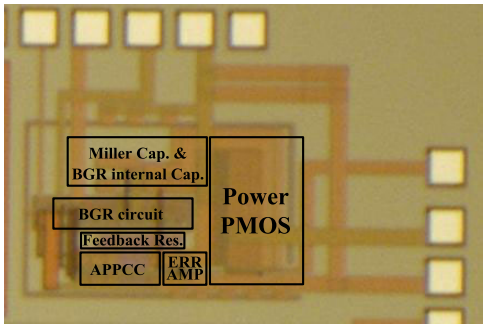
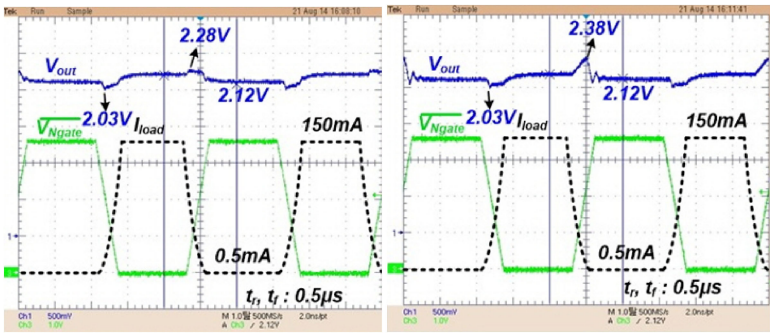


Fig. 5. IC micrographs of the proposed LDO regulator.



(a) (b)

Fig. 6. Experimental results for the transient-load response. (a) V_{DD} = 3.3 V, C_{load} = 100 pF, (b) V_{DD} = 2.5 V, C_{load} = 100 pF.

reported LDO regulator design. The circuit was implemented in 0.35-μm complementary metal-oxide semiconductor (CMOS) process. The chip micrograph is shown in Fig. 5. The measured transient-load responses without an off-chip output capacitor are shown in Fig. 6. When load changes from 0.5 to 150 mA, the measured results show that the maximum undershoot and overshoot voltages are 90 and 260 mV, respectively. The measurement results show that the proposed LDO regulator fully recovers within 0.56 μs. Table I shows a performance comparison with previously published works.

Table I. Performance summary and comparison

	This work	[6]	[7]	[9]
Tech. (um)	0.35	0.6	0.13	0.11
Type	Cap-less	Cap-less	Cap-less	Cap-less
V_{DD} (V)	2.5–3.3	1.5–4.5	0.9–1.5	1.8–3.8
I_{max} (mA)	100	100	50	200
$T_{recovery}$ (μs)	0.56	2	28	0.61
Undershoot in load tran. (mv) (sweep time)	90 (0.5 μs)	Unstable @	730 (0.2 μs)	385 (0.5 μs)
I_q (uA)	55	38	1.33	41.5
Area (mm^2)	0.22	0.31	0.03	0.21
FOM (pV·s)	23.1	-	543.7	48.7

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A figure of merit ($\Delta V_{undershoot} \cdot I_q \cdot T_{recovery}/I_{max}$) was used to compare the proposed structure with a previous design.

4 Conclusion

A LDO regulator based on a novel APPCC technique was proposed. The APPCC circuit enables the enhancement of the slew rate via the adjustment the gate current of a PMOS pass transistor. The undershoot of the output voltage in the transient-load response can be reduced to less than 90 mV. The proposed LDO regulator has good stability under the full range of a 100-mA load current. The chip was implemented using 0.35-μm CMOS technology. The simulation and experimental results demonstrate the performance of the proposed LDO. This work helps to eliminate off-chip capacitors in LDO regulators while preserving a fast transient response.

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