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A transient pulse dually filterable and online self-recoverable latch

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Abstract: This paper presents a transient Pulse Dually Filterable and online Self-Recoverable (referred to as PDFSR) latch. Based on soft error masking property of C-element and using built-in delayed paths combined with a Schmitt inverter, a single event transient (SET) pulse could be dually filtered. Meanwhile, mutually feeding back mechanism of multiple C-elements was constructed to retain data, which makes the latch self-recoverable from a single event upset (SEU). Simulation results have demonstrated the SET filtering ability and SEU resilience at the cost of only 2.0% area-power-delay-width product increase on average, compared with the similar latches.

Keywords: single event transient, single event upset, latch design

Classification: Integrated circuits

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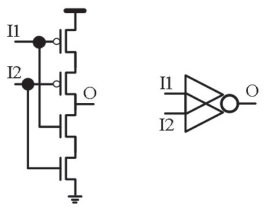
1 Introduction

Soft error is of transient error induced by transient fault in an IC and the transient fault mainly results from striking of particles especially in radiation environment. The lifetime of an IC includes three parts from tape-out to discard as useless, i.e. early lifetime, normal lifetime and aging [1]. In normal lifetime, soft error is the main factor impacting circuit reliability and in nanoscale technology the impacting factor is becoming more serious [2].

As regards soft error, researchers have paid much attention to single event transient (SET) and single event upset (SEU). Recently, many schemes about latch hardening against SET or SEU have been proposed [3, 4, 5, 6, 7, 8, 9, 10] and these schemes could be divided into three categories: 1) SEU not immune ones [3, 4], i.e. there is at least one weak node and if the node is flipped by an SEU the latch would retain invalid data; 2) SEU immune but SET not filterable ones [5, 6, 7, 8], i.e. the output would not retain invalid data no matter which node of the latch is affected by an SEU, but cannot filter an SET; 3) SEU immune and SET filterable ones [9, 10].

Among these schemes, C-element (CE) is widely used. Take a 2-input CE for an example, Fig. 1 has presented the circuit structure, symbol and truth table of it. From Fig. 1 we can see that if the inputs are identical the CE behaves as an inverter and if the inputs are different the output enters high-impedance state i.e. keeps the previous value. Hence if anyone of the inputs is affected by an SET or SEU, the output prevents the soft error propagation and retains the previous correct value, which could be defined as the soft error masking property of CE.



I1	I2	O
0	0	1
1	1	0
0	1	Z
1	0	Z

a) Circuit structure b) Symbol c) Truth table

Fig. 1. Introduction to a 2-input C-element.

Fig. 2 has presented a typical SEU-not-immune latch [4]. In latching mode of operation, if Q is affected by an SEU, the latch would retain invalid data, since Q is feeding back to nodes N1 and N2 simultaneously. Note that the structure in the dotted box is a Schmitt inverter (ST-inv), which could filter an SET and the latch is SET filterable.

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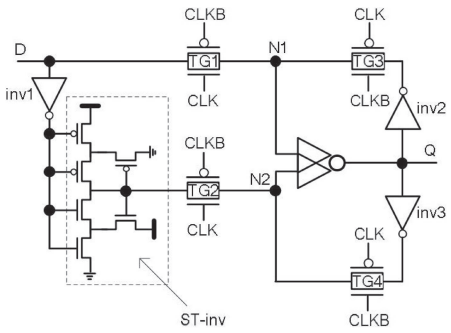

Fig. 2. A latch design in [4].

In order to achieve SEU immunity, HLR latch has been proposed by H. Nan et al. [5] The latch mainly consists of two traditional latches feeding back to a CE to robustly retain data. If anyone of the traditional latches is affected by an SEU, the CE blocks the incorrect data, but the CE would enter high-impedance state (HIS) and its output may charge or discharge to an incorrect value due to leakage current as time goes by especially when working in standby mode. Besides, the latch could not filter an SET.

In order to achieve SEU immunity and SET filtering ability simultaneously, LSEH1 and LSEH2 latches have been proposed by R. Rajaei et al. [9] Similarly, these latches employ spatial redundancy to achieve SEU immunity and at the same time employ temporal redundancy to achieve SET filtering ability. However, there is at least one node for these latches that could not self-recover from an SEU and these latches have lower SET filtering ability as well. Besides, the latch in [10] also has the same problems.

2 Proposed PDFSR latch

To achieve SEU resilience (i.e. any node is self-recoverable from an SEU) and improve SET filtering ability, we present the PDFSR latch as shown in Fig. 3, in which, D is the input, CLK and CLKB are the system clock and negative system clock, respectively, and Q is the output. Note that, TG1, TG2 and TG3 are transmission gates and cg-inv is a clock gating based inverter.

When CLK = 1, the latch works in the transparent mode of operation. TG1 and TG2 are turned ON and TG3 and cg-inv are turned OFF. N3 is driven by N1 and N2 through CE1, N3b is driven by N3 through ST-inv, N4 is driven by N2 and N3b through CE2 and Q is driven by N3 and N4 through CE3, thus D propagates to Q successfully. As we can see, the output of CE1 is feeding back to one of the inputs of CE3 and CE2 simultaneously. Meanwhile, the output of CE2 is feeding back to one of the inputs of CE3. Obviously, the inputs of CE2 and CE3 have delay difference d_1 and d_2, respectively, and

$$d_i = \tau_i + \tau_{\text{st-inv}}, \quad i = 1, 2. \tag{1}$$

In Eq. (1), τ_i is transmission delay of CE1 (when $i = 1$) and CE2 (when $i = 2$) from their inputs to output on average and $\tau_{\text{st-inv}}$ is transmission delay of ST-inv from its input to output on average.

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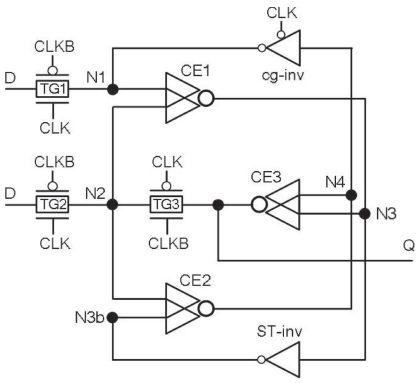
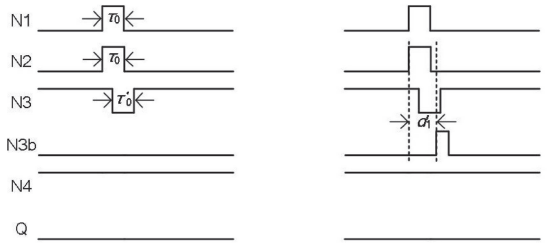


Fig. 3. Proposed PDFSR latch.



a) Fully filtered τ'_0 by ST-inv; b) Partly filtered τ'_0 by ST-inv

Fig. 4. Filtering cases for a positive SET.

Assumed a positive SET pulse with width τ_0 propagates to N1 and N2 through TG1 and TG2, the pulse would be reversed through CE1 to N3 (noted as τ'_0) and there are two cases for discussion.

1) If τ'_0 is fully filtered by ST-inv, N3b would equal to correct D signal. According to the soft error masking property of CE, the SET τ_0 propagating from N2 to the input of CE2 would be masked and N4 would equal to the reverse of D signal. Similarly, the SET τ'_0 propagating from N3 to the input of CE3 would be masked. This case has been presented in Fig. 4-a).

2) If τ'_0 is partly filtered by ST-inv, we can detect an SET on N3b with width less than τ'_0. If $\tau_0 \leq d_1$, according to the soft error masking property of CE, the SETs propagating from N2 and N3b to the inputs of CE2 would be masked. Similarly, the SET propagating from N3 to the input of CE3 would be masked. This case has been presented in Fig. 4-b). Note that, if the width of an SET is very larger especially when $\tau_0 > d_1$, the SET could not be effectively masked. On the other hand, as regards filtering cases for a negative SET, we could draw a similar conclusion.

As discussed above, we can see ST-inv is supporting first-level SET filtering and used to delay the pulse on N3b, while CE2 is used for actual first-level SET filtering and CE3 is used for actual second-level SET filtering. Hence, the proposed latch could dually filter an SET to improve SET filtering ability.

When CLK = 0, the latch works in the latching mode of operation. TG1 and TG2 are turned OFF and TG3 and cg-inv are turned ON, hence robust feedback loops are constructed to retain data using triple mutually feeding back CEs. The feeding back rule of the CEs is that the output of the first CE is feeding back to one

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of the inputs of the second CE and also feeding back to one of the inputs of the third CE. In latching mode, ST-inv and cg-inv are mainly used to ensure correct feeding back logics and note that N2 = Q.

In latching mode, there are five nodes may sensitive to an SEU, i.e. N1, N2(Q), N3, N3b, N4, in which, N1 and N3b are the output of two kinds of inverters and they are defined as first-kind nodes, but other nodes are the output of CEs and they are defined as second-kind nodes.

When a first-kind node is affected by an SEU, since the input of the according inverter is not affected, the first-kind node could on-line self-recover through the inverter. When a second-kind node is affected by an SEU, it means the output of a CE is affected. According to the feeding back rule of the CEs, this case also means both an input of the other two CEs are affected. According to soft error masking property of CE, the so called the other two CEs would temporally enters HIS and the outputs of them would keep correct data. According to the feeding back rule of the CEs, these correct outputs are feeding back to the inputs of the CE whose output has been affected, thus the CE could on-line self-recover from its correct inputs. In sum, the latch is on-line self-recoverable from an SEU.

3 Simulation and comparison

The SET filtering ability and on-line self-recoverability verifications of the PDFSR latch were performed utilizing HSPICE simulation. The simulation conditions are listed below. 1) 32 nm technology, PTM model [11]; 2) 0.9 V supply voltage and room temperature; 3) 0.5 GHz working clock frequency; 4) Double exponential current source model for SET and SEU injections [6, 7, 8].

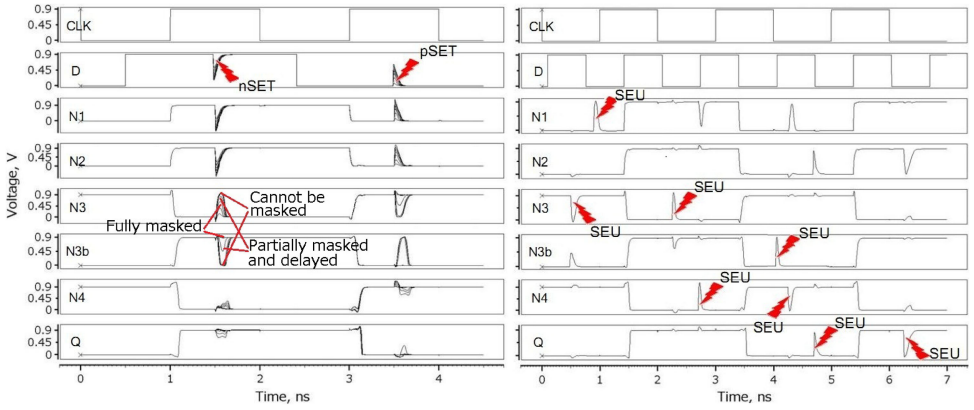

Fig. 5. Simulation results of SET and SEU tolerance.

Fig. 5 presents the simulation results of SET and SEU tolerance. As we can see, the SET with a certain width could be effectively filtered, resulting in nearly no impact on Q no matter for a negative SET (nSET) or a positive SET (pSET). As regards SEU tolerance, we can see any node could self-recover from an SEU. Since N2 = Q in latching mode, the SEU injection on N2 is omitted. In sum, the latch is SET filterable and SEU resilience.

In order to quantitatively analyze overheads of the PDFSR latch and make comparison with the alternative latches mentioned in the first section, we have

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performed the simulations for these latches using the same simulation conditions as well. Table I has presented the comparison results among the latches. In Table I, the fifth to the last column data are silicon area, the average of dynamic plus static power dissipation, D to Q transmission delay, the maximum width of filterable SET, SET filtering ability (SFA) and the comprehensive area-power-delay-width product (APDWP), respectively.

Table I. Comparison results among alternative latches.

Latch	SET Filterable	SEU Immune	SEU Resilient	Area (USTs)	Power (μw)	Delay (ps)	Max. width (ps)	SFA (%)	APDWP
Design in [4]	YES	NO	NO	98.9	1.64	90.8	72.7	80.1	202.58
HLR in [5]	NO	YES	NO	81.5	0.77	1.6	-	-	-
LSEH1 in [9]	YES	YES	NO	100.4	1.81	98.2	74.2	75.6	240.50
LSEH2 in [9]	YES	YES	NO	97.2	2.13	91.5	64.5	70.5	293.70
Design in [10]	YES	YES	NO	149.1	2.39	101.3	80.7	79.7	447.31
Proposed	**YES**	**YES**	**YES**	138.2	1.87	99.6	82.4	82.7	312.38

Similarly, the silicon area was also measured in equivalent unit size transistors (USTs) required in each latch as in [8], the SFA was calculated by dividing the maximum width of filterable SET by D to Q transmission delay and the APDWP metric was calculated by multiplying area, power, and delay and dividing by the maximum width of filterable SET. Obviously, among the same type latches (e.g. SEU immune ones), a smaller APDWP is better.

From Table I we can see that only our latch has four YES. As regards SFA, our latch is the maximum and best due to the SET dully filtering property. As regards area, power and delay overheads, our latch is a litter larger than those for LSEH1 and LSEH2 and smaller than those for design in [10] but these latches are not SEU resilient at all. As regards APDWP, our latch saves 30.2% compared with design in [10] and increases only 2.0% on average compared with the latches which are both SET filterable and SEU immune.

4 Conclusion

This paper presents an SET dually filterable and SEU online self-recoverable latch. Simulation results have demonstrated the superiority of SET filtering ability and SEU on-line self-recoverability with lower overheads on average.

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