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A spread-spectrum clock generator with direct VCO modulation in open-loop

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Abstract: A new topology is proposed to achieve a spread-spectrum clock generator. It employs a new modulation filter, consisting of two capacitors and a resistor. The modulated triangular waveform is formed at the center of the control voltage coming from the segregated PLL. A definite advantage is that the spreading behavior does not affect the bandwidth of the PLL. Moreover, the modulation filter consumes smaller chip area because a larger resistor can be utilized for the required bandwidth.

Keywords: spread spectrum, VCO modulation, clock generator

Classification: Integrated circuits

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1 Introduction

Conventionally, Δ-Σ fractional-*N* PLL is used to spread the spectrum of the clock by changing the fractional divider ratio [1, 2, 3]. This method can effectively reduce the EMI level, however, the design is relatively complex. The design in [4, 5] is based on the regular integer-*N* PLL and it adds the triangular-wave into the low pass filter for the direct modulation of VCO in PLL. It has advantages of the simple circuit structure and the absence of sigma-delta modulator noise. However, the loop bandwidth of a PLL has to be much less than the modulation frequency to allow the frequency variation of the VCO. In general, the required loop bandwidth is about one tenth of the modulation frequency which is typically around 30 to 50 kHz, thereby the loop bandwidth is around 3 to 5 kHz, leading to a huge capacitor of several tens of nano-Farads in the loop filter.

Based on the previous works [4, 5, 7], a new structure is proposed so as to reduce the chip area constraint for accommodating the required capacitances.

2 Description of system architecture

'Hershey-Kiss' [6] profile shows a good EMI performance but its nonlinear equations make it more expensive due to a larger area and power consumption. The linear triangular profile can be an alternative [4, 5]. A conventional SSCG (spread-spectrum clock generator) is shown in Fig. 1(a) [5] where the linear triangular profile is realized by using direct VCO modulation. Since the modulation filter consisting of C_1, R_1, and a buffer resides inside the loop, the triangular modulation signal is integrated into the main loop filter. While the modulation path from CP_2 creates a zero for the loop stability, it affects the bandwidth of the loop filter consisting of C_2, R_2, and C_3. And hence, the loop bandwidth must be modified so that a triangular wave (V_m) is transmitted to V_b.

In order to avoid the loop bandwidth turbulence that might occur in Fig. 1(a), the proposed structure places the modulation filter of C_1, C_2, and R_1 outside the PLL loop as shown in Fig. 1(b). As the triangular wave V_m is superimposed on the control voltage V_c generating V_b, the modulation can be bidirectional, both up and down from the center frequency operating at V_c. Since the output frequency f_{out} appears in the context of the open-loop consideration, it does not affect the original bandwidth of the closed-loop PLL.

Analysis of modulation: The loop bandwidth of the PLL is critical because it influences the modulation profile and the jitter performance. As one of the input signals of the phase-frequency detector (PFD) contains the modulation component, the bandwidth of the PLL in the nonspread-spectrum mode must be small enough to filter out this feedback component generated by the modulation signal. Therefore, the choice of the proper loop bandwidth is essential to achieve a uniform

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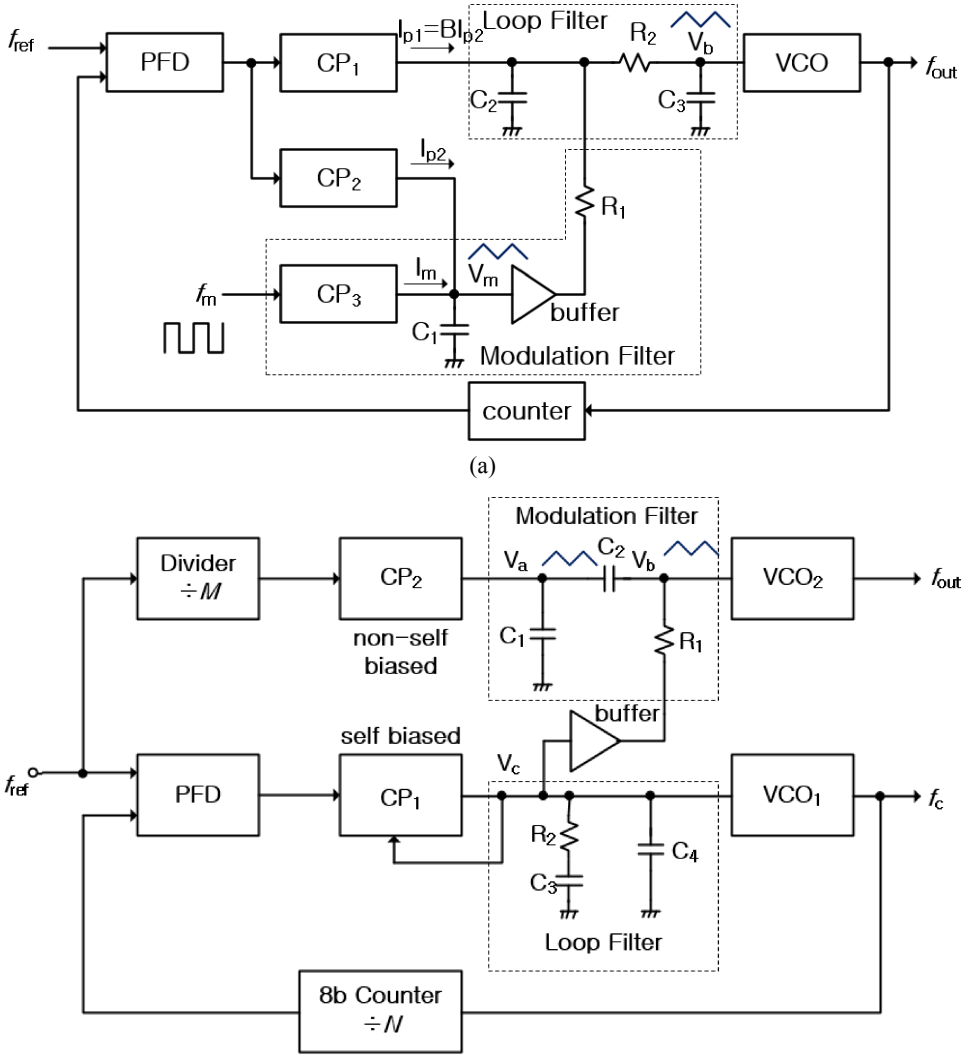

Fig. 1. Architectures of SSCG (a) conventional direct VCO modulation in closed loop (b) proposed direct VCO modulation in open loop

spread. The linear model shown in Fig. 2(a) can be used to analyze the modulated behaviors in the closed loop of Fig. 1(a). The modulated voltage denoted by $V_m(s)$ is applied to the input of the VCO generating the frequency deviation $\Delta\omega$. The relationship between the pumping current I_{p1} and the controlling voltage V_C can be easily obtained via the loop filter redrawn in Fig. 2(b). To simplify the analysis, the higher order effect of R_2 and C_3 in Fig. 1(a) is ignored, then, the transfer function is given as

$$F(s) = \frac{R_1\left(s + \dfrac{1}{R_1BC_1}\right)}{s(1 + sR_1C_2)} \approx \frac{R_1\left(s + \dfrac{1}{R_1BC_1}\right)}{s} \quad \text{when } f_m \ll 1/(2\pi R_1C_2) \qquad (1)$$

where B denotes the capacitance multiplication factor. Then, the transfer function from $V_m(s)$ to $\Delta\omega(s)$ is obtained as

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$$\frac{\Delta\omega(s)}{V_m(s)} = \frac{2\pi K_v s^2}{s^2 + \frac{2\pi K_d K_v R_1}{N}s + \frac{2\pi K_d K_v}{NBC_1}} \tag{2}$$

which can be further simplified to $2\pi K_v$ at high frequencies. In practice, its behavior is a high-pass characteristic whose loop bandwidth is roughly equal to $K \approx 1/(R_1 B C_1)$ as illustrated in Fig. 2(d). It readily demonstrates that the required capacitance is huge: (1) the modulation frequency should be much larger than the loop bandwidth, e.g. $\omega_m \approx 10 \cdot K$; (2) R_1 cannot be large in fear of adding ripple noise to V_c, e.g., $\omega_m = 2\pi \cdot 50$ [krad/sec] and $R_1 \approx 100\,\Omega$, C_1 reaches 0.32 µF (in case $B = 1$) which definitely leads to the off-chip solution.

Fig. 2(c) shows the linear model of the proposed modulation filter. As it resides out of the main loop, the relationship between $V_m(s)$ and $\Delta\omega(s)$ is proportional and straightforward, yielding

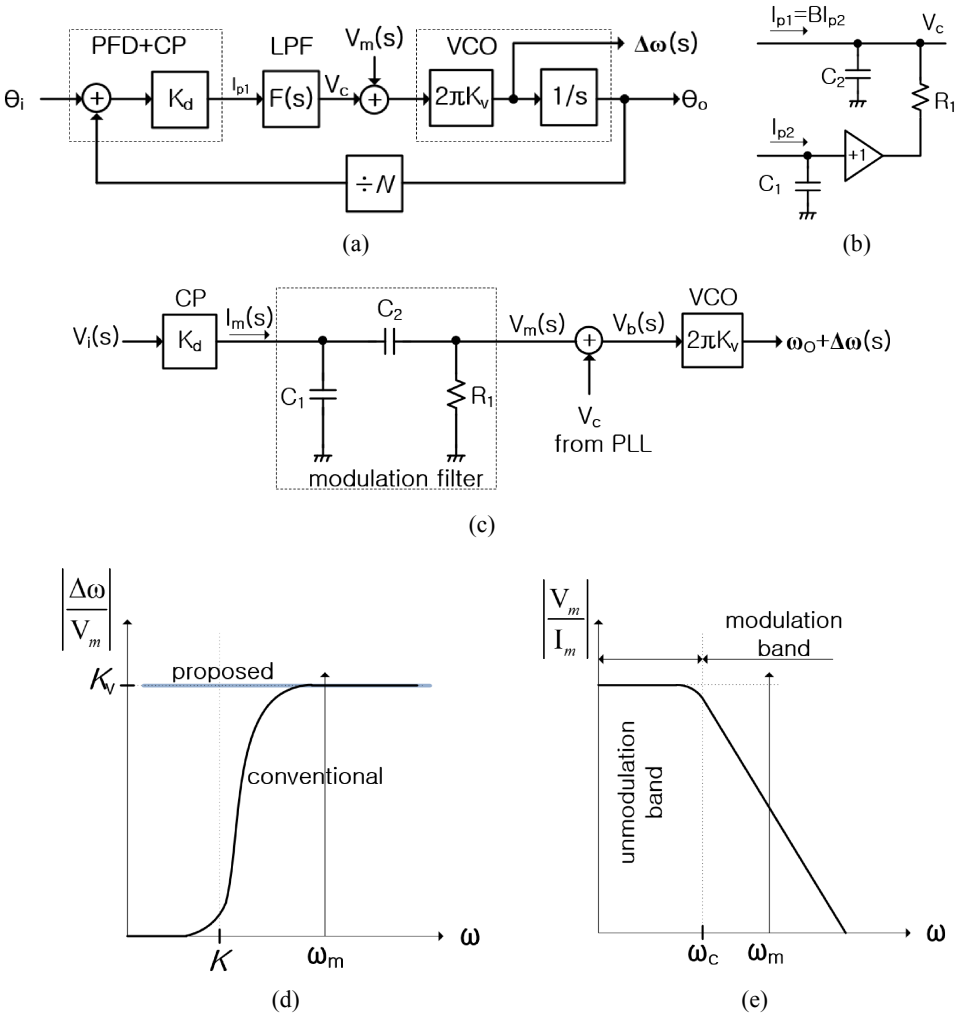

Fig. 2. (a) Linear model of conventional SSCG (b) simplified model of loop filter in Fig. 1(a) (c) linear model of proposed direct VCO modulation in Fig. 1(b) (d) frequency response from V_m to $\Delta\omega$ (e) frequency response of (c) from I_m to V_m

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$$\frac{\Delta\omega(s)}{V_m(s)} = 2\pi K_v, \tag{3}$$

which is the all-pass characteristic as is also depicted in Fig. 2(d).

By the way, the transfer function from the modulation current $I_m(s)$ to the modulation voltage $V_m(s)$ with the circuit of Fig. 2(c) can be obtained as

$$\frac{V_m(s)}{I_m(s)} = \frac{\dfrac{1}{C_1}}{s + \dfrac{1}{R_1}\left(\dfrac{1}{C_1} + \dfrac{1}{C_2}\right)} \text{ with } \omega_c = \frac{1}{R_1}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \tag{4}$$

which shows a low-pass characteristic. The behavior of integration occurs in the modulation band, e.g., $\omega_m \approx 10\omega_c$, therefore, the cutoff frequency of the modulation filter ω_c should be much less than the modulation frequency ω_m. By selecting $f_c \approx 3.2$ kHz with $R_1 \approx 1$ MΩ so that $f_m = 50$ kHz is to be in the modulation band, C_1 and C_2 might be 100 pF, respectively, which are definitely acceptable. The fact is that a large R_1 can be adopted without fear of the ripple noise in PLL because it is placed out of the loop filter of the PLL. It renders the accommodation of on-chip capacitances.

3 Design and implementation

The prototype of Fig. 1(b) has been manufactured in a standard 0.18-μm CMOS technology. Fig. 3(a) depicts a self-biased charge pump (CP_1) along with a VCO delay cell (VCO_1) used in the closed-loop of Fig. 1(b) [8]. The gate voltage, V_{BN}, for the charge pump and VCO cells is self-generated in the bias stage without additional reference circuits, and is adjusted so that all the diode-connected nodes, e.g., ⓐ, ⓑ, and V_{BP} are all equal to V_c. Therefore, the pull-down and the pull-up current, I_1 and I_2, are driven to be equal. It can also be noted that this topology allows the tracking between the differential delay cells in VCO and the charge pump. The linear VCO, which consists of four stages of differential delay cells (VCO cells), is shown in Fig. 3(b).

Fig. 3(c) shows the analog buffer with the unity gain to be used in Fig. 1(b). It renders a large swing of input and output signals with a low output impedance. On the contrary to CP_1, the charge pump (CP_2) used in the open-loop in Fig. 1(b) cannot accommodate the self-bias concept because the output voltage, V_a, fluctuates with a triangular waveform. A non-self-biased charge pump is selected [9, 10], minimizing the mismatch between the pull-up and down currents.

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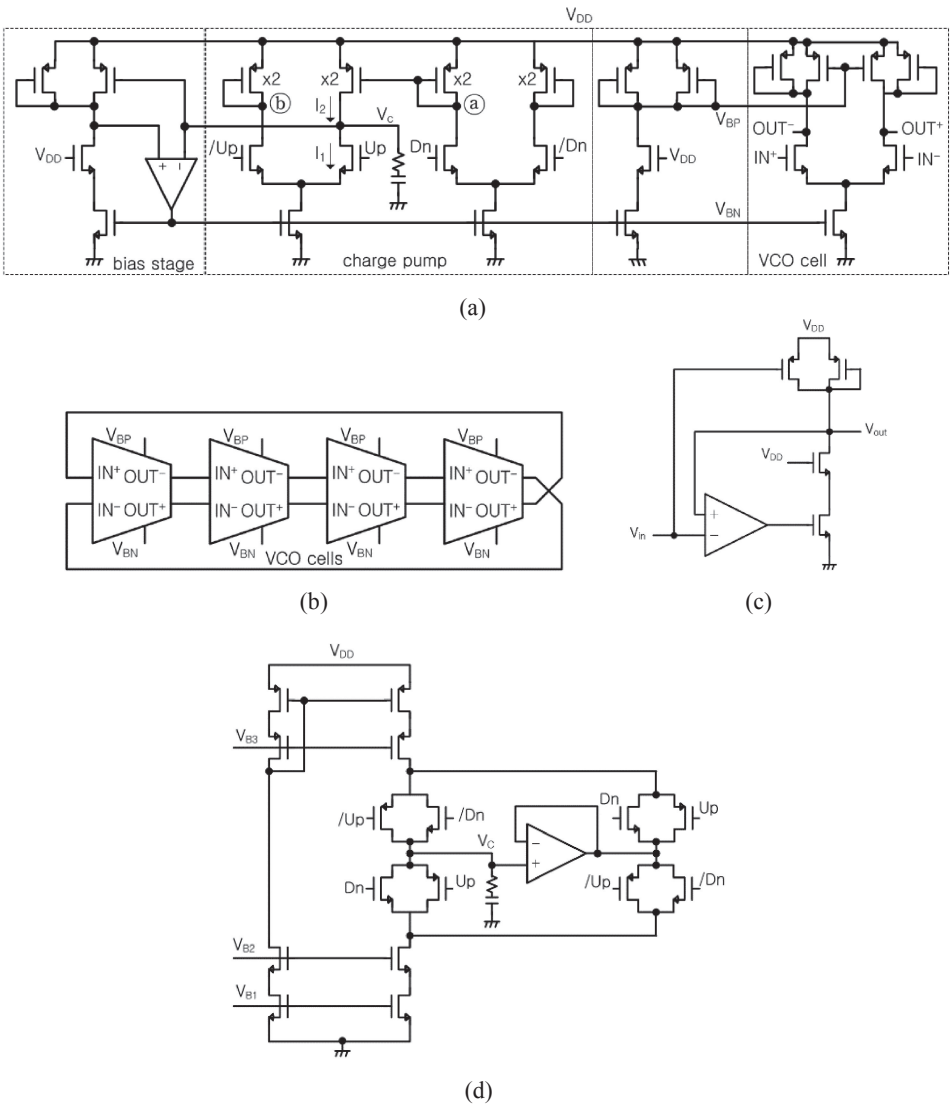

Fig. 3. (a) Self-biased charge pump and delay cell (b) differential VCO circuit (c) analog buffer with low output impedance (d) non-self-biased charge pump.

Matlab simulations were performed with Fig. 1(b) by varying $C_2 = 10\,\text{pF}$, and 100 pF with $f_m = 50\,\text{kHz}$, $C_1 = 100\,\text{pF}$, $R_1 = 1\,\text{M}\Omega$, $I_m = 2\,\mu\text{A}$, and $K_v = 10\,\text{MHz/V}$. The results are shown in Fig. 4(a) and (b), respectively, at the center frequency of 500 MHz. Fig. 4(a) illustrates the output spectra and the profile of V_m when f_m resides out of the modulation band, i.e., with $f_m = 50\,\text{kHz}$ and $f_c = 32\,\text{kHz}$. The modulation waveform looks distorted, and the EMI attenuation is 11.6 dB. In Fig. 4(b), when f_m resides in the modulation band, i.e., with $f_m = 50\,\text{kHz}$ and $f_c = 3.2\,\text{kHz}$, the modulation waveform appears as a clean triangular, and hence, the EMI attenuation is improved to be 25.4 dB.

Fig. 4(c) shows the layout plot of the test vehicle with an active area of $4\,\text{mm}^2$ with $C_1 = 100\,\text{pF}$, $C_2 = 20\,\text{pF}$, and $R_1 = 5\,\text{M}\Omega$. The measured waveforms of V_b and the output clock in the open-loop are shown in Fig. 4(d), with $f_m = 50\,\text{kHz}$ and $f_{out} = 1\,\text{MHz}$. It can be seen that the control voltage $V_c \approx 0.8\,\text{V}$ from the PLL is transmitted to V_b, and the triangular profile formed at the center value of 0.8 V

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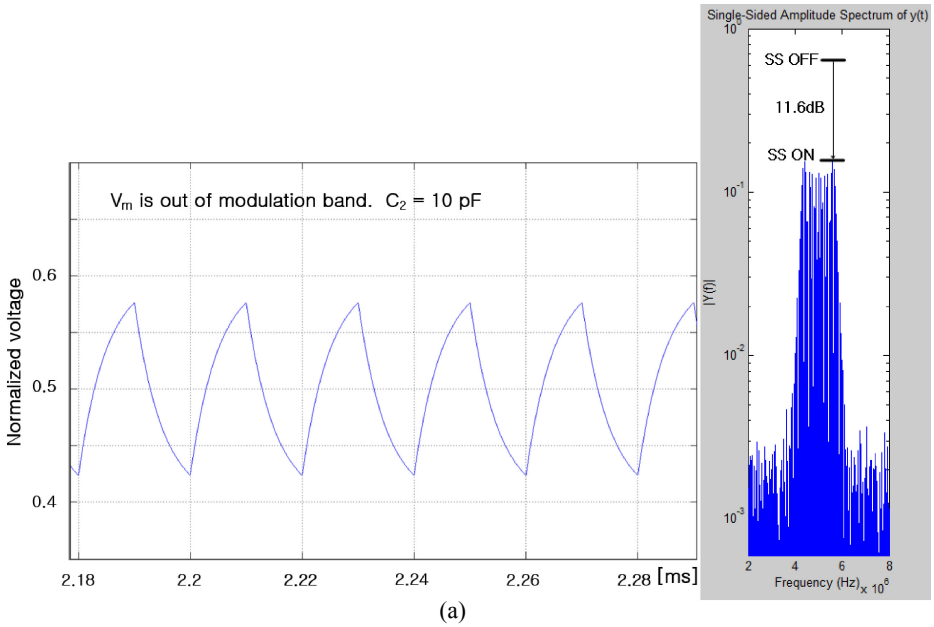
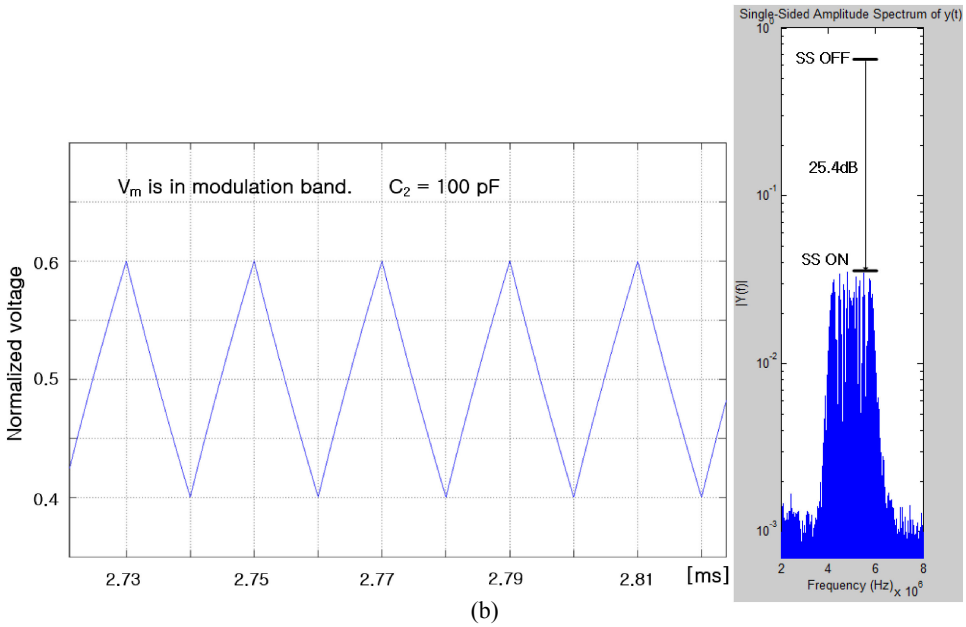
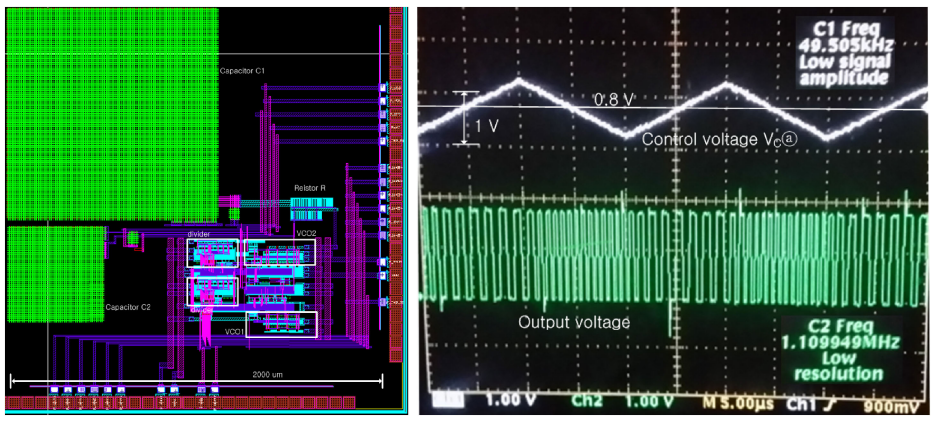


(a)



(b)



(c) (d)

Fig. 4. Simulated and measured results of Fig. 1(b) (a) output spectra and modulation voltage with $C_2 = 10\,\text{pF}$ (f_m is out of modulation band), and (b) with $C_2 = 100\,\text{pF}$ (f_m is in modulation band) (c) layout plot of Fig. 1(b) (d) measured waveforms of V_b and f_{out} (modulated output clock)

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ensures a center spreading. Table I summarizes the characteristics of the proposed SSCG.

Table I. Performance summary

Process	CMOS 0.18-μm
Supply voltage: V_{DD}	1.8 V
Modulation frequency: $f_{m(min)}$	40~50 kHz
Charge pump current	1~2 μA
VCO gain K_v	100~300 MHz/V
Capacitance (C_1)	100~600 pF
EMI reduction	−16 dB
Max. center frequency: $f_{C(max)}$	400~500 MHz

4 Conclusion

In this paper, a SSCG with triangular modulation in a 0.18-μm CMOS process is presented. The modulation filter is segregated from the PLL in a mixed-loop (both closed and open-loop) architecture, revealing two major advantages: (1) spectrum modulation does not affect the parameters of the closed-loop PLL; (2) smaller on-chip capacitance can be adoptable in the modulation filter; (3) it does achieve a center-spread spectrum.

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