

High Q series negative capacitor using negative group delay circuit based on a stepped-impedance distributed amplifier

Tiedi Zhang^{1a)}, Chung-Tse Michael Wu², and Ruimin Xu¹

¹ Fundamental Science on EHF laboratory, University of Electronic Science and Technology of China (UESTC), Chengdu, P. R. China

² Department of Electrical and Computer Engineering, Wayne State University, Detroit 48202, Michigan, USA

a) teddyjohn1987@163.com

Abstract: This paper presents a novel approach to achieve a high Q series negative capacitor (NC). A stepped-impedance distributed amplifier (DA) is used to achieve the negative group delay (NGD) response. The input/output (I/O) impedance of the transistor in each stage is calculated to meet the specific voltage gain coefficient ratio. By this way, the NGD phenomenon can be observed between the input and reversed output ports of DA. A major advantage of this architecture is that the gain is configurable while maintaining a fixed NGD. By properly choosing the gain coefficient, the proposed circuit can exhibit the same S_{21} as an ideal NC network. From the experimental results, it can be calculated that in 1.4–1.55 GHz the NGD circuit can exhibit the desired equivalent NC value. In addition, thanks to the active structure, the circuit shows a high quality-factor (Q) performance.

Keywords: dispersion engineering, negative group delay, negative group velocity, non-Foster reactance

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

NGD, as an exotic electromagnetic phenomenon, results from the fact that superluminal velocity occurs at certain frequency band in which the derivative of the propagation phase with respect to frequency is positive [1]. In many applications, this can be used to compensate dispersion effects which are caused by positive group delay [2]. By this way, the system linearity characteristic can be improved [3, 4]. In addition, one of the useful and practical applications for NGD circuits is the realization of non-Foster circuit (NFC). This results from the fact that both NGD circuit and NFC have a positive phase slope with respect to frequency within the operating band [5].

In general, NFCs often refer to a capacitor or inductor that has negative value. Different from traditional Foster components, the NFCs can break Bode-Fano limit. This means that the matching network using NFC can achieve a wide bandwidth characteristic, which is particularly useful for matching high-Q electrically small antennas [6, 7].

However, it deserves to be noticed that most of these NFCs are implemented by networks that are built by lumped inductors, capacitors or resistors [8]. In the high frequency regime, these networks cannot show good performances anymore because of their parasitics. At the same time, the passive resistors also cause great loss, resulting in an extra-low Q factor. In this paper, a novel NGD circuit using a stepped-impedance DA is proposed. The transconductance (g_m) of transistors in different stages are same while the I/O impedances are different. An important feature of this proposed structure is that the gain can be configurable while the

NGD time still remains unchanged. By applying the proposed NGD circuit, a -2 pF equivalent series NC can be implemented. Measurement results show that the equivalent capacitance is quite close to an ideal NC with a high Q performance operating in 1.4–1.55 GHz.

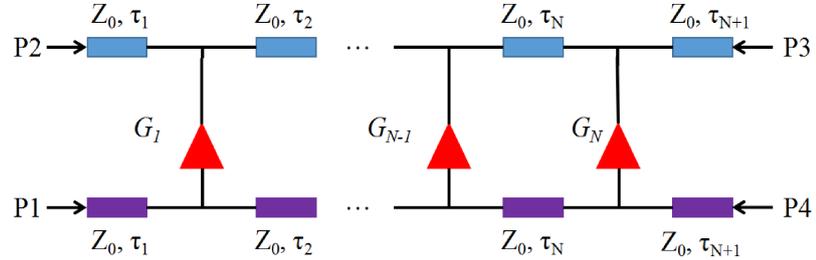


Fig. 1. Schematic of the NGD circuit based on DA

2 Theoretical analysis

Fig. 1 shows the structure of an NGD circuit based on an N -stage DA. The NGD phenomenon can be observed between P1 (input port) and P2 (reversed port). P3 and P4 are terminated with 50Ω loads. The k_{th} amplifier contributes the overall voltage gain as G_k . The delay time of the k_{th} drain and gate transmission lines are τ_k . The characteristic impedance of all transmission lines are Z_0 . The transfer function between P1 and P2 can be calculated as [9, 10]

$$H_{rev}(\omega) = \sum_{k=1}^N G_k \exp\left(-2j\omega \sum_{i=1}^k (\tau_k)\right). \quad (1)$$

According to the previous study [10, 11, 12], the NGD phenomenon can be obtained by adjusting G_k in different stages to satisfy the specified coefficient ratio. In the previous design, different G_k are achieved by controlling the bias voltages where the coefficient ratio is equal to the ratio of g_{mk} ; however, it is noted that g_m is very sensitive to the gate voltage, in which some fluctuation in the bias voltage may bring degradation to the overall NGD characteristics.

As an alternative to the original design, this paper applies the stepped-impedance DA topology to achieve the desired NGD characteristic. The schematic diagram of the proposed circuit is shown in Fig. 2. Different from Fig. 1, the characteristic impedance of the k_{th} transmission line is Z_k and all transistors have the same g_m .

In (1), G_k is the voltage gain amplitude of each stage, and it should be noted that G_k depends not only on g_m , but also on the I/O impedances of transistors. The impedances seen towards P2 and P3 are shown in Fig. 2 as $Z'_{out,k}$ and $Z_{out,k}$. For the theoretical analysis, it is assumed that all the transistors are ideal (the internal impedance is infinite) and the delay time of transmission lines are all $0.25T$, where T is the period of the input signal. According to the basic circuit theory, it can be calculated that for the k_{th} amplifier, its contribution to overall voltage gain is

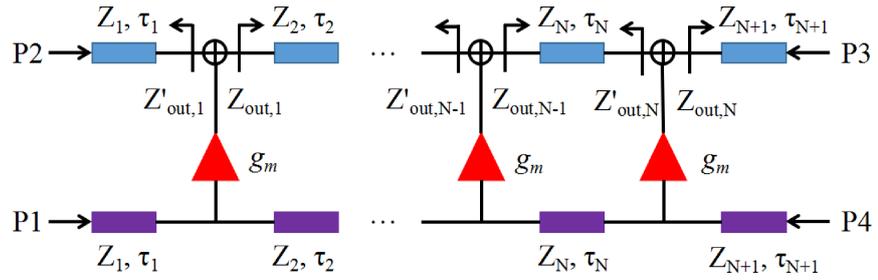


Fig. 2. Schematic of the proposed NGD with a stepped-impedance DA

$$G_k = g_m \frac{Z_{out,k}^2}{Z_{out,k} + Z'_{out,k}} \quad (2)$$

where

$$Z_{out,k} = \frac{Z_{k+1}^2}{Z_{out,k+1}} \quad (3)$$

$$Z'_{out,k} = \frac{Z_k^2}{Z'_{out,k-1}} \quad (4)$$

$$Z_{out,N+1} = Z'_{out,0} = Z_0 = 50 \Omega \quad (5)$$

From (2) to (5), it can be clearly seen by carefully adjusting the characteristic impedances of different stage transmission lines, a specific G_k ratio can be achieved under the same g_m condition. More importantly, this ratio no longer depends on g_m , resulting in a constant NGD time while the total gain can still be configurable. This feature is very useful in NC implementation as it is always desired to weaken the correlation between the NGD and gain/loss.

For proof-of-concept, Fig. 3 shows the simulated results of a two-stage NGD circuit based on the above theory. In this simulation, we set $Z_1 = Z_3 = 40 \Omega$, $Z_2 = 33.7 \Omega$ and $\tau_k = \tau_0 = 0.25T$. g_m varies from 0.18 mS to 0.58 mS. It can be seen from Fig. 3(a) that the circuit can exhibit a group delay of -1 ns at most, when the slope of phase is positive. Additionally, the gain between I/O ports increases when g_m increases, as shown in Fig. 3(b). It is worth mentioning that the group delay response remains unchanged as shown in Fig. 3(a) under different g_m conditions. These results are in good agreement with our previous theoretical analysis.

Based on the theory above, the implementation of the proposed NC circuit will be described as follows: It is noted that for a non-Foster two-port network, the relationship between S_{21} and non-Foster impedance Z_{NF} is [8]

$$S_{21} = \frac{2Z_0}{2Z_0 + Z_{NF}} \rightarrow Z_{NF} = \frac{2Z_0(1 - S_{21})}{S_{21}} \quad (6)$$

In Z_{NF} , the imaginary part can be used to calculate the equivalent NC. The quality factor Q can be obtained from the ratio between the reactance and resistance of Z_{NF} . From (6), it is observed that if S_{21} of the proposed NGD circuit is same with the ideal series NC network, the equivalent process is possible.

However, it should be pointed out that an identical S_{21} is only the sufficient but not necessary condition to obtain the specific NC. From (6), if Z_{NF} has a large real part when the imaginary part is unchanged, NC can still be calculated out but

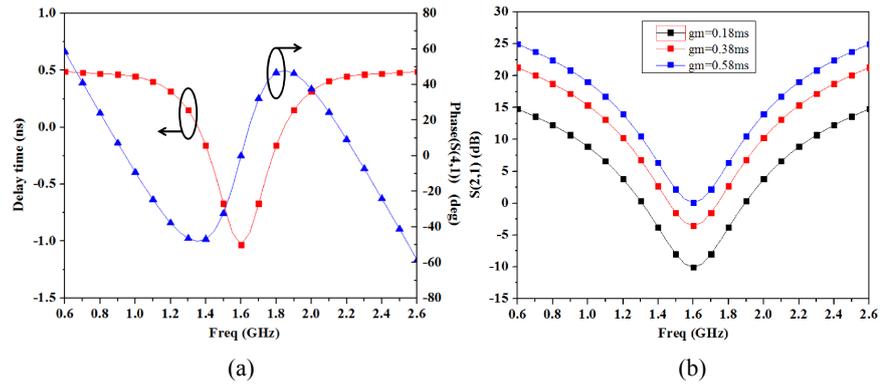


Fig. 3. Simulation results of the proposed NGD circuit
(a) Phase and delay time (b) Gain/loss performance

the S-parameter will be quite different from the ideal network. The equivalent circuit will include other components such as resistors. The delay time may even be positive because of these resistors. Accordingly, in order to achieve a pure equivalent series NC, the same S_{21} condition is required.

3 Measurement results

To validate the proposed concept, the entire circuit is fabricated using PCB substrate RF60 with a thickness of 0.76 mm, as shown in Fig. 4. The NGD circuit is based on a two-stage DA structure, and Avago's enhancement mode HEMT, ATF50189, is used here as the active device to achieve high g_m . A shunt inductor is used at the gate of the transistor to ensure the unconditionally stability throughout the entire band (0–20 GHz). The widths of Line 1 and 3 are both 0.74 mm and the width of Line 2 is 1 mm. The length of all lines are 21 mm. In addition, the drain bias (VDD) is 7 V, and the gate bias (VG) is 0.37 V. I_D is about 130 mA.

Fig. 5 shows the simulated and measured amplitude and phase performance of S_{21} . It is seen that comparing with the ideal NC, the measured gain error is less than 1.3 dB and phase error is less than 6° in 1.4–1.55 GHz, indicating a good agreement.

Fig. 6 shows the equivalent NC value derived from the measured S_{21} . It can be seen from Fig. 6(a) that the calculated capacitance value is close to -2 pF when the

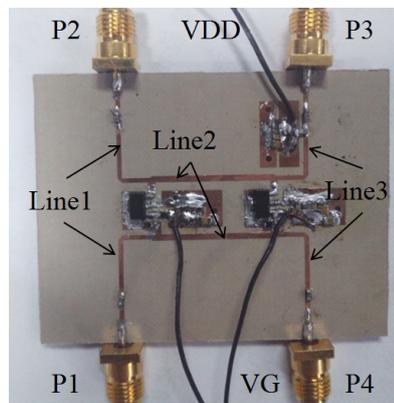


Fig. 4. Photograph of the proposed NC circuit

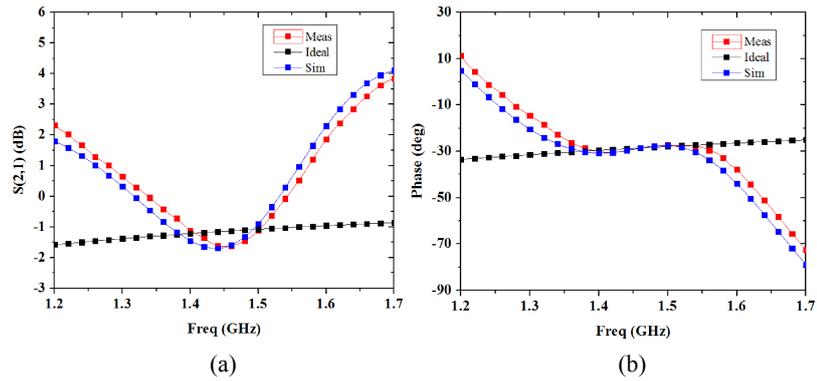


Fig. 5. Measurement results of the proposed NC circuit
(a) Gain/loss performance (b) Phase performance

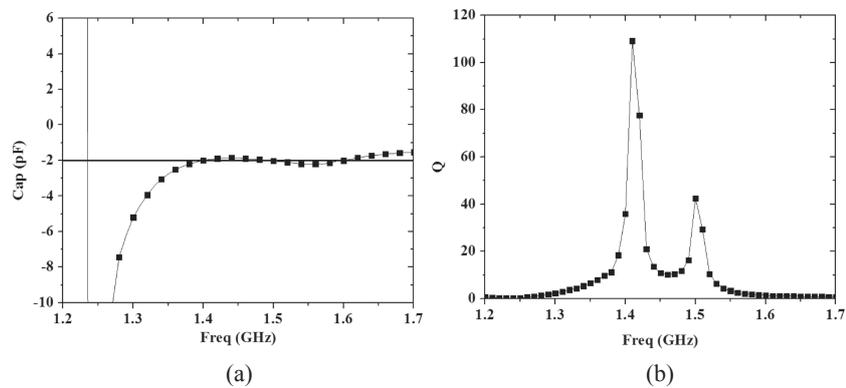


Fig. 6. Component values calculated from measured data
(a) Equivalent NC value (b) Quality factor

frequency is greater than 1.4 GHz. But according to our explanation above, the equivalent process is considered valid only in 1.4–1.55 GHz where S_{21} is identical with ideal NC. In Fig. 6(b), an extra low Q factor in 1.6–1.7 GHz proves that the calculated Z_{NF} indeed has a great real part.

From Fig. 6(b), it can be seen that the Q factor of the circuit reaches 110 and 42 at 1.41 GHz and 1.5 GHz respectively. Comparing this result with the curve in Fig. 5, it can be seen that these two frequency points are exactly where the measured S_{21} coincides with the ideal NC.

4 Conclusion

A novel approach to achieve a non-Foster NC is proposed in this work. An NGD circuit based on a stepped-impedance DA is used to achieve the desired S-parameter response of the desired non-Foster element. By this way, the NGD time of proposed circuit is stable, while the gain performance is configurable. This provides the possibility to achieve a stable NC value. The measurement results show that the circuit can obtain a series capacitance of -2 pF in 1.4–1.55 GHz with a maximum Q of 110.