

A wide-band monolithic differential power amplifier

Ting Tian¹, Xiaodong Zhang^{2a}), Huai Gao³, and Shengli Lu¹

¹ National ASIC System Engineering Center, Southeast University, Nanjing

² School of Electronic & Information Engineering, Suzhou University of Science and Technology, Suzhou

³ Suzhou Innotion Tech. Co., Ltd., Suzhou

a) zhangxd_usts@126.com

Abstract: A differential PA (power amplifier) with a novel structure is introduced in this paper. This PA is constructed with single ended input and balanced output. It is fabricated in 2 μm InGaP/GaAs HBT technology. The small-signal bandwidth of this PA covers from 1.5 GHz to 2.7 GHz. 34 dBm $P_{-1\text{dB}}$ (1 dB gain-compression power) and 45% PAE (power added efficiency) is achieved at 2.1 GHz. Moreover, the quiescent power dissipation is 400 mW with 12 V supply.

Keywords: differential, push-pull, power amplifier, InGaP/GaAs HBT

Classification: Electron devices, circuits and modules

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1 Introduction

With continuing growth of personal communications, the number of portable devices with wireless connectivity has increased rapidly. Currently, in the portable devices, a single ended PA feeding an unbalanced antenna is a preferred scheme for the circuit designers. However, this unbalanced design generates a current flow on the ground plane. External objects, such as a human's hand, easily impact the current, the radiation performance of the system is degraded. To solve this problem, an obviously substituted method is using the differential PA and the balanced antenna [1]. It's well known that differential circuits offer an improved linearity and enhanced CMRR (common-mode rejection ratio) [2].

The push-pull amplifier is a basic building block for differential PA. But the research on push-pull amplifier with a complementary P-n-p/N-p-n InGaP/GaAs HBT pair appears being ignored due to the complexity in fabrication [3, 4, 5, 6]. A high-efficiency class-AB pseudo-push-pull amplifier designed with N-p-n HBTs alone can be realized by using a 180-degree phase splitters (or baluns) [7, 8]. Due to the incomplete symmetry of the two branches, the difference in output signal between the positive and negative half-cycle of the waveform is relatively obvious. The use of a differential topology can improve the above phenomenon.

In this paper, a novel monolithic differential PA with single ended input and balanced output is proposed. The PA is fabricated in 2 μ m InGaP/GaAs HBT technology, which achieves a bandwidth from 1.5 GHz to 2.1 GHz, a P_{-1dB} of 34 dBm and PAE of 45% at 2.1 GHz. The output stage of the PA is biased on class AB, so the PA has a low quiescent current and dissipates only 400 mW quiescent power with 12 V supply.

2 Circuit design

2.1 Circuit topology

The circuit architecture of the proposed differential PA is shown in Fig. 1. This differential PA consists of an input stage and two push-pull amplifiers. A1, A2, Q1 and Q2 compose a push-pull amplifier. Another exactly same push-pull circuit includes A3, A4, Q3 and Q4. A0 is the input stage which drives the next two push-pull amplifiers with opposite phase.

In the positive half cycle of the input signal, the transistor Q1 and Q4 are turned on. Simultaneously, the transistor Q2 and Q3 are turned off. Thus, the current flows from Q1 to Q4. On the contrary, the current flows from Q3 to Q2 in the negative half cycle of the input signal.

2.2 Push-pull amplifier

Fig. 2 presents the schematic of push-pull amplifier. This is a wide-band Class AB amplifier. Power device Q1 and Q2 are the last output stage. Q5 is a common

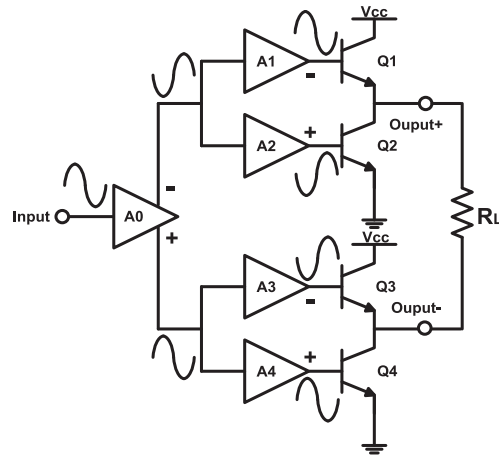


Fig. 1. Simplified circuit topology structure

emitter amplifier, as the inverse amplifier A1 in Fig. 1, which drives Q1. Q6 is an emitter follower, as the amplifier A2 in Fig. 1, which drives Q2. D1 and C1 are used to shift the DC input level of Q5. Thus, Q5 and Q6 can share a bias circuit composed by Q7, Q8, Q9 and D2. To achieve high power efficiency, the circuit is designed for a low idling current of 15 mA in Q1 and Q2, by adjusting the resistor R2, R3 and R4.

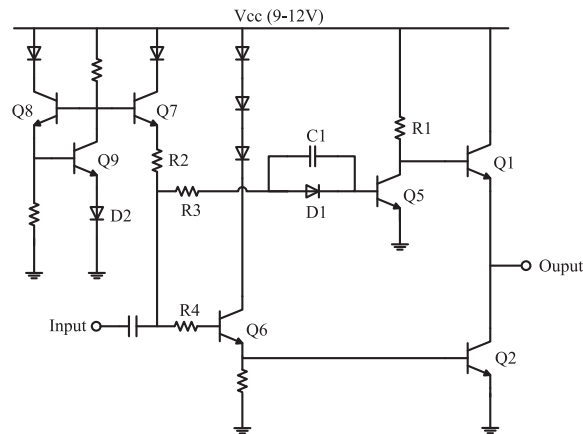


Fig. 2. Schematic of push-pull amplifier

Obviously, in the push-pull amplifier, the two half-cycles are magnified by different circuits. So it is impossible to make the voltage gain of two half-cycles equal in the whole temperature range and frequency range. However, the proposed differential PA in Fig. 1 allows preventing from the difference between the positive and negative half-cycle of the output waveform. Fig. 3 shows the simulated results of the output waveform of the push-pull structure and differential structure. With a 7 dBm input power at 2.1 GHz, the difference in output signal between the positive and negative half-cycle of the waveform of the push-pull structure is 1.357 V, while 0.919 V of the differential structure.

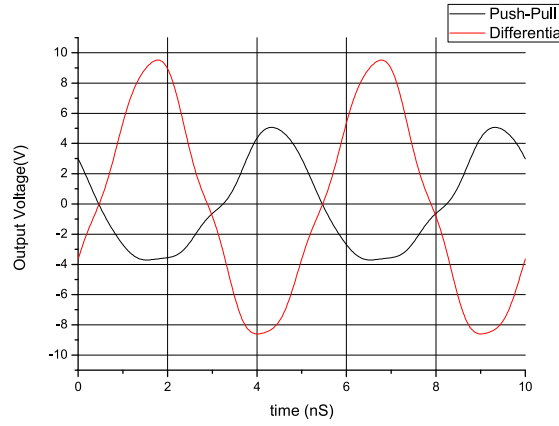


Fig. 3. Output signal of the push-pull and differential structure

2.3 Input stage design

The PA's first stage is shown in Fig. 4. In this circuit, R3, R4 and D2 offer the bias voltage for the transistor Q0. The signals v_- and v_+ output from the collector and emitter of transistor Q0 separately. If the base current of Q0 can be ignored, the signals v_- and v_+ will swing with same amplitude and opposite phase, when the resistor R5 equals to R6. However, in order to acquire the better performance in high frequency, the base-emitter and base-collector junction capacitance in Q0 have to be taken into account.

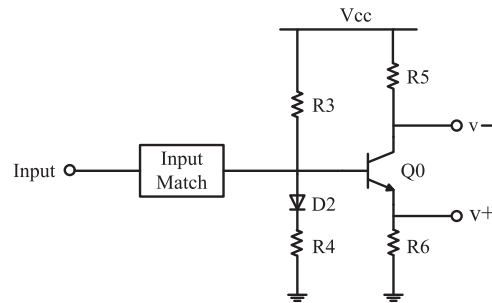


Fig. 4. Schematic of input stage

The elements in Fig. 5 are as follows.

- 1) g_{be} and C_{be} are base-emitter conductance and capacitance of Q0.
- 2) C_{bc} is base-collector capacitance of Q0.
- 3) r_{bb} and g_m are intrinsic base resistance and transconductance of Q0.
- 4) R5 and R6 are the impedance connected with collector and emitter.
- 5) r_{pp} and C_{pp} are the input resistance and input capacitance of the following push-pull amplifier.

The parameters of the input stage equivalent circuit are shown in Table I.

Write the following equations using Kirchoff's current laws (KCL):

$$\begin{cases} -v_e Y_e + (v_{b'} - v_e)(g_m + g_{be} + sC_{be}) = 0 \\ (v_c - v_{b'})sC_{bc} + v_c Y_c + (v_{b'} - v_e)g_m = 0 \end{cases} \quad (1)$$

Based on the KCL above, in order to satisfy the requirement of $v_e = -v_c$, formula (2) can be derived. According to formula (2) and the parameters in Table I,

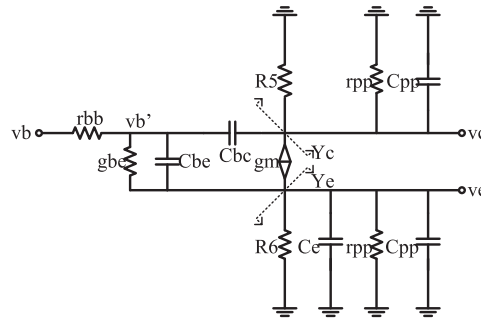


Fig. 5. Equivalent circuit of input stage

Table I. Parameters of the equivalent circuit

gbe	gm	Cbe	Cbc	rpp	Cpp	R5	R6
0.84 mS	66 mS	0.42 pf	0.04 pf	83 ohm	0.21 pf	80 ohm	80 ohm

a small capacitance C_e (0.26 pf) shunted beside the resistance R_6 can lead to better symmetry between v_e and v_c

$$Y_e - Y_c = \frac{Y_c(g_{be} + sC_{be} + sC_{bc}) + 2sC_{bc}(g_m + g_{be} + sC_{be})}{g_m - sC_{bc}} \quad (2)$$

2.4 Input matching

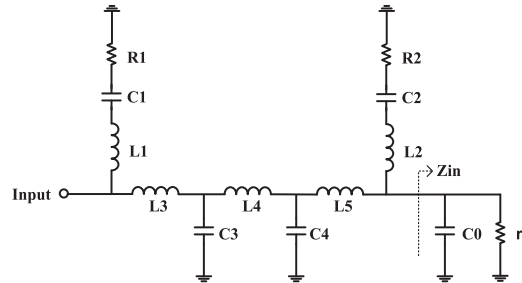


Fig. 6. Equivalent circuit of input matching

A traveling wave matching structure is used to enhance the bandwidth of amplifier [9, 10]. The input matching equivalent circuit is shown in Fig. 6. The input impedance of input stage can be simplified as parallel C_0 and r_0 . For broadband input impedance matching, a tapered artificial transmission line with three sections is introduced before the input stage. The equivalent capacitance C_0 is incorporated with the on chip lumped elements, L_3 , L_4 , L_5 , C_3 and C_4 , to form the lossless artificial transmission line. The characteristic impedance of the line sections, r_1 , r_2 and r_3 , are determined by the following.

$$r_3 = r_0 = \sqrt{\frac{L_5}{C_0}}, \quad r_1 = r_s = \sqrt{\frac{L_3}{C_3}}, \quad r_2 = \sqrt{r_1 r_3} = \sqrt{\frac{L_4}{C_4}}$$

Where, r_s is the input source impedance.

The parameters of the input matching circuit are shown in Table II.

Table II. Parameters of the input matching circuit

r_s	r_0	C0	C3	C4	L3	L4	L5
50 ohm	120 ohm	0.3 pf	0.3 pf	0.3 pf	0.75 nH	1.8 nH	4.32 nH

Furthermore, two RLC compensation network are connected to the artificial transmission line, which form an M-Type filter to improve the matching performance for high and low frequency band. The high frequency compensation network is composed of L1, C1, and R1. The low frequency compensation network is composed of L2, C2, and R2.

2.5 Output matching

This differential PA is with balanced output. The measurement system is generally single-ended system. Transmission-line transformers are well known for their wide bandwidth. So, in the output matching, a 1:4 transformer manufactured by RFMD, RFXF8553 is employed as a double-end and single-end conversion circuit.

3 Measurement result

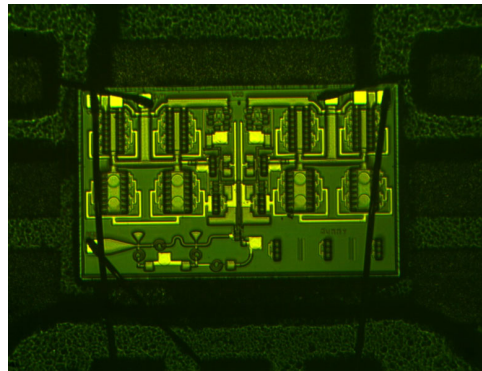


Fig. 7. Die photo of the proposed differential PA

The proposed differential PA was implemented in a commercial InGaP/GaAs HBT technology. The HBT emitter area is $2 \times 20 \mu\text{m}^2$. The chip size is $0.9 \times 1.5 \text{ mm}^2$. The die photo is shown in Fig. 7.

The measurement broadband small signal gain and return loss are plotted in Fig. 8(a). The small signal gain is 27 dB at 2.1 GHz and the input return loss is better than 15 dB from 1.78 GHz to 2.67 GHz. Fig. 8(b) shows the measurement results of power gain vs. input power at three typical frequencies. Fig. 8(c) shows the measurement result of the 1-dB output power vs. frequency. Fig. 8(d) shows the measurement result of PAE vs. output power. 34 dBm P-1 dB and 45% PAE is achieved at 2.1 GHz.

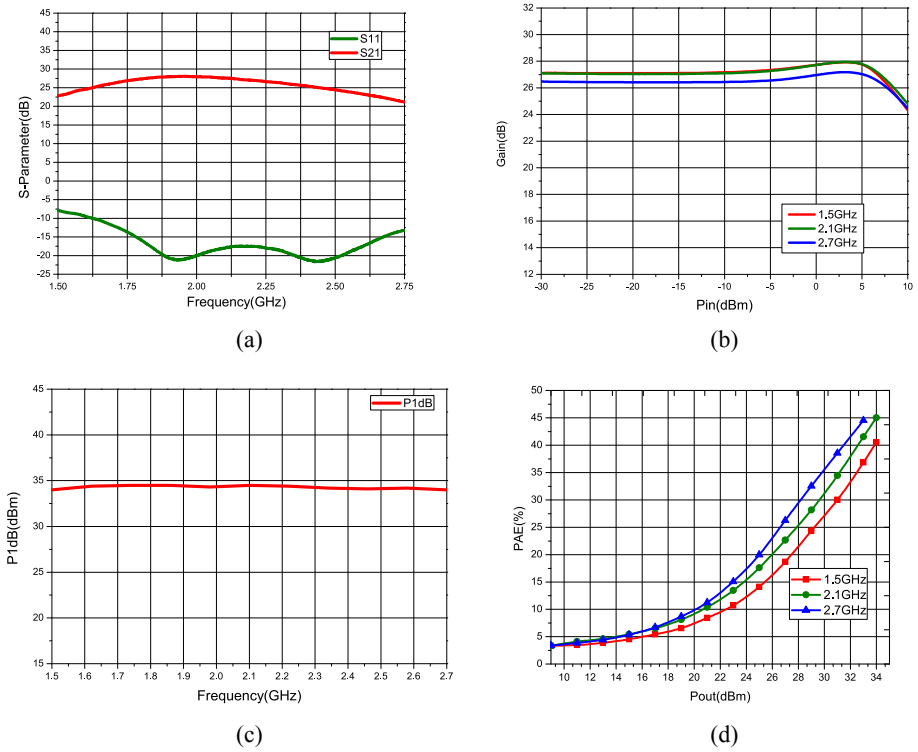


Fig. 8. (a) Broadband gain & return loss. (b) Power gain vs. input power. (c) P_{1dB} vs. frequency. (d) PAE vs. output power.

4 Conclusion

In this letter, a novel differential PA fabricated in $2\mu\text{m}$ InGaP/GaAs HBT technology is proposed. It is target for a wide band frequency application from 1.5 GHz to 2.7 GHz. The novel differential PA consists of an input stage and two push-pull amplifiers. Only N-type active devices are used in circuit design. 34 dBm P_{1dB} and 45% PAE are achieved at 2.1 GHz.