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Design and analysis of Z-source based 7 level cascaded multi level inverter for induction motor

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Abstract: Multilevel inverter, a powerful electronic device capable of supplying desired alternating voltage level, is a renowned device majorly employed in appliances such as UPS systems, huge drives of induction motors as well as Transmission Systems. Multilevel inverters acquires the wanted output of their voltage from varied DC voltage sources. Thus, the number of DC voltage sources is directly proportional to the level of output voltage procured by the inverter. Multilevel inverters are constituted with several major advantages like, better harmonic performance, lower semi-conductor voltage stress, lower Electro Magnetic Interference (EMI) and diminished losses on account of switching. However, in spite of these, their output voltage runs in accordance with the input from DC sources. Hence, to avoid such limitation there is requirement for an intermediate DC to DC converter in order to boost the working of the MLI output voltage. Thus, in accordance with the above limitation, a seven-level cascaded Z-source based multilevel inverter is proposed for this task. MATLAB/Simulink power system toolbox has been employed for the proposed system, in consequent of which experimental findings are analyzed to attest the efficiency of the method.

Keywords: cascaded multilevel inverter, Z-source inverter, induction motor, multi carrier CDPWM, FPGA

Classification: Power devices and circuits

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1 Introduction

With time, there is an apparent widespread use of induction motors in various industries. In order to achieve high productivity and enhanced accuracy, various speed induction motors require alternating torque dynamics, ranging from high to low [1]. A variable speed induction motor is comprised of two control schemes, specifically, FOC or the Field Oriented Control and the DTC or the Direct Torque Control. Comparing both the schemes, DTC is much more effective to control induction machines. Unlike FOC, DTC implementation minimizes the machine parameters and is comprised of quick transient response characteristics. However, both these techniques showcase ripples at high torque, are able to flux value and result in high acoustic noise. Power electronics has been acquainted with a recent development as per which steps have been take to improve the level of inverter and uplift its status rather than the mere increase of its filter [2, 3, 4]. By using single or multiple DC voltage sources, the Multi-level inverter is able to integrate a vital output voltage which produces 'n' output levels. As levels increase, the disparity between each voltage step decreases, which consequently lead to reduction in the total harmonic distortion (THD) [5, 6].

There is classification among the multilevel inverters in three different configurations, namely, Multilevel inverters with cascaded H-bridge, Diode-Clamped, Flying Capacitor [7, 8]. Distinctive perks of these inverters include high power

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quality, satisfactory electromagnetic compatibility and the skill to eliminate coupling transformers at the nascent stage of voltage level distribution, which makes it cost-effective in principle. No output voltage levels can increase beyond the DC voltage source, thus, to further the boost of DC voltage converters such as D-DC must be used. However, additional components are required to uplift the voltage and this happens usually in the form of two stage converters. Nonetheless, with the employment of Z-source network instead of dc-dc converters can boost the output voltage in a single stage. Z-source MLI is capable of boosting the voltage as it comprises of an impedance circuit which forms a link between the power source and inverter circuitry. This distinctive feature cannot be replicated in the traditional Voltage Source Inverter (VSI), which utilizes a capacitor and Current Source Inverter (CSI) [2, 3]. This work aims to present a novel multilevel inverter system for Induction Motor, by conveniently using Z network to boost operation between the DC source and circuitry of the inverter. Modulation index and a shoot through control method is useful in maintaining the output voltage of the proposed inverter. Cascaded Z-Source Multilevel inverter is studied with third harmonic injection PWM technique and its performance measures are evaluated throughout the course of this study. The results of the Cascaded Multilevel inverter of Z-source is compared with traditional cascaded multilevel inverter to formulate an apt analysis based on their respective performances. Simulation of circuit configuration is done with MATLAB/SIMULINK design, and the generated findings are also aptly rechecked by this experiment. Methodology for the system proposed here.

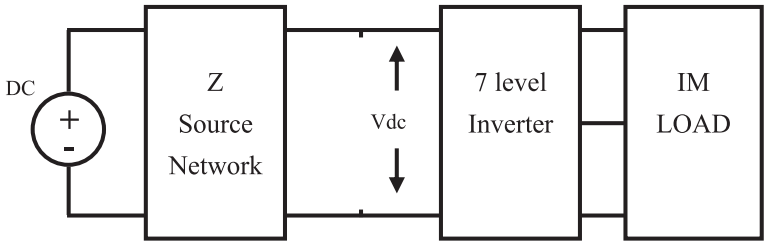

Fig. 1. Block diagram of the proposed system

Fig. 1 shows the proposed system's block diagram representation. The proposed system uses the Z network in between the proposed system's inverter circuit and the DC source. The output voltage is managed via the modulation index, and the Z-Source Multilevel inverter is assessed using SVPWM technique.

2 Z-Source network

Fig. 2(a) indicates the Z-source topology's proposed basic unit.

The above figure comprises of a DC voltage source, Z impedance with one switch S7 and Diode DS. It manipulates through two states: non shoot-through and shoot through state [4].

Diode DS has to be switched off and switch S7 has to be switched on for the shoot through stage and the apparent voltage for Z network is zero. The shoot-through pulse is obtained by contrasting DC reference line and the triangular carrier wave.

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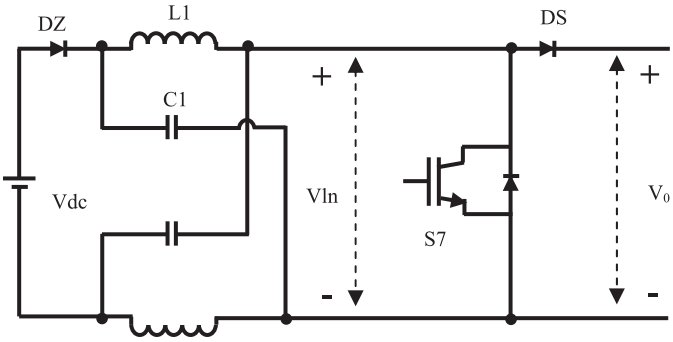

Fig. 2. (a) Single phase proposed basic unit

i) Shoot-through state:

The Shoot through state's equivalent circuit is represented in Fig. 2(b).

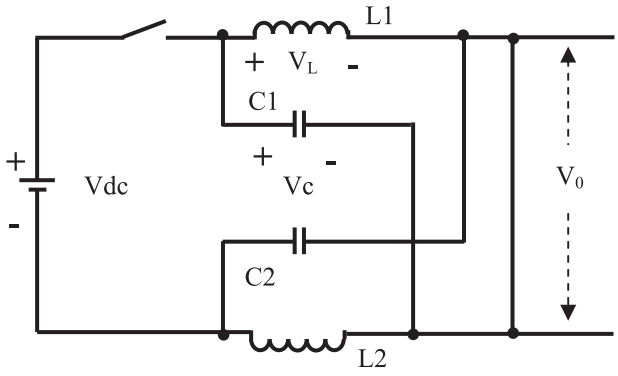

Fig. 2. (b) Basic unit in shoot through state

The circuit's 2(b) analysis is indicated as follows:

$$V_L = V_c \tag{1}$$

$$V_{in} = 0 \tag{2}$$

ii) Non-shoot through stage:

Non-shoot through stage's equivalent circuit is represented in Fig. 2(c).

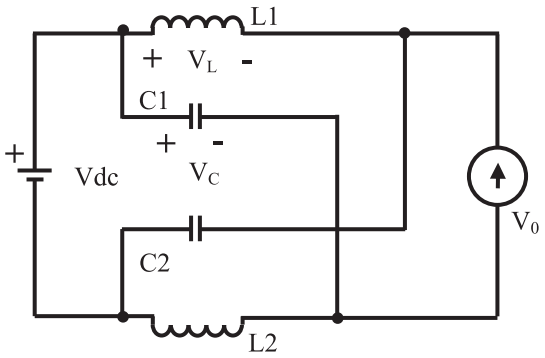

Fig. 2. (c) Basic unit in non-shoot through state

The calculation of LC networks output and voltage of inductors is as follows:

$$C1 = C2, L1 = L2 \quad V_L = V_{dc} - V_c \tag{3}$$

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$$V_{in} = V_c - V_L \quad (4)$$

$$V_{in} = 2V_c - V_{dc} \quad (5)$$

3 Multilevel inverter topology

The multilevel topology involves single phased inverter units of H bridges, voltage sources based on DC and Z impedances. Each H-bridge Z-Source inverter is capable of generating three output voltage: +Vin, 0, −Vin [9, 10].

Such type of converter doesn't involve the need for clamping diodes, flying capacitors or transformers. Voltage outputs are different for every level like +Vdc, 0 and −Vdc, when the DC sources are linked with the AC ones on the output side when four switches are used in varied combinations. The sum of all the distinctive inverter outputs is the combined output voltage in case of a multi-level inverter. Only at the fundamental frequency, all the H-Bridges active devices switches and manages to generate an apparent-square waveform by oscillating between the positive and the phase legs. Furthermore, every switching device conducts itself for 180° (or half cycle) nevertheless of the pulse width of the quasi-square wave. The present stress in every device that is active is determined by this switching method. This topology is efficient in conversion of power and for higher voltages due to its capacity of synthesizing waveforms with superior harmonic spectrum and switching frequency at a lower level. There are main four advantages of using a multilevel inverter; due to the series connection of the switch the voltage stress on each switch decreases, thus making it possible to increase the voltage and the inverter power consequently; there is an apparent decrease in the rate of voltage change (dV/dt) due to the lower voltage swing of every oscillating cycle in the switch; the reduction in harmonic distortion and the retrieval of diminished EMI or the Electro Magnetic Interference and the acoustic noise.

PWM modulation

It is relatively easy to apply the SVM technique for all multilevel inverters. Two-, three-, and five-level inverters and their space vectors can be represented by way of Fig. 3. These vector diagrams are universal in occurrence and hence are not subjective to various types of multilevel inverter. By calculating the computing duty cycle for each vector (Tj,Tj + 1, and Tj + 2), a voltage vector can be profitably synthesized by adjacent three vectors. Thus,

$$V^* = ((TjVj + Tj + 1Vj + 1 + Tj + 2Vj + 2))/T \quad (6)$$

There are several features which encompass space-vector PWM methods, for instance, low current ripple, apt implementation of dc-link voltage, and an eased hardware execution by a digital signal processor (DSP). PWM methods are made a desirable fit for the high power and voltage applications with the help of these features. With the increase in levels, there is a dramatic consequent increase in the unnecessary stages in switching and the difficulty of choosing them. Various authors attempted to control ripples and easily control ripples by attempting a phase shift of five level space-vector diagrams into two diagrams of three levels each. Moreover, it was found that without the need for calculation of the duty cycle for the consecutive three vector, a simple vector method could be instituted.

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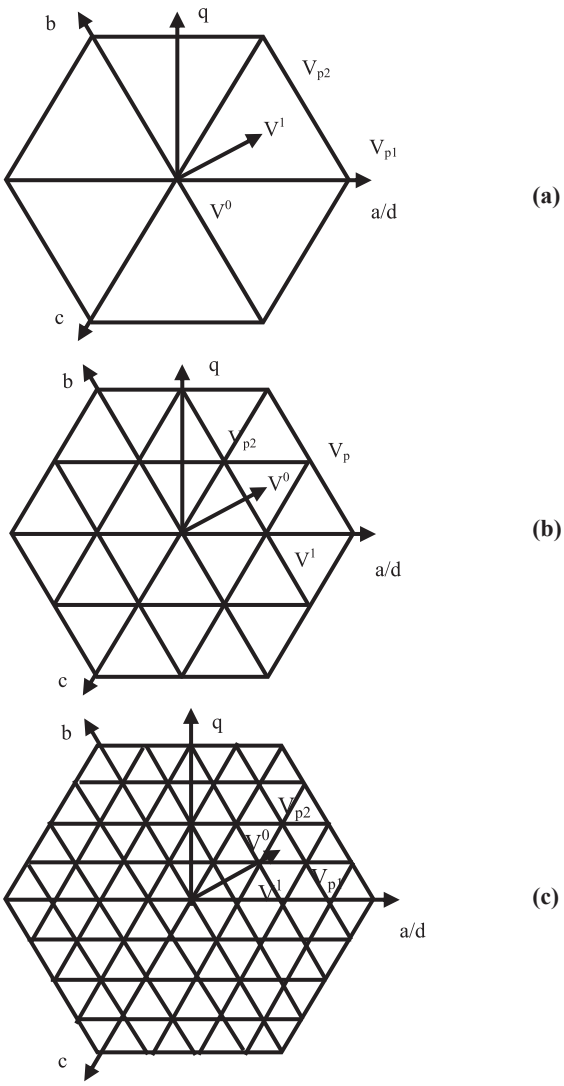

Fig. 3. Space-vector diagrams: (a) two-level, (b) three-level, and (c) five-level inverter

4 Simulation results

A voltage of 150 V DC is applied to each H-bridge configuration to get an output voltage of 450 V. The output is assessed using the scope block which is used to give the output of the simulated circuit in MATLAB. A sine wave of amplitude 3 and frequency 2*pi*150 act as the reference signal, and is used for comparison by repeating sequence block parameter with a triangular carrier signal. The modulation index of the reference signal and comparator signal is 0.8. The output signal is obtained when comprator signal is lower than the reference signal which is given to the gate section of the MOSFET's or IGBT's used as switches. Here a sine wave of amplitude 3 and frequency 2*pi*150 is observed in comparison to a triangular carrier signal. To obtain the triangular carrier signal of 180° phase shift is obtained by using repeating sequence as shown in Fig. 4.

5 Performance analysis

The efficiency of proposed system is analyzed in the order of harmonics, form factor and crest factor. THD, total harmonic distortion, is a calculation of the

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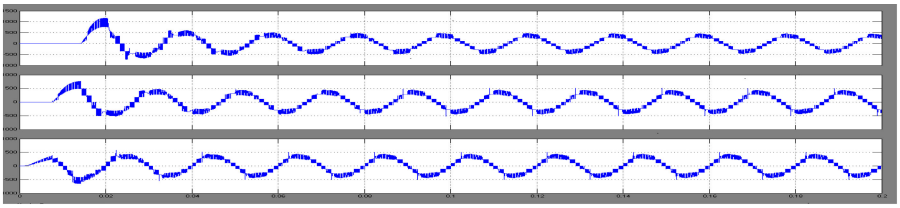

Fig. 4. Output voltage of the inverter

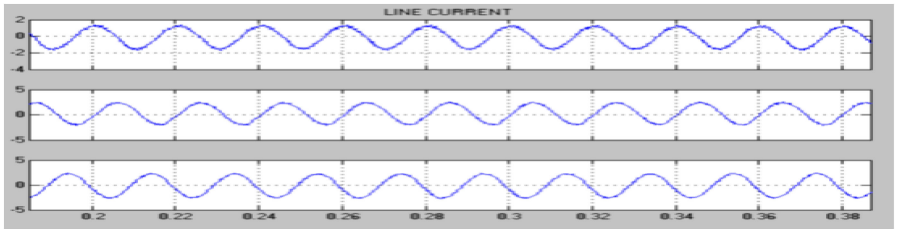

Fig. 5. Line current of the inverter

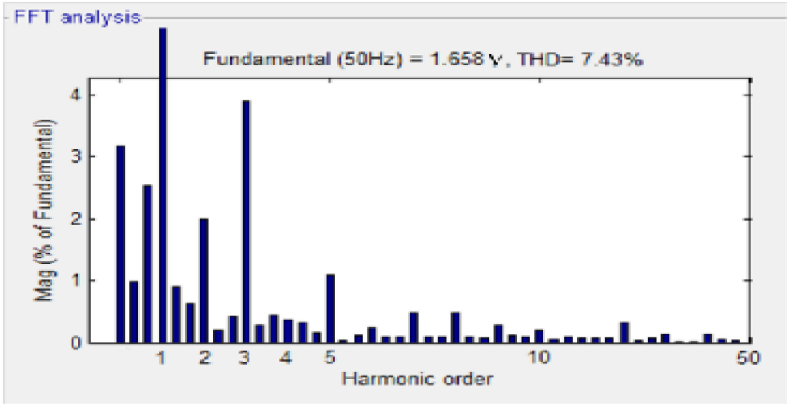

Fig. 6. Total harmonic distortion of Z-source inverter

harmonic distortion in existence. It is the ratio of the powers of harmonic components summed together to the fundamental frequency power in a signal.

From the Fig. 6, the THD is found to be 7.43%. It is evident that the amplitude of the key harmonics as well as its sidebands are diminished by the modulation technique. There by implying that the process of filtering is much easier, and smaller in size.

6 Experimental results

6.1 Parameters of ZSI based test system

The performance of the current approach is validated with laboratory prototype. Following parameters are considered in the ZSI based test system.

L1 = L2 = 1.0 mH

C1 = C2 = 1.3 mF

Input Voltage = 260 V

Cut off frequency = 1 kHz

Modulation index for Simple Boost Control & Constant Maximum Boost Control = 0.812

Modulation index for Maximum Boost Control = 1

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6.2 1HP AC induction motor parameters

Power----------746WATTS
Voltage----------200V, DELTA CONNECTION
Current----------1.8A
Pole----------4POLE
Frequency---------50HZ
Speed----------1435RPM
Stator Resistance (Rs)----------19.35OHM
Rotor Resistance (Rr)----------8.04OHM
Stator Inductance (Ls)----------0.032H
Rotor Inductance (Lr)----------0.032H
Mutual Inductance (Lm)----------0.601H

The experimental set up of the proposed inverter is shown in Fig. 7. Multi-carrier CDPWM strategy phase disposition is implemented in this proposed inverter. AHMY_SP6_LX9_LC is an easy to use FPGA Low cost board featuring Xilinx Spartan-6 FPGA, which is exclusively designed for research, experimenting and learning system design with FPGAs. These devices are built on 45 mn technology and are the most viable cost-effective FPGAs available. The experimental results of the input and output voltage in non-shoot through mode operation are presented below.

Fig. 7. Experimental setup of Z source 7-level cascaded inverter

Case-1: Response of Induction motor for speed of 500 RPM

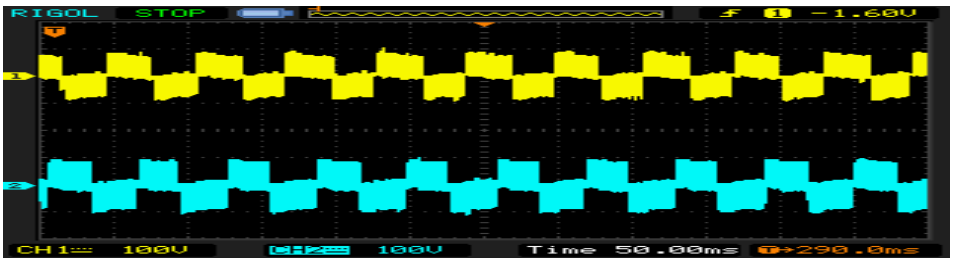

Fig. 8. Output voltage response of Z source seven-level cascaded inverter (V_{rn} and V_{bn})

Fig. 8 and 9 represent the Z-source inverter's recaptured waveforms at 500 RPM. Thus, the proposed PWM scheme leads to switching all the fundamental cycle which in turn results in more desirable quality and low output current ripple.

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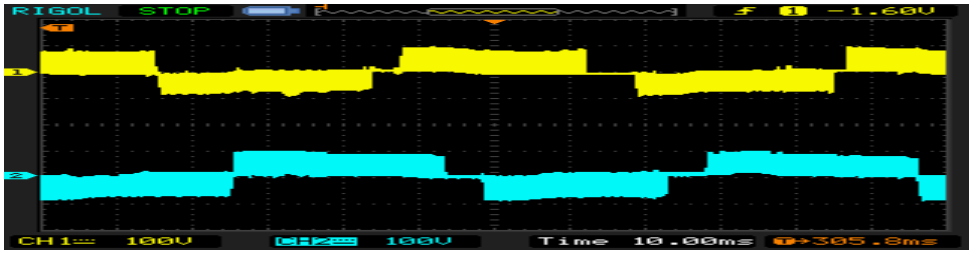

Fig. 9. Output voltage response of Z source seven-level cascaded inverter (V_{rn} and V_{yn})

Case-2: Response of Induction motor for speed of 1200 RPM

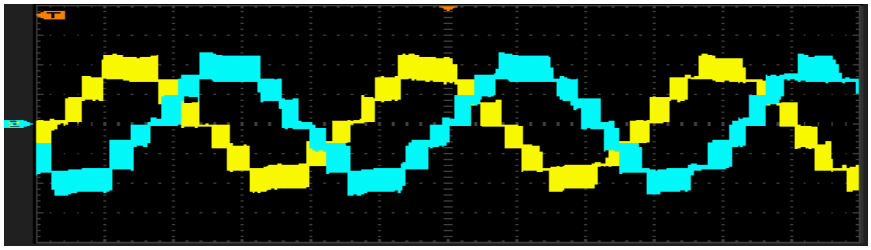

Fig. 10. Output voltage response of Z source seven-level cascaded inverter (V_{an} and V_{bn})

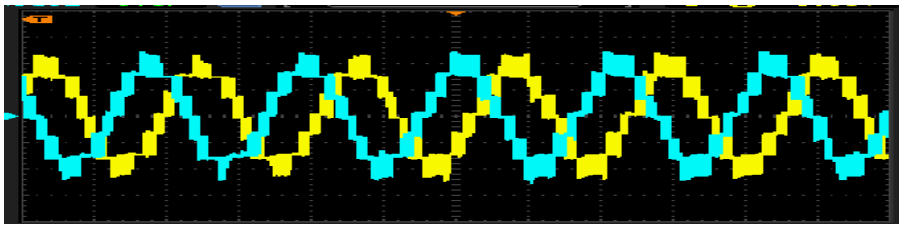

Fig. 11. Output voltage response of Z source seven-level cascaded inverter (V_{an} and V_{cn})

Fig. 10 and 11 display the recaptured waveforms of Z-source inverter at 1200 RPM. Initially the speed of induction motor increases linearly, as a result, in order to maintain torque, more current is used by the motor. The induction motor can reach up to a maximum speed of 1200 rpm under steady conditions of its state.

The switching states for Z-source seven level cascaded inverter shown in Fig. 12.

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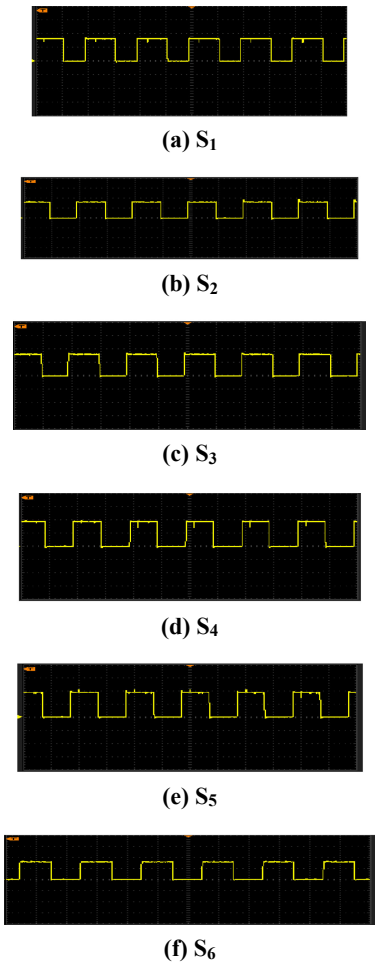

Fig. 12. Switching sequences of Z source seven-level cascaded inverter
(a)–(f) shows the Switching sequences of Z source seven-level cascaded inverter

7 Conclusion

Multilevel Inverter (MLI) is considered a desirable topology associated with the high voltage DC-AC conversions, it is successfully able to maintain the required voltage wave shape from varied DC voltage levels. However, one of major disadvantage of MLI is the limitation of its output voltage to DC sources voltage summation. Thus, a seven-level cascaded Z-Source multilevel inverters has been recommended to overcome this hurdle in the most significant manner. In this suggested topology, amplitude of output voltage can be augmented with the aid of Z network shoot-through (ST) state control. This scheme has presented itself with various advantageous properties, such as improved quality of spectral output, greater boost to voltage, element counts being passive and commutation going to nominal levels. This proposal with its verified properties and advantages can be successfully implemented for harnessing solar energy as well as controlling the fuel cell vehicle.

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