

Impact of adjacent transistors on the SEU sensitivity of DICE flip-flop

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Abstract: This paper studies the impact of adjacent transistors on the SEU sensitivity of the DICE flip-flop. We compare the SEU sensitivity of the DICE flip-flop with two different layout topologies. Heavy ion experiment results indicate the separation layout topology can reduce the SEU sensitivity of the DICE flip-flop, both in SEU threshold and SEU cross section. TCAD simulation is used to investigate the mechanisms. Simulation results indicate the higher charge collection capability of adjacent transistors in the separation layout topology is the main reason to reduce the SEU sensitivity.

Keywords: SEU, adjacent transistor, DICE flip-flop, cross section

Classification: Integrated circuits

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1 Introduction

Single-event upset (SEU) has become an important reliability concern for nanoscale technologies [1, 2]. Reduced nodal capacitance and supply voltage decrease the critical charge to cause SEU [3]. Close proximity of transistors results in charge sharing at multiple nodes [4]. These phenomena increase the SEU sensitivity of integrated circuits. Therefore, it is important to explore novel hardened techniques to mitigate the SEU sensitivity at advanced CMOS technologies.

Dual-interlocked cell (DICE) is widely used to mitigate the SEU sensitivity of flip-flops [5, 6, 7]. It was firstly described in [8] and it is immune to SEU caused by charge collection at a single node. However, because of the scaled technologies, charge sharing is becoming more and more prominent [9]. The adjacent transistors among the sensitive transistors also collect charge simultaneously, which may significantly affect the SEU sensitivity of the DICE flip-flop.

Therefore, this paper studies the impact of the adjacent transistors on the SEU sensitivity of the DICE flip-flop. Technology computer-aided design (TCAD) simulation is used to investigate the mechanisms. Heavy ion experiment is used to confirm the SEU sensitivity of the DICE flip-flop which is affected by the adjacent transistors. Simulation and experiment results indicate the adjacent transistors with different layout topologies significantly affect the SEU sensitivity of the DICE flip-flop.

2 The SEU sensitivity caused by adjacent transistors

The conventional DICE flip-flop considered in this paper is shown in Fig. 1. Although it is immune to charge collection at a single node, it can be upset if any sensitive node pair collect charge simultaneously. The DICE flip-flop has two conventional layout topologies, as shown in Fig. 2. Transistors are separated respectively in the first layout topology. It is called the separation layout topology. On the contrary, the transistors have the common source in the second layout topology. It is called the common layout topology.

Two conventional layout topologies result in the different SEU sensitivity of the DICE flip-flop. The main reason to cause this discrepancy is the different placements of the adjacent transistors. For instance, if the transistors at node *mn2* and

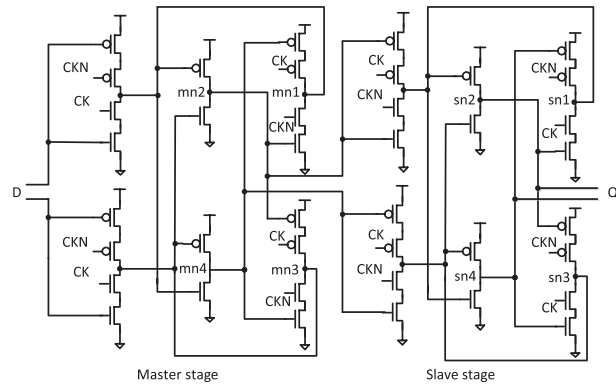


Fig. 1. The schematic of the conventional DICE flip-flop.

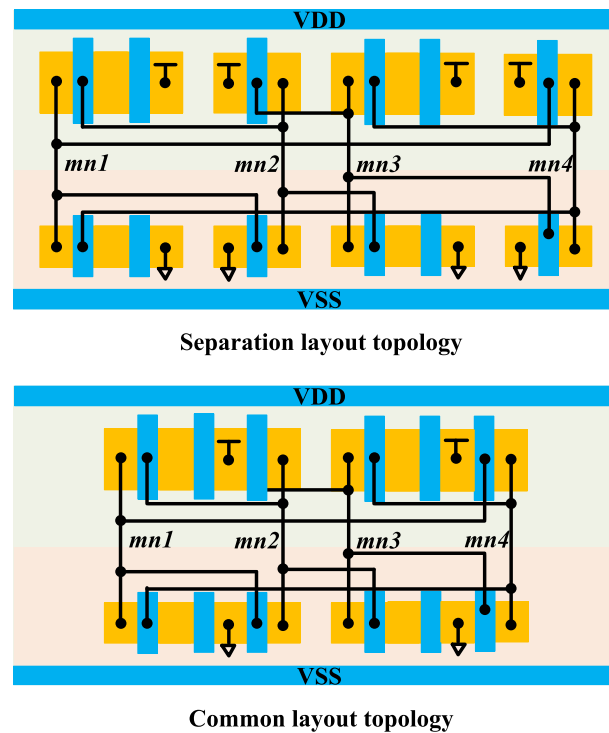


Fig. 2. The layout topologies of the conventional DICE flip-flop.

$mn4$ are the sensitive transistors, the transistors at the other nodes are the adjacent transistors, as shown in Fig. 3. When an incident ion strikes the sensitive transistor at node $mn2$, the other transistors also collect charge because of charge sharing. If the adjacent transistors can help to collect sufficient charge, the ionized carrier is hard to diffuse the other sensitive transistor at node $mn4$. For the common layout topology, only the drain regions of the adjacent transistors can help to collect charge. However, for the separation layout topology, the additional source regions of the adjacent transistors can also help to collect charge. Therefore, the charge collection capabilities of the adjacent transistors in two layout topologies are different. This discrepancy will significantly affect the collect charge of sensitive node pairs and finally affect the SEU sensitivity of the DICE flip-flop. Therefore, these layout topologies result in the different SEU sensitivity of the DICE flip-flop. The impact of the adjacent transistors on the SEU sensitivity should be considered.

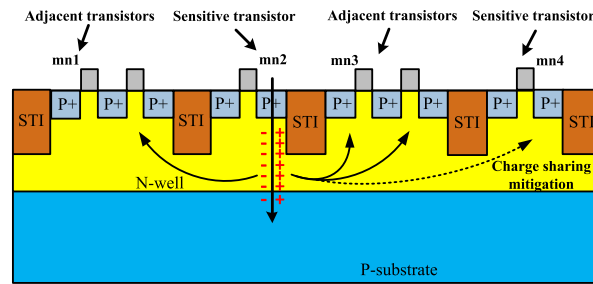


Fig. 3. Adjacent transistors help to collect charge and mitigate charge sharing.

3 Simulation setup and results

3.1 Simulation setup

In our previous works, TCAD simulation was a useful means to investigate the physical mechanism of single-event effect (SEE) [10, 11, 12]. In this paper, TCAD simulation was performed to compare the SEU sensitivity of the DICE flip-flop with two layout topologies. The DICE flip-flop with two layout topologies were represented as the TCAD models, as shown in Fig. 4. The PMOS and NMOS transistors in each TCAD model were calibrated to match electrical characteristics obtained from standard compact models. The transistor size, spacing and the well configuration were satisfied with the layout rules. The input and clock signals were set to 0. The incident locations were set to the sensitive transistors and the incident LET was set to $10 \text{ MeV} \cdot \text{cm}^2/\text{mg}$. The node voltages after each ion strikes were simulated to determine SEU.

Physical models used in TCAD simulation included Fermi-Dirac statistics, band-gap narrowing effect, Auger recombination, and doping dependent, electric field dependent, and carrier-carrier scattering mobility models. Unless otherwise specified, the default models and parameters were provided by Sentaurus TCAD vH-2013.03.

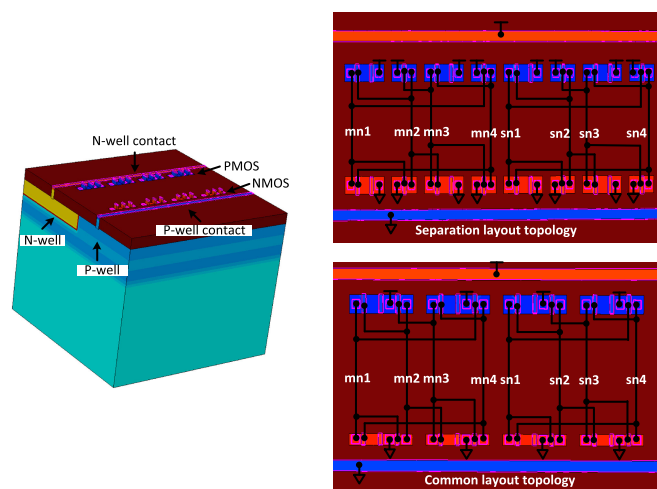


Fig. 4. The TCAD models with different layout topologies.

3.2 Simulation results

When the input and clock signals were set to 0, the PMOS transistors of node *mn2* and *mn4* were sensitive to SEE. If the sensitive PMOS transistors collect sufficient charge simultaneously, SEU occurs in the DICE flip-flop. Similarly, the NMOS transistors of node *mn1* and *mn3* were also sensitive to SEE and they can also result in SEU. Therefore, the incident location was set to the PMOS transistor of node *mn2* firstly to investigate PMOS transistors induced SEU.

The simulated transient voltages after particle strikes are shown in Fig. 5 and Fig. 6. The node voltages show an obvious discrepancy between the two layout topologies. When an incident particle strikes the PMOS transistor, the voltages of node *mn2* and *mn4* in the common layout topology rise immediately. It results in the perturbation of the other node voltages (for example node *mn3*), and finally induces an upset in the DICE flip-flop.

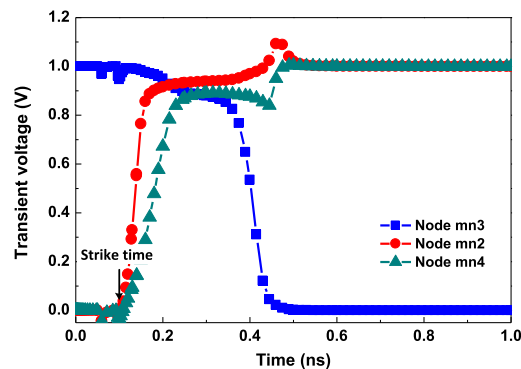


Fig. 5. The simulated transient voltages after particle strikes in the common layout topology.

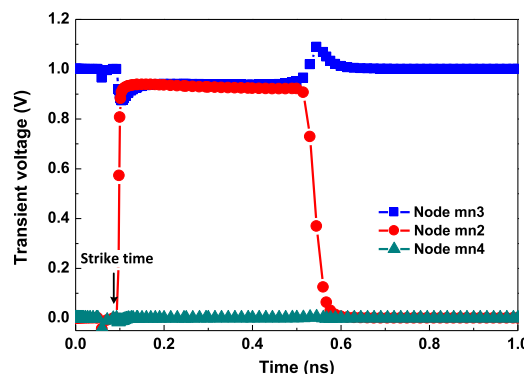


Fig. 6. The simulated transient voltages after particle strikes in the separation layout topology.

For the separation layout topology, although the voltage of node *mn2* also rises immediately, the voltage of node *mn4* is still low. Only one node upset does not influence the other node voltages. Therefore, the voltage of the node *mn2* comes back to the initial value after hundreds picoseconds and an upset does not occur. Similar simulation results are observed when the incident location is set to the sensitive NMOS transistors.

The transient current and the collected charge at the sensitive node *mn4* are shown in Fig. 7. An obvious transient current pulse is observed in the common layout topology while a slight transient current pulse is observed in the separation layout topology. The collected charge of the sensitive node *mn4* in the common layout topology shows about two orders of magnitude higher than that in the separation layout topology. Simulation results indicate the adjacent transistors can significantly affect the transient current and collected charge of the sensitive node pairs. Because they have a higher charge collection capability in the separation layout topology, the separation layout topology can reduce the SEU sensitivity of the DICE flip-flop.

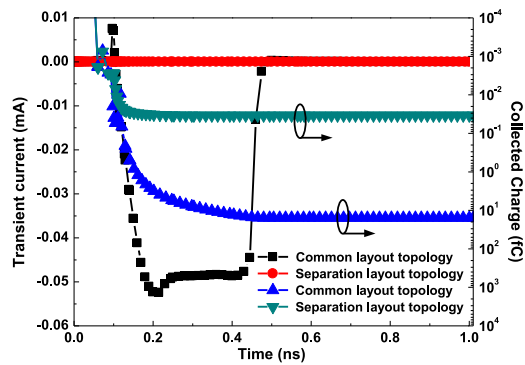


Fig. 7. The transient currents and collected charge correspond to the node *mn4* in two layout topologies.

4 Experiment setup and results

4.1 Test chip design and experiment setup

A test chip was designed and fabricated based on the commercial 65 nm CMOS technology. It was constructed by the conventional DICE flip-flop with two different layout topologies. The schematic of the test circuit and the layout topology is shown in Fig. 8. The test chip consisted of two shift registers. Each shift register consisted of 2048 stages DICE flip-flops with the data and the clock tree. Once one stage of the shift register chain was corrupted by heavy ion or pulsed laser, the subsequent ones in the chain propagated the upset value until it was read out from the output pin.

Heavy ion experiment was conducted at the HI-13 Tandem Accelerator in China Institute of Atomic Energy. The characteristics of the heavy ions used in the experiment are listed in Table I. The incident ion dose rate was 1×10^4 ions/cm²·s and the fluence in each incident ion was 1×10^7 ions/cm².

Table I. Heavy ions used in the experiment

Ion	Energy at the silicon Surface (MeV)	Effective LET (MeV·cm ² /mg)	Range (μm)
Si	143	9.01	54.5
Ci	165	15.1	47.4
Ti	169	21.8	34.7
Fe	170	27.9	30.0
Ge	212	37.2	30.8

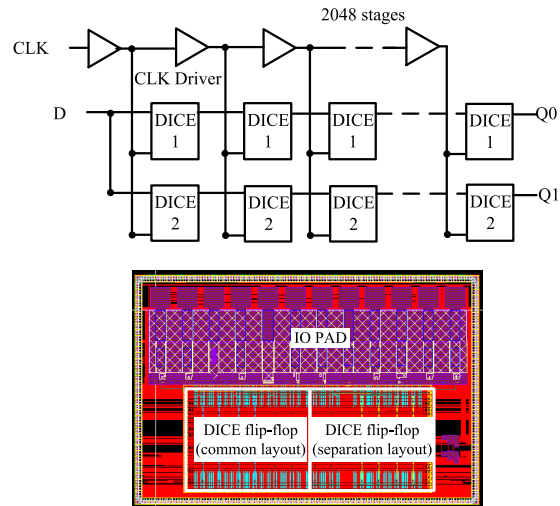


Fig. 8. The schematic of the test circuit and the layout topology.

SEUs were measured with the normal supply voltage and the room temperature. The dynamic test mode was used to measure the SEU sensitivity of the D and DICE flip-flops. The test circuit was irradiated with solid 0 data or solid 1 data. Since the input data were fixed, soft errors owing to the clock tree were avoided. The upset in the clock tree may cause the data to shift forward without any error. Therefore, only flip-flop induced upset can cause SEU.

4.2 Experiment results

The measured SEU cross sections are shown in Fig. 9. The SEU cross section is defined as the total number of SEUs captured in heavy ion experiment divided by the fluence (1×10^7 ions/cm²) and the stages of the shift register chain (2048). The Y error bars are represented as the 95% confidence intervals.

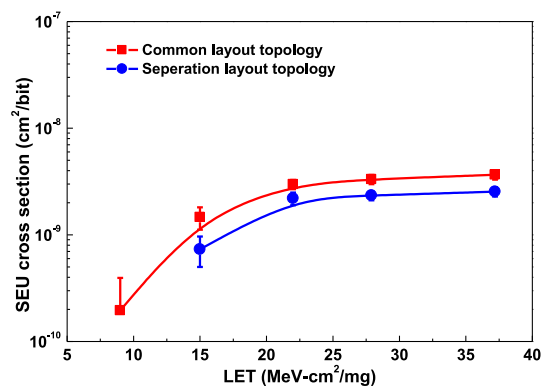


Fig. 9. The measured SEU cross section with two layout topologies.

Based on the measurement results, the DICE flip-flop shows the different SEU sensitivity with two layout topologies. For the common layout topology, the DICE flip-flop upsets its storage value when the LET is only 9 MeV·cm²/mg. For the separation layout topology, the DICE flip-flop does not upset at 9 MeV·cm²/mg as has been shown by the TCAD simulation such that its charge collection is two

orders of magnitudes less than the common structure. The SEU cross sections with two layout topologies also show obvious discrepancies. The SEU cross sections with the separation layout topology has about 29% decrease compared with that with the common layout topology. Measurement results confirm the adjacent transistor can significantly affect the SEU sensitivity. The adjacent transistors with the separation layout topology can reduce both the SEU threshold and the SEU cross sections of the DICE flip-flop.

5 Conclusion

Technology scaling has increased the SEU sensitivity of the DICE flip-flop. Because of charge sharing, the adjacent transistors among the sensitive transistors also collect charge simultaneously, which may significantly affect the SEU sensitivity.

This paper has studied the impact of adjacent transistors on the SEU sensitivity of the DICE flip-flop. Two different layout topologies are considered to investigate the effect mechanisms of the adjacent transistors. Simulation and experiment results indicate the adjacent transistors significantly affect the transient current and collected charge of the sensitive node pairs. The adjacent transistors with the separation layout topology can reduce both the SEU threshold and the SEU cross sections of the DICE flip-flop.

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