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Study of closed-loop high-resolution sigma-delta for a MEMS accelerometer

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Abstract: In this paper, a high-resolution Sigma-Delta (ΣΔ) modulator in a standard 0.5 μm CMOS technology for a MEMS accelerometer is presented. The digital output is attained by the interface circuit based on a low-noise front-end charge-amplifier and a back-end forth-order Sigma-Delta modulator. The low-noise front-end detection circuit is proposed with correlated double sampling (CDS) technique to eliminate the $1/f$ noise and offset of operational amplifier. The capacitance compensation array is used for rejecting the sensor element mechanical offset. The lead compensator circuit is to ensure the stability of the high-order closed-loop system. The interface is fabricated in a standard 0.5 μm CMOS process and the active circuit area is about 8 mm^2. The MEMS accelerometer system consumes 25 mW from a single 7 V supply at a sampling frequency of 250 kHz. The ΣΔ modulator can achieve an effective number of bits 20.30 bits and an average noise floor in low-frequency range of 140 dB.

Keywords: MEMS accelerometer, interface circuit, capacitance compensation array, Sigma-Delta

Classification: Integrated circuits

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1 Introduction

Recently, high-precision capacitive accelerometers are widely applied in inertial navigation and guidance, aerospace, military and automotive market [1]. Many high-performance micro-accelerometers are based on the electromechanical force-balancing sigma-delta loop. In order to improve the linearity, dynamic range (DR) and bandwidth, the capacitive accelerometers work in the case of closed-loop [2, 3]. ΣΔ modulators are widely used for low-frequency analog-to-digital conversion in applications such as speech processing where the oversampling ratio can be considerably high and the noise rejection is very efficient [4, 5]. In micromechanical accelerometers, since the mechanical bandwidth is usually quite small (<2 kHz), ΣΔ conversion can effectively reduce noise and improve overall performance. Because MEMS accelerometers have good compatibility with CMOS process, the research on ΣΔ interface circuit of micro-machined accelerometers have significant theoretical value and applied benefit [6, 7].

In this work, we propose a 4th-order low-noise closed-loop ΣΔ modulator interface circuit based on MEMS accelerometers. The high-resolution sensor element has a low mechanical noise of smaller than 1 μg/Hz$^{1/2}$ from Colibrys SF1500. The capacitance compensation array is used for rejecting the sensor

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element mechanical offset. The lead compensator circuit is to ensure the stability of the high-order closed-loop system. The correlated double sampling (CDS) is used for eliminating the $1/f$ noise and offset of operational amplifier in the front-end detection circuit. Tested results and discussions are shown.

2 Proposed system architecture

The proposed closed-loop accelerometer system architecture is shown in Fig. 1. The closed-loop accelerometer system includes a capacitor compensation array, a switched-capacitor charge sensing amplifier (CSA), a CDS, a lead compensator, and a 4th-order ΣΔ modulator. The closed-loop accelerometer structure is achieved by time shared multiplexing electrostatic feedback micro-accelerometer principle without use of electrostatic electrode performer. The electrostatic feedback and charge sensitization are accomplished in different phases of one cycle, which greatly eliminates feedthrough between feedback signal and capacity sensitization signal. The SC CSA is interfaced with the top and bottom electrodes, which is used to convert the charge signal of the balanced bridge-structure to an amplified voltage signal. The CDS circuit is employed to eliminate the $1/f$ noise and offset of operational amplifier [8]. The compensation is required for the stability of high-order system in this work and the lead compensator provides electrical damping for the high-Q sensor element [9]. The back-end blocks consist of a 4th-order ΣΔ modulator. The differential feedback voltages are fed to the top and bottom electrodes. It generates electrostatic force in opposite directions based upon its input bitstream.

2.1 Capacitor compensation array circuit

Ideally, the size of a pair of differential capacitors between the beams and the fixed electrode is equal. However, in the actual process, because of errors in the processing technology, it can result in deviations between active beams and a central location, and thus the output offset is generated in the circuit. The compensation capacitor can make up for disadvantages of the compensation in the circuit. The capacitor array consists of a series of rhythmic changes in capacitance between the drive signal and the detection signal designed to achieve compensation in a certain variable step. The design of the capacitor array includes 500 fF, 250 fF, 125 fF, 62.5 fF, 31.25 fF and 15.625 fF. In each sub-unit, the unit capacitor is connected to the active beam and the fixed electrode through the switch. The size of different capacitors can be controlled by each switch because the compensation capacitor and sensitivity sensor act in parallel. The capacitance compensation array unit circuit is shown in Fig. 2. When electrode1 is high level, M1 and M2 are working and the fixed electrode is connected to *A* point. If C1_control is high level, M3, M4, M5 and M6 are working, the capacitor C1 is connected to the fixed electrode and mass block, which can implement the capacitor compensation function. If C1_control is low level, M7 and M8 are working and the upper and lower plates of capacitor C1 are both connected to GND. In the whole compensation array, the upper and lower plates can share C1, C2, C3 … and C_n capacitors, the two control signals electrod1 and electrode2 can determine *A* point is connected to the upper plate or the lower plate.

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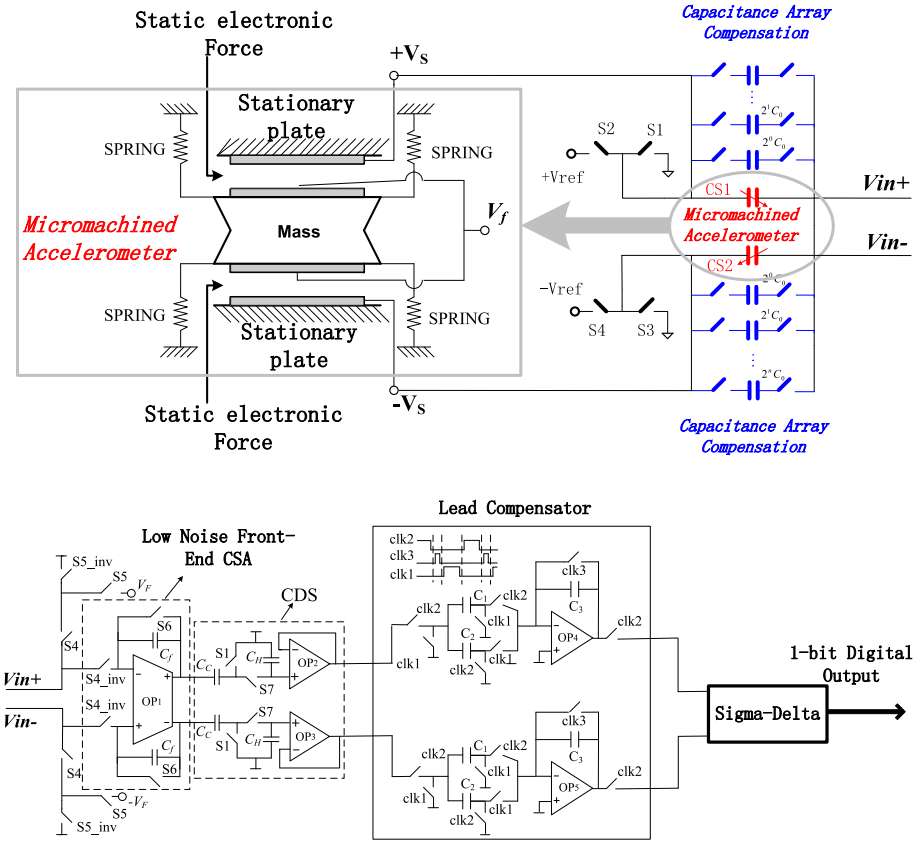

Fig. 1. The closed-loop accelerometer system architecture

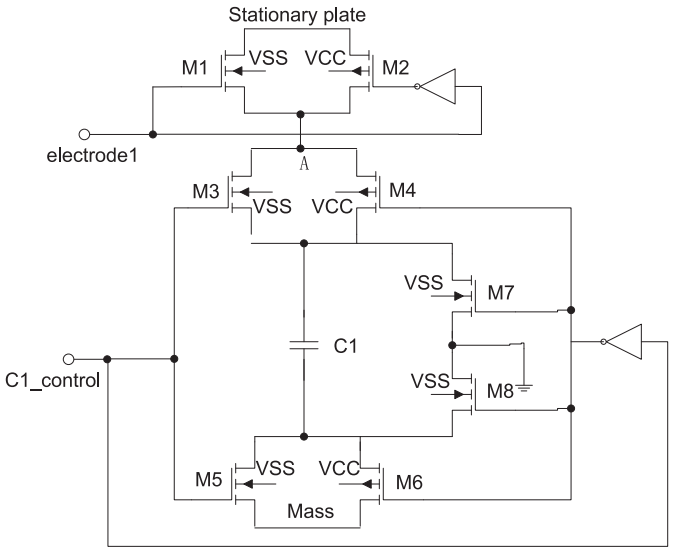

Fig. 2. The capacitance compensation array unit circuit

2.2 Sigma-Delta modulator

Fig. 3 shows a fully differential 4th-order forward ΣΔ modulator and sequence diagram circuit. The noise shaping module of double-ended fully differential structure consists of four in-phase integrators. The 1-bit quantizer is achieved by the dynamic comparator. The input signal of the modulator is as the input signal of the integrator and input signal of forward summation network. The output of the comparator is as a control signal to control feedback reference voltage V_{neg} and V_{pos} in the first stage integrator. Wherein ck_1 and ck_2 are the two-phase non-

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overlapping clock, ck_1 is active-high, ck_2 is active-low. The shutdown time of ck_{1d} is later than ck_1, The shutdown time of ck_{2d} is later than ck_2, it can effectively suppress the influence of charge injection and clock-feedthrough in the switched-capacitor circuit. When $ck_1 = 1$, $ck_2 = 0$, the modulator begins to sample the signal, the signal is quantized by the one-bit quantizer. When $ck_1 = 0$, $ck_2 = 1$, the modulator begins to be integral to the signal, the quantizer output feeds back to the first stage integrator input.

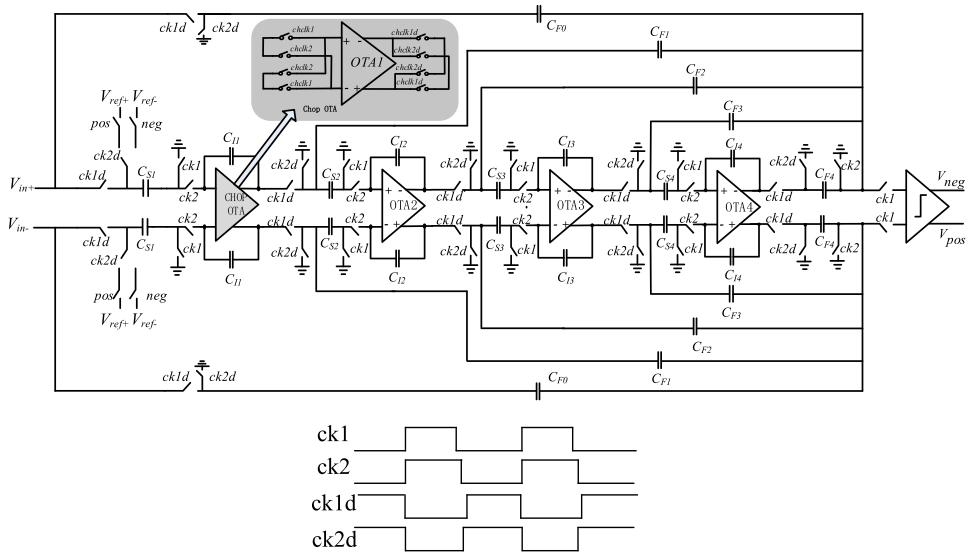

Fig. 3. The fully differential 4th-order ΣΔ modulator and sequence diagram circuit

3 Experimental results

The interface circuit was fabricated in a standard 0.5 µm CMOS process, and the photograph of the accelerometer interface chip is shown in Fig. 4 with an active area of 8 mm^2. The 7 V power supply is supported by the Agilent E3631 and the power dissipation of the sensor is 25 mW with a sampling frequency of 250 kHz. The digital output bitstream is captured by the Agilent Logic Analyzer 16804A and processed by a standard Matlab program. The 65536-point FFT plot result of the high-order high-Q accelerometer sensor is presented in Fig. 5(a) which indicates that average noise floor in low-frequency range is around 140 dB. The input range of the sensor is limited to ±1.2 g by power supply as shown in Fig. 5(b) which shows the relation between the input acceleration and sensor output and indicates a sensitivity of about 0.5 V/g. The DC non-linearity of the sensor is 0.15%. Additionally, the non-linearity of the front-end is dominated by the two unity-gain amplifiers, which is due to the influence of the common-mode. The sensor system achieves a resolution of 0.5 µg/$Hz^{1/2}$ over a 300 Hz bandwidth, which is limited by the fundamental frequency of the sensor element. We compare the performance of this work with the previously reported one based on a representative figure of merit ($FOM = P \times a_n \times BW^{1/2}/BW$), where P is the power dissipation, a_n is the noise floor and BW is the signal bandwidth. It can be seen that the accelerometer in this work achieve a better performance. This work is advantageous in the noise floor compared with [10, 12, 13] and a better FOM as shown in Table I.

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Table I. Performance summary and comparison

Parameters	[10]	[11]	[12]	[13]	This work
Bandwidth (Hz)	200	300	500	300	300
Noise floor (μg/Hz$^{1/2}$)	2	0.3	4	1.15	0.5
Power (mW)	3.6	85.8	4.5	12	25
Process (μm)	0.35	0.7	0.5	0.6	0.5
FOM	0.51	1.49	0.80	0.80	0.72

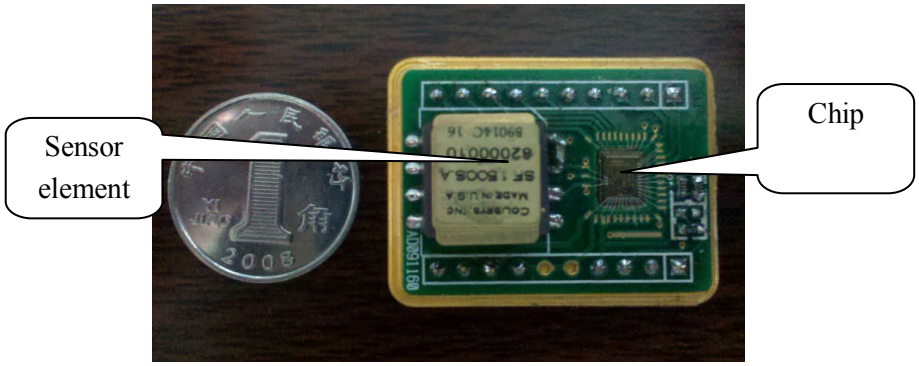
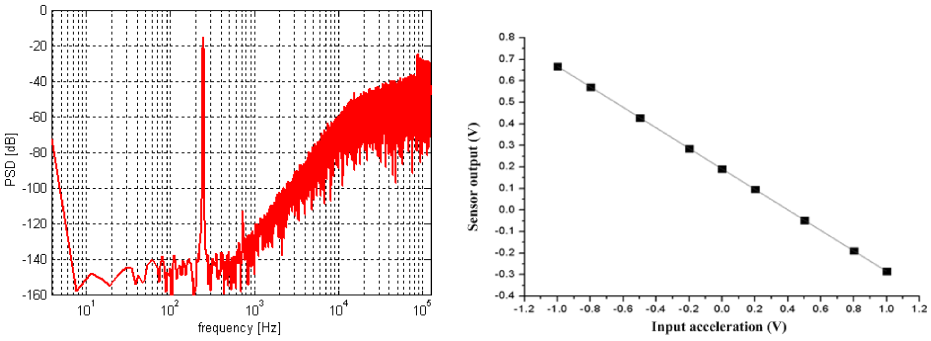


Fig. 4. The forth-order Sigma-Delta modulator circuit



(a) (b)

Fig. 5. (a) The output spectrum of Sigma-Delta modulator, (b) The non-linearity test

4 Conclusions

A high-order closed-loop Sigma-Delta modulator for a MEMS accelerometer is proposed in this work. The capacitance compensation array is used for rejecting the sensor element mechanical offset. The CDS circuit is employed to eliminate the $1/f$ noise and offset of operational amplifier. The lead compensation is required for the stability of high-order system. The dynamic range (DR) of the modulator can reach 125 dB. The average noise floor in low-frequency range can reach around 140 dB.

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