Multilevel pre-equalization using an analog FIR filter with multiple binary delay lines for 20-Gb/s 4-PAM multimode fiber transmission

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Abstract: We propose a novel multilevel pre-equalizer using an analog FIR filter having multiple binary delay lines composed of CMOS inverters. The proposed pre-equalizer can decrease the required circuit scale of conventional analog FIR filters based on binary delay lines. The required number of multiplier circuits was halved by the proposed design scheme in the case of four-level pulse amplitude modulation (4-PAM). The performance was investigated using numerical simulation of a 20-Gb/s 4-PAM multimode fiber (MMF) transmission system. The proposed pre-equalizer successfully compensated the 4-PAM signals, improving the error vector magnitude (EVM) from 40% to 21%.

Keywords: equalization, pre-distortion, FIR filter, 4-PAM, multi-mode fiber, CMOS circuit

Classification: Optical systems

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1 Introduction

Higher-speed and larger-capacity data transmission is required in fiber optic communication links to accommodate rapidly increasing data traffic. High-speed network links constructed using 100-G and 400-G Ethernet have been reported [1]. Multilevel modulation is one key technology to increase the transmission capacity. In particular, four-level pulse amplitude modulation (4-PAM) with multimode fibers (MMFs) is one promising technology for achieving cost-effective transmission systems. However, inter-symbol interference (ISI) caused by differential modal delay (DMD) limits the transmission speed of MMFs. Various schemes have been investigated to compensate for DMD. For example, electrical-domain compensation using multipurpose digital-signal processors (DSPs) has been reported; in this approach digital filters, such as finite impulse response (FIR) filters, are calculated by the DSPs [2, 3]. On the other hand, analog FIR filters based on analog electronic circuit technology are also attractive for achieving cost-effectiveness and low power consumption [4, 5, 6, 7, 8]. We have investigated analog FIR filters using binary delay-line components based on complementary metal-oxide-semiconductor (CMOS) inverters which can realize smaller integrated-circuit (IC) chip size [9]. The analog FIR filters can be used for pre-equalization for binary data formats, such as binary phase-shift keying (BPSK). Additionally, we have proposed a multilevel pre-equalizer composed of multiple binary analog FIR filters [10]. However, the proposed multilevel pre-equalizer has a drawback that the required circuit scale increases in proportion to the bit-scale of the multilevel signals. For example, to pre-equalize 4-level (2-bit/Symbol) and 8-level (3-bit/Symbol) signals, the multilevel pre-equalizer requires 2-times and 3-times larger circuit scales, respectively [10]. In this paper, we propose a novel multilevel pre-equalizer that can decrease the required circuit scale. The pre-equalizer employs multiple binary delay lines which can realize multilevel modulation format in spite of binary delay-lines.

The delay lines can be implemented with simple CMOS inverters. The performance was investigated by numerical simulations of 28 nm fully depleted silicon on insulator (FD-SOI) based CMOS circuits for 20-Gb/s 4-PAM MMF transmission.

2 Construction of proposed multilevel pre-equalizer

Fig. 1(a) shows a conventional multilevel pre-equalizer using multiple binary analog FIR filters for four-level (2 bit/Symbol) signals composed of $X_1(n)$ and $X_0(n)$ [10]. The n-th four-level signal value $X(n)$ is given by

$$X(n) = 2^1 \times X_1(n) + 2^0 \times X_0(n), \tag{1}$$

where $X_1(n)$ and $X_0(n)$ are the most-significant bit (MSB) and least-significant bit (LSB), respectively. Using Eq. (1), the output value of the FIR filter $Y(n)$ can be expressed as
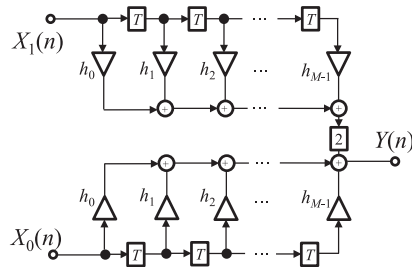
$$
\begin{aligned}
Y(n) &= \sum_{i=0}^{M-1} h_i X(n-i) \\
&= \sum_{i=0}^{M-1} h_i \{2X_1(n-i) + X_0(n-i)\},
\end{aligned} \tag{2}
$$

where h_i and M are the i-th tap-coefficient and the number of taps, respectively. Equation (2) is also expressed as
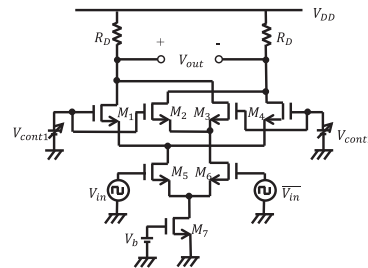
$$Y(n) = 2\sum_{i=0}^{M-1} h_i X_1(n-i) + \sum_{i=0}^{M-1} h_i X_0(n-i). \tag{3}$$

The two terms on the right side of Eq. (3) are represented by two FIR filters in Fig. 1(a). In Fig. 1(a), one multilevel pre-equalizer consists of two parallel binary FIR filters and a 2/1-weighted adder. The two binary FIR filters have the same tap-coefficients, h_i, and tapped delay time, T. Binary input signals $X_1(n)$ and $X_0(n)$ are pre-equalized by the two FIR filters independently, and are added after 2/1-weighting. In our proposed analog FIR filter, the multipliers are implemented with Gilbert cells, as shown in Fig. 1(b) and the binary delay lines are implemented with CMOS inverters, as shown in Fig. 1(c) [9]. Here, it should be noted that adders can be easily realized using resisters in current summing circuits. However, the conventional multilevel pre-equalizer has a drawback that the required circuit scale increases in proportion to the bit-scale of the multilevel signal. For example, to pre-equalize 4-level (2-bit/Symbol) and 8-level (3-bit/Symbol) signals, the multilevel pre-equalizer requires 2-times and 3-times larger circuit scales, respectively. Fig. 1(d) shows the proposed multilevel pre-equalizer, which can decrease the required circuit scale. The block diagram in Fig. 1(d) represents Eq. (2) directly. The proposed circuit employs multiple binary delay lines to realize multilevel signals. The binary signals $X_1(n)$ and $X_0(n)$ are delayed by using different delay lines. Delayed binary signals $X_1(n)$ and $X_0(n)$ are added after 2/1-weighting and are multiplied by the tap-coefficient h_i. Here, it should be noted again that the 2/1-weighted adder can be easily realized using resisters in current summing circuits as described above. Therefore, the 2/1-weighted adders do not increase the circuit scale. The required number of multiplier circuits is halved by the
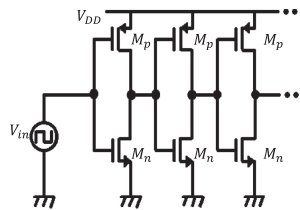
proposed design scheme in this case of four-level (2 bit/Symbol) signals as shown in Fig. 1(d). In the case of 8-level (3 bit/Symbol) signals, the required number of multiplier circuits becomes one-third in comparison with the conventional circuit. The multiplier circuit is the largest component in the pre-equalizer as shown in Fig. 1(b). Therefore, the proposed pre-equalizer can dramatically decrease the required circuit scale.
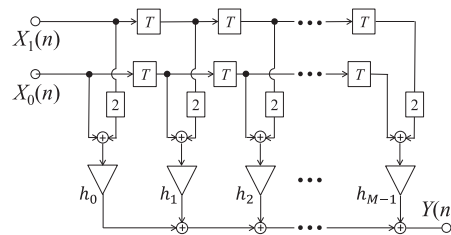

(a) Conventional four-level pre-equalizer using binary analog FIR filters.

(b) Gilbert cell.

(c) CMOS inverters.

(d) Proposed four-level pre-equalizer.

Fig. 1. Four-level pre-equalizers composed of Gilbert cells and CMOS inverters.

3 System setup

Fig. 2 schematically shows the system setup used in our numerical simulation for 20-Gb/s 4-PAM transmission over 500 m of MMF. A DFB laser with a wavelength of 1550 nm was directly modulated by a four-level signal pre-equalized using the proposed four-level analog FIR filter calculated by a SPICE circuit simulator, resulting in a pre-equalized optical 4-PAM signal. The pre-equalizer had six taps

whose tap coefficients had been determined by a least-mean-square (LMS) algorithm. The four-level signal was composed of 10-Gsymbol/s PRBS 2^9-1 binary data. The modulated optical signal was transmitted by a 500 m MMF with a 50 μm parabolic-index core. A mode scrambler was used at the input of the MMF to evenly excite higher-order modes. The received optical power was adjusted using an attenuator (ATT) and was directly detected by a photodetector (PD).
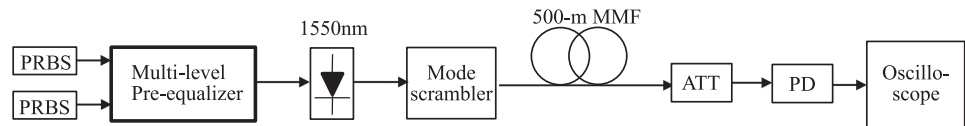
Fig. 2. System setup for 20-Gb/s 4-PAM transmission over 500 m MMF.

4 Results and discussion

Figs. 3(a), (b), and (c) show eye diagrams of the transmitted 4-PAM signals. Fig. 3(a) shows the eye diagram for the case where the pre-equalization was not employed. The waveform was completely distorted by DMD in the MMF. Fig. 3(b) shows the eye diagram for the case where pre-equalization was employed by using the proposed multilevel pre-equalizer shown in Fig. 1(d). Clear eye openings were achieved by the pre-equalization. For comparison, Fig. 3(c) shows the eye diagram for the case where pre-equalization was employed by using the conventional multilevel pre-equalizer shown in Fig. 1(a). Comparing the two eye diagrams shown in Fig. 3(b) and (c), we can observe some degradation of the eye opening when employing the proposed pre-equalizer. The degradation was caused by imbalances of the analog multiplier and adder circuits. Calculated EVM values versus optical received power are shown in Fig. 4. In the case without the pre-equalization, the EVM did not decrease to less than 40%, even when we increased the optical received power. In the case using the proposed pre-equalization, however, the EVM was improved to 21%. In the case of the conventional pre-equalizer, EVM values of 9% were achieved. The results clearly showed the effectiveness of our proposed multilevel pre-equalizer. To improve the performance, however, we have to optimize the circuit parameters of the analog FIR filter to resolve the imbalances of the circuits.
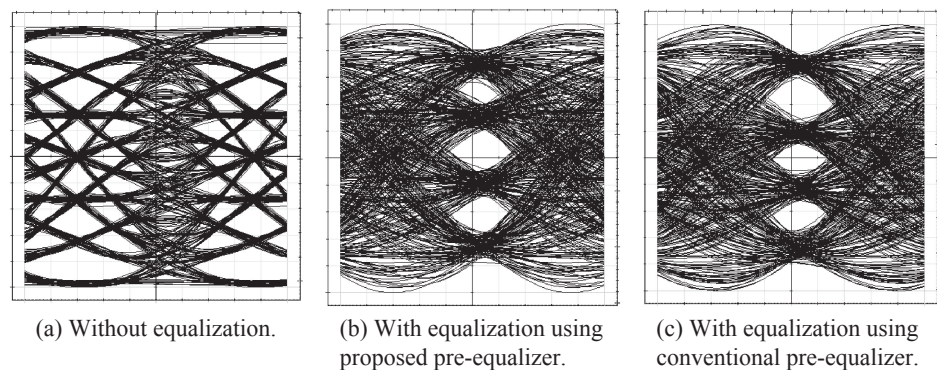
(a) Without equalization.

(b) With equalization using proposed pre-equalizer.

(c) With equalization using conventional pre-equalizer.

Fig. 3. Eye diagrams of the transmitted 4-PAM signals.
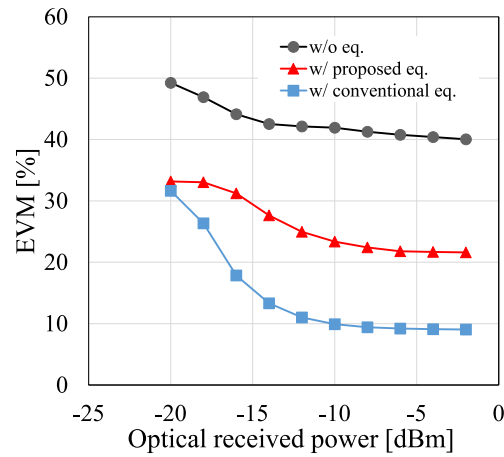
Fig. 4. EVM characteristics of the transmitted 4-PAM signals.

5 Conclusion

We proposed a novel multilevel pre-equalizer using an analog FIR filter with multiple binary delay lines. The proposed design scheme can decrease the required circuit scale of conventional analog FIR filters. The equalization technology described here should encourage the adoption of analog FIR filters in future cost-effective, low-power, high-speed optical data links.