LETTER

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Robust digital deadbeat control design technique for 3 phase VSI with disturbance observer

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Abstract: A novel technique for an optimized deadbeat controller, having higher convergence rate for certain disturbances and capability to maintain the system stability, rapid response and extinction of errors, is presented in this paper. This control law is stimulated with integral control for tracking the reference signals. Moreover, the deadbeat controller is proposed with a state estimator and a disturbance observer for estimating the next sampling interval and to maintain the robustness along with rapid dynamic as well as static response in case of load uncertainty or unpredicted disturbance. The proposed technique is found relatively more effective than the conventional controller and previously designed deadbeat controllers due to its properly designed parameters, as discussed through simulation and by loop experiments in real time hardware assessments.

Keywords: 3-Phase VSI, deadbeat controller, SVPWM, stand-alone mode

Classification: Power devices and circuits

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1 Introduction

The increasing demand for electricity claims innovation in technology for electricity and power electronics equipment. In order to meet this challenge, several control techniques, having various Pulse Width Modulation (PWM) schemes are introduced for stable output, prompt response and reduction of stable errors. However, Voltage Source Inverter (VSI), also known as Voltage Source Converter (VSC), is gaining much interest with an integrated output LC filter, in its control strategy, for being extensively used in the industrial applications as well as for the domestic purposes. Several techniques are mentioned by various authors like proportional resonant controller [1], feedback linearization technique [2, 3], LCL filter with active damping algorithm [4] are extensively applied methods nowadays. However, these control schemes are stated vulnerable due to variations in parameters. VSIs have several applications in power electronics motor drives [5], distributed generation systems [6], uninterruptable power supply system [2, 7] and

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active power filters [8]. Several deadbeat controllers with current control techniques and LC/LCL filters are implemented on VSIs, UPSs and active filters are presented in [9, 10, 11, 12, 13]. Most of the techniques are either on microprocessors, instead of DSP, or outdated inverter technologies having susceptibility due to parameters variation or complicated implementation technique. In [14], the disturbance observer is used with a deadbeat controller for appropriate response and robust controller performance. However, suitable PWM technique for multiloop control is not comprehensively described and PWM pattern in case of load uncertainties is not elaborated in detail. Moreover, experiments were performed through a single phase 2 kVA laboratory prototype. In [15], a detailed actively damped LC filter model with a virtual damper is designed and implemented with deadbeat controller for robust control of parameters mismatching. Moreover, a comparison with conventional control technique is also described. However, implementation of deadbeat controller in this technique is much complicated and its design is more complex and it is unsuitable for economical implementation. However, energy losses are relatively higher in that technique. In [16], high fluctuation is observed in parameters of the deadbeat controllers as well as load uncertainties and steady state errors also exists.

In the proposed technique, an optimum deadbeat controller, is designed for norm-bounded uncertainties in the system. The criteria of system designing are well organized with a certain set of parameters through mathematical modeling. Intelligent tuning of these parameters can lead to optimal control of VSI and improved performance for given disturbances. Overall control model is designed orderly and systematically for making it user friendly. In stabilizing control law, integral controller is integrated for purpose of reference tracking. Moreover, derived Eigen values and poles placement on the origin makes the system more robust having less THD value as well as it shows the prompt response to a dynamic load or voltage fluctuations. The system is designed in simplified manners and SVPWM technique is used for smooth PWM pattern and less harmonics. Unlike other controllers, parameters are not sensitive to disturbance and remain stabilized and show robust dynamic, transient and step response in case of unpredicted disturbance. Moreover, controller was tested through simulation and real time hardware tests and the results depict that response time is not increased instead of dead-time and fluctuations in dc-link voltage. Furthermore, no parameter mismatching occurred and state variable errors were reduced to zero successfully as verified through simulation and experimental results.

The rest of the paper is organized as follows: Modeling diagram and its description is mentioned in Sec. 2. In Sec. 3, mathematical modeling and details regarding proposed control method are presented. Current and Voltage loop modeling is described in Sec. 4. Disturbance observer is mentioned in Sec. 5. Conventional PI controller is illustrated in Sec. 6. However, analysis and discussion of simulation and real time hardware experimental results are demonstrated in Sec. 7 and 8 respectively, whereas the conclusion part is declared in Sec. 9.

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2 System modeling and controller design

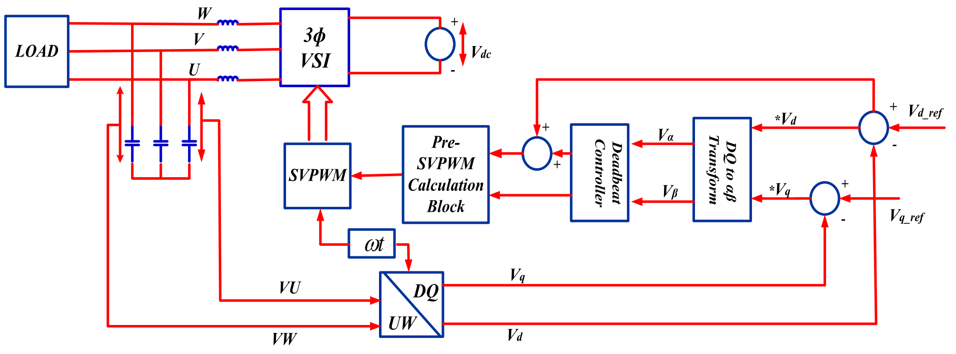

Fig. 1. Three Phase VSI control block configuration diagram.

In Fig. 1, a three-phase inverter, having six IGBT switches is considered. An LC filter is integrated at its output side for smooth and stable output. In case of elongated time interval, a closed loop system is implemented with a suitable control technique for prompt response and optimum stability. In the proposed method, a modified deadbeat controller is used. Park's transformation technique is applied for reference frame transformation. All three reference frames, i.e. *uvw*, $\alpha\beta$ and *dq*, are used for the coordinate's transformation. Space vector pulse width modulation, SVPWM technique is used for meticulous analysis for results. In this case, a three-phase VSI is considered in stand-alone mode. Reference voltage, V_{ref} is fed in synchronized *dq* reference frame for the abrupt response and comprehensive analysis. However, V_q is fed as zero for smooth tracking purpose. V_{ref} is accurately tracked in case of *dq* reference frame as well as in the three phase system as depicted in the results. However, Pre-SVPWM block represents essential mathematical functions for suitable pulse width modulation. Whereas, ωt represents the angle required for Park's transformation as well as for SVPWM.

3 Mathematical system modeling

A system is usually designed for fulfilling the structural requirements and to get the desired results. For getting the desired response several controllers are designed and various techniques have been planned. One of the most enhanced techniques designed till date is a deadbeat controller. Model of the project is fundamentally observed in this technique; so, if there would be any differences in the model, the results would be affected. Therefore, the modeling of the project is especially taken under consideration in this case. The deadbeat control structure analyzes the system to fetch its output in steady state in the minimum number of time steps.

$$\begin{bmatrix} I_L \\ V_c \end{bmatrix} = X = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} U_r. \tag{1a}$$

$$Y = CX = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix}, \tag{1b}$$

where, I_L and V_c are the current across inductor and the voltage across capacitor. Eq. (1) is extracted from inner current loop and outer voltage loop in state space

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model after mathematical modeling of the inverter with LC filter. U_r is rated voltage referred to the system i.e. output voltage. However, R, L and C are resistance, inductance and capacitance of the system respectively. For system discretization in state space form, it can be defined as following:

$$G(s) = y = C(SI - A)^{-1}BU. \tag{2}$$

Transforming Eq. (2) into system function:

$$G(s) = X = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} s & \frac{1}{L} \\ -\frac{1}{C} & s + \frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}. \tag{3}$$

In case of linear time-invariant system, the system has an inherited characteristic of taking itself to equilibrium. In order to convert this model into discrete time domain, it should be converted into z-domain. Several techniques are described for Z-transformation. Bilinear method is implemented for getting this model simplified. As a deadbeat controller depicts the expected value of a new upcoming sample $U_o(k+1)$, for which an input is given to the system and desired output can be taken. Therefore, for a new sample $(k+1)$, describing $k = T$ *in* discrete time domain, a general system equation is obtained as following:

$$G(s)\begin{cases} = 4\left(\frac{LC}{T_s^2} - \frac{2L}{RT_s^2} + 1\right)U_o(k-1) + \left(2 - \frac{8LC}{T_s^2}\right)U_o(k) + \left(4\frac{LC}{T_s^2} + \frac{2L}{RT_s} + 1\right)U_o ref \\ = U_r ref(k-2) + 2U_r ref(k-2) + 2U_r ref(k-1) + U_r ref(k) \end{cases} \tag{4}$$

Where T_s represents switching time, U_o is output voltage for sampling time k, L is inductance and C is capacitance of the LC filter. The values of capacitor and inductor in LC filter as well as various other parameters required for Simulation as well as experimental verification of mathematical model are described in Table I.

Table I. System constraints

Parameters	Symbol	Value
Grid Frequency	f	50 Hz.
DC voltage	V_{dc}	440 V
Filter capacitance	C_F	15 µF
Filter inductance	L_F	2.7 mH
Nominal load resistance	R_N	40 Ω
Reference output voltage	$[V_d\ V_q]$	[50 0] V
Base voltage (phase-neutral)	V_B	220 V
Switching frequency	f_s	12 kHz.

4 Current and voltage loops modeling

System is converted in $\alpha\beta$ coordinates, analyzing it, solving it further, equations of inner current loop and outer voltage loop in open and closed loop conditions respectively, are described in Eqs. (5) and (6) as follows:

$$G(z) = z\left[\frac{T_c K_c}{L(z-1)}\right] \text{ and } G(z) = \left[\frac{T_c K_c}{K_c T_c + L(z-1)}\right] \tag{5}$$

$$G(z) = z\left[\frac{1 - e^{-Ts}}{s}\frac{K_v}{sC}\right] \text{ and } G(z) = \left[\frac{T_v K_s}{K_s T_v + L(z-1)}\right] \tag{6}$$

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From Eqs. (5) and (6), both current and voltage controllers for inner and outer loop are further checked for bode plot and root locus response. K_c and K_v represents gains for current and voltage loop while T_c and T_v are the time period for current and voltage loop, taken as 50 µs and 100 µs respectively.

5 Disturbance observer

A disturbance observer was designed for predicted control and to remove errors for next sampling time. Its equation modeling is done with eigenvalues by considering poles at origin, converting it into state space design and solving with state transform matrix, µ, state input matrix, δ and system output matrix, ψ, are defined as follows:

$$\mu = \begin{bmatrix} 1 & -\frac{T_s}{L} \\ \frac{T_s}{C} & 1-\frac{T_s}{RC} \end{bmatrix}, \quad \delta = \begin{bmatrix} \frac{T_s}{L} \\ 0 \end{bmatrix}, \quad \text{and } \Psi = \begin{bmatrix} 0 & 1 \end{bmatrix}, \tag{7}$$

$$\hat{x}(k+1) = (\mu - HC)\hat{x}(k) + \delta u(k) + Hy(k) \tag{8.1}$$

$$\hat{y}(k+1) = \psi\hat{x}(k) \tag{8.2}$$

From Eq. (8.1) $H = [\,h_{11} \quad h_{12}\,]^T$ is the state output matrix, and further solving voltage and current loops predictive disturbance system Eqs. can be described as follows:

$$\hat{V}_c(k+1) = 0.887\hat{V}_c(k) - 0.0370\hat{i}_L(k) - 0.0370U(k) + 0.2815i_d + 0.1130V_c(k) \tag{9.1}$$

$$\hat{i}_L(k+1) = 5.223\hat{V}_c(k) - 0.0370\hat{i}_L(k) - 0.0370U(k) + 1.722i_d + 1.444V_c(k) \tag{9.2}$$

Implementing the Eq. (9) in MATLAB/Simulink, having poles on the origin and through calculation of Eigen values, results were determined. Furthermore, implementing it through DSP coding on inverter loop experiments, results were also verified as stated in Sec. 7.

6 Conventional PI controller

The conventional PI controller is designed due to its several applications in industry as well as its tuning ability. But in this case PI controller is properly designed in MATLAB/Simulink environment by using SISO tool. A suitable mathematical function for a three-phase voltage source inverter (VSI) is derived and implemented. The mathematical equation of PI controller given in Fig. 2 is given as follows:

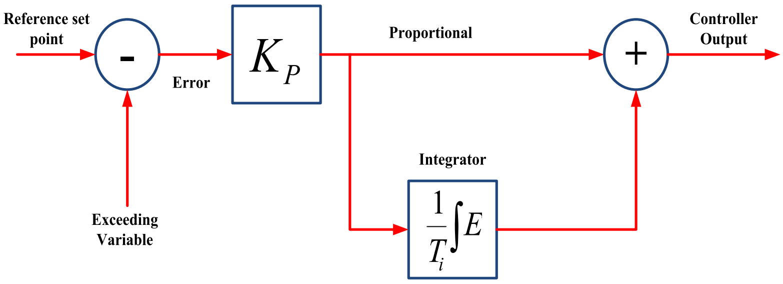

Fig. 2. Structure of conventional controller for controlling three-phase VSI.

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$$C = K_p + \frac{K_i}{s}, \quad (10)$$

where, K_p is the gain for proportional controller whereas K_i represents the integral controller. However, solving this equation mathematically with the parameters mentioned in Table I, the final equation for a three phase VSI system with a LC filter is described as follows:

$$M = \frac{V_i}{s^2LC + 1}. \quad (11)$$

Table II represents the values of K_P and K_i parameters for controlling a three phase VSI.

Table II. Parameters of conventional controller

Conventional controller parameters	Values
K_p	0.16492
K_i	0.24338

7 Simulation results

The proposed system is verified for its performance through simulation and experimental results and these results are compared with a conventional controller which is used on a high scale in industry. Although parameters of conventional controller can be tuned but in this case, they are properly designed through SISO tool in Matlab/Simulink. In order to ensure an effective comparison of both techniques, sinusoidal SVPWM technique with 12 kHz switching frequency, f_s for generating gate signals is introduced. However, the anticipated phase voltages for the converter of Fig. 1 are: $v_a = V_m \sin(\omega t)$, $v_b = V_m \sin(\omega t - 120)$ and $v_c = V_m \sin(\omega t + 120)$, where V_m is maximum amplitude of an arbitrary three phase system. In Figs. 3 and 4, both the techniques are planted in Matlab/Simulink environment through mathematical modeling for finding the response at static $V_{ref.}$ level. The results are found quite suitable and no fluctuation or effective disturbance was observed during the operation though $V_{ref.}$ was taken as 200 V in the both cases. Figs. 5 and 6 show the dynamic response of the proposed technique and conventional method. Several fluctuations in the voltage were specified to observe the stability in the parameters, and the response of the proposed controller was more accurate and less time consuming as compared to designed conventional controller. The voltage level in both cases were kept as 200 V, 150 V, 100 V, 180 V, 50 V and then 200 V respectively for observing the dynamic response. Proposed controller is found comparatively more appropriate in its response as mentioned in Fig. 7(a) and (b). The rising and falling time of active power, transition time and harmonic distortion were extensively taken under deliberation and results anticipated that the proposed controller is more accurate and errorless as compared to the conventional controller. Moreover, the proposed controller offers precise control with very low harmonic noises and distortions along with proper regulation of output active as well as reactive powers, as active power rise and fall time can be observed through dynamic response of the system, where step jump and step drop response were taken under consideration. However, the results are not reported here. The reference tracking capability in both cases is extremely accurate with

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slightly faster tracking ability of the proposed controller. However, steady state performance is optimum and accurate as it should be in a properly designed system. Although both techniques control the sinusoidal voltages as a result of which current is controlled with low distortion and low THD. However, the proposed controller is found comparatively more accurate and having better performance as compared with the conventional controller. In addition, it has the capability of predicting new sampling period having less harmonic noise, low distortion and less THD value than the conventional technique.

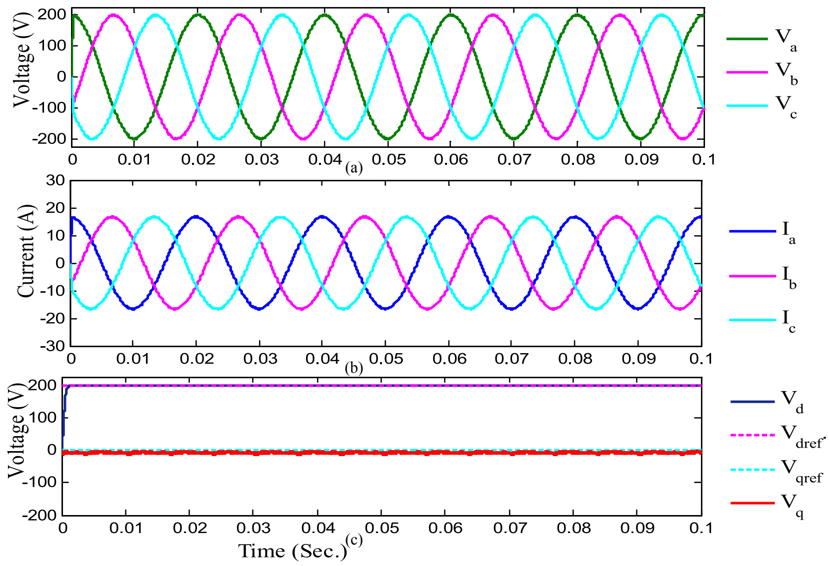

Fig. 3. Static response of conventional controller

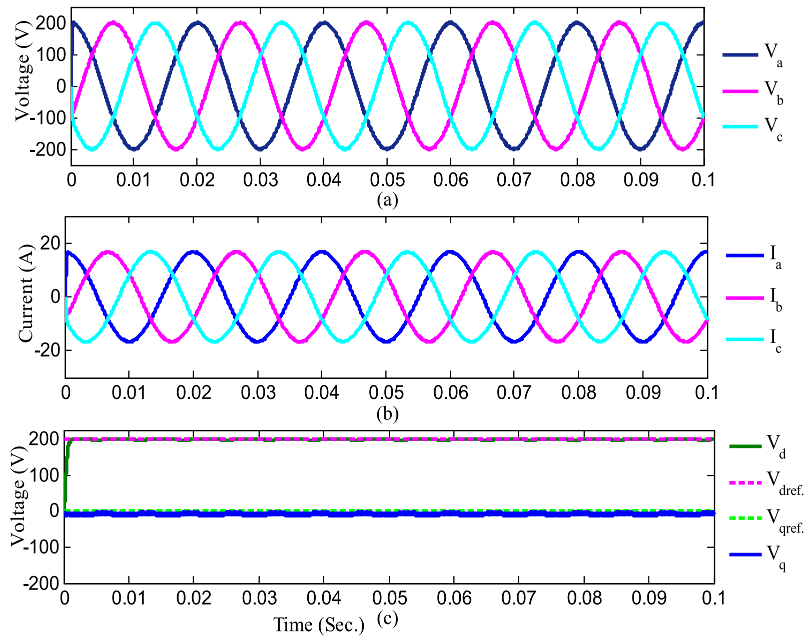

Fig. 4. Static response of proposed controller

8 Experimental results

The experimental setup of the proposed scheme is comprehensively demonstrated. It is also depicted that a 9 kW three-phase VSI including a power circuit module

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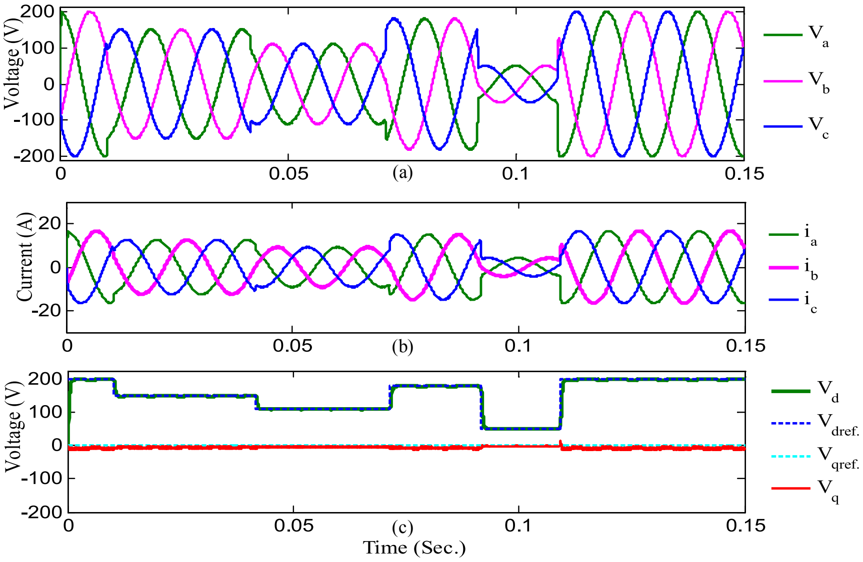

Fig. 5. Dynamic response of conventional controller.

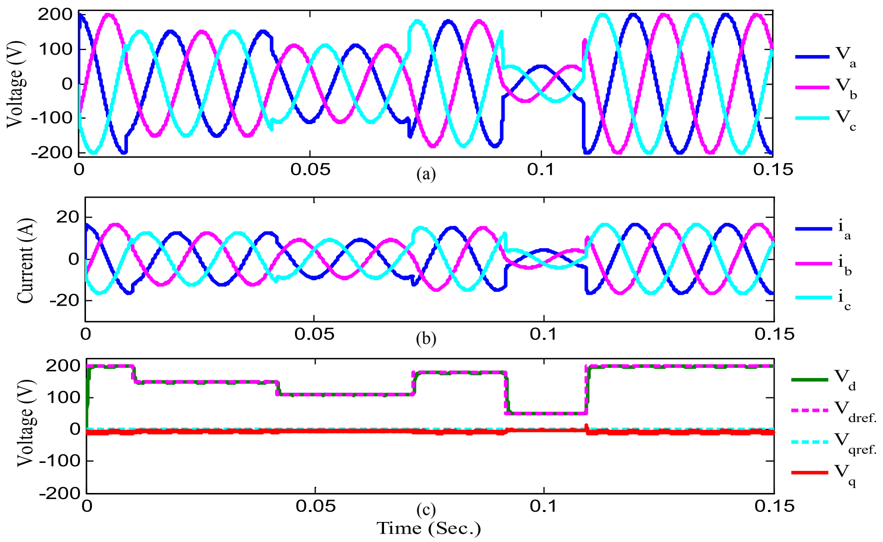

Fig. 6. Dynamic response of proposed controller

interlinked to a sensing module through interfacing module, along with drive signal generator and PWM generation system as well as resistive load is included in experimental setup. The inverter is equipped with software as well as hardware protections to protect over-voltage, over-current and high temperature. Control strategy is developed for its implementation on hardware by using DSP technique in C language coding on DSP board TMSF28335 as shown in Fig. 8. During implementation of experiments, robustness of the system, disturbance and tracking ability of the system were observed acutely. It is also investigated through experimental results. As results of the conventional controller are illustrated in Fig. 9 and experimental results of the proposed controller are described in Fig. 10, whereas Fig. (a) in both cases show voltage across condenser U, when 50 V, $V_{ref.}$ was provided. However, Fig. (b) shows the reference value for V_q, i.e. zero, as shown in Table I and it is observed that it stays zero throughout the experiment with slight variation that has almost negligible effect on the output. Fig. (c) depicts

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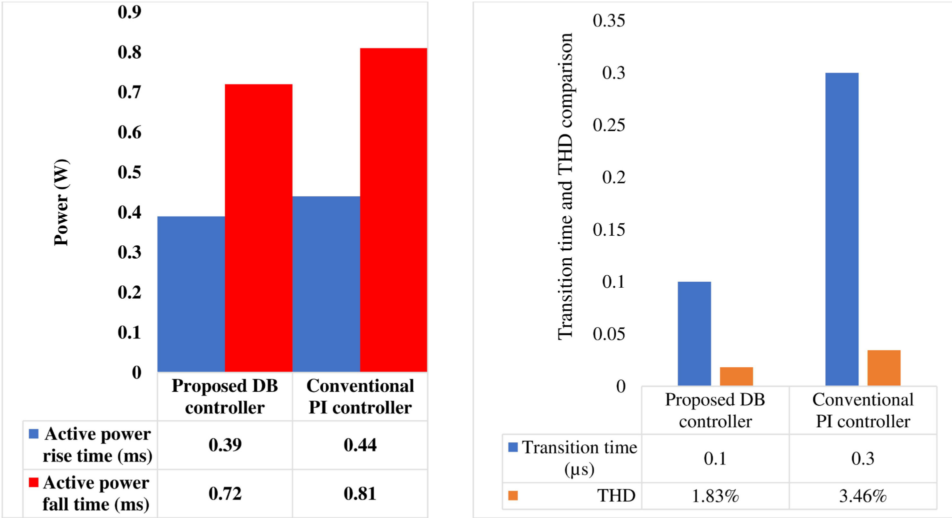

(a) (b)

Fig. 7. (a) Active power rise/fall time comparison of the proposed and the conventional controllers, (b) Comparison of THD and transition time between the proposed controller and the conventional controllers.

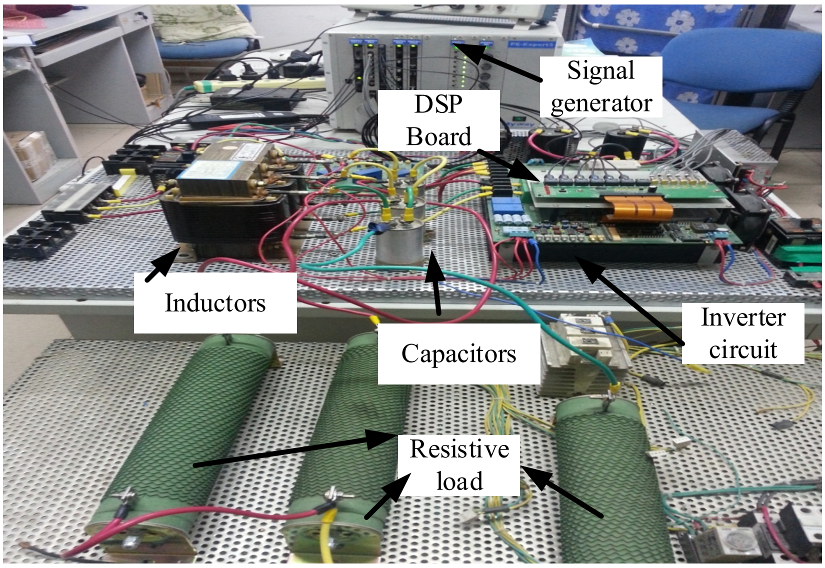

Fig. 8. Experimental setup of 3-phase VSI through the conventional/ proposed controller

V_d, the reference value of V_d was 50 V, as mentioned in Table I. Moreover, Fig. (d) shows condenser voltage across W phase. It can be observed that results are quite stable and no disturbance is detected across any frame of reference. The accurate response of VSI, when analyzed practically, leads to implementation of proposed technique on large scale for industrial benefits. However, in previous cases, experimental results were not verified in such comprehensive manners. System is observed for its robustness by acquainting it with several small uncertainties in the load and system was found robust and no change occurred in the wave forms. Moreover, dq components also remained smooth and stable, which shows it much better than previous results by various authors as mentioned in introduction part.

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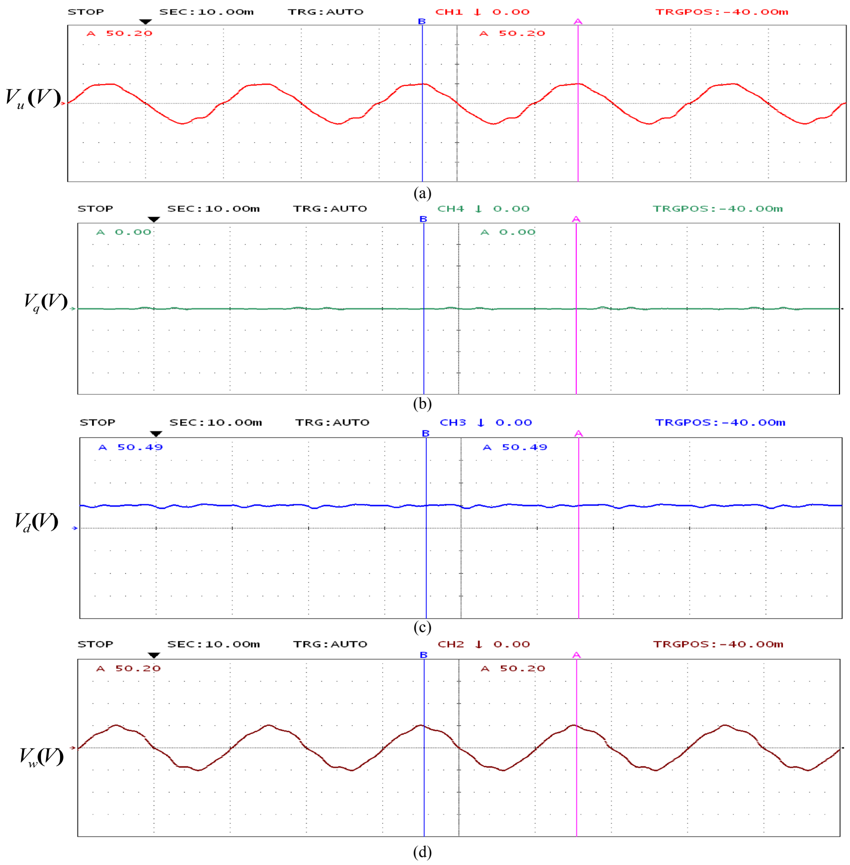

Fig. 9. (a)–(d) Experimental results of a conventional controller

As shown in Table I, the grid frequency was 50 Hz., and DC-Link voltage was 440 V, for a smooth output. Both the conventional controller as well as the proposed controller were coded and implemented on the laboratory prototype to observe their response. As a result, the conventional controller has comparatively larger harmonics and so THD value in its output wave as compared to the proposed controller. In fact, the nominal load, R_N is changed from 40 Ω to several different values for observing the system response in case of uncertain load. But it was observed that system remained highly stable. The value of V_B was 220 V as standard input. Therefore, a very smooth profile of a three-phase inverter is observed and any variations are hardly noticed. Changes in load current are expected and depicted in simulation results as the resistance of the system changes. After the transition period, smooth and stable signals for load current and load voltage are obtained in all frames of references. The tracking ability of the system and synchronization of reference frames can be profoundly observed through Figs. 9 and 10, where V_u, V_w, V_d and V_q showed the exact values, as referred to them. Mutually, the *dq*-components of voltage reach to the reference level in less than 3 msec., without any large shoots which shows good transient behavior and then stay at the reference levels with very small distortions showing robust steady state characteristics. However, the transient response of the proposed controller was comparatively much faster as compared to conventional controller.

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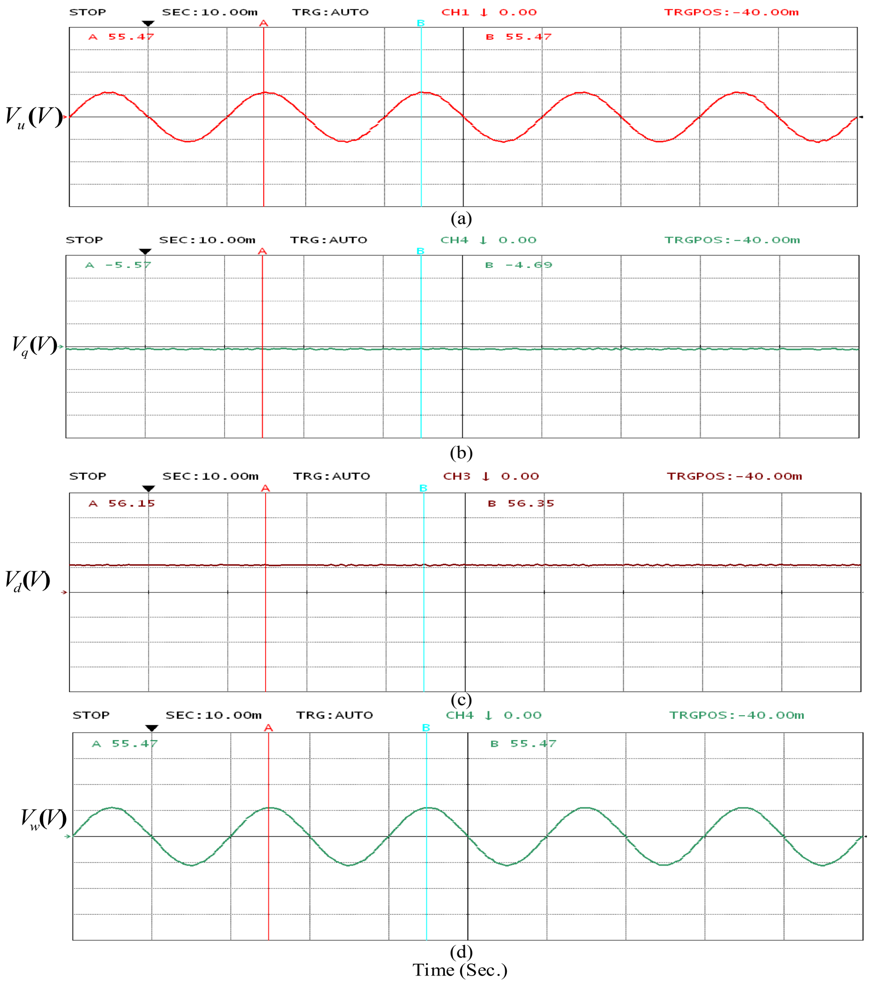

Fig. 10. (a)–(d) Experimental results of the proposed controller

9 Conclusions

To the best of author's knowledge, it has been verified through simulation and experimental setups that the proposed deadbeat technique is more accurate, reliable and effective than the conventional one. It has a *dq* minor current loop and a voltage major loop, presented with SVPWM technique and coordinates conversion. In this paper, a predictive disturbance observer is used for prediction of expected error in the next sampling time. The proposed technique plays a major role in digital control of a DSP based sinusoidal inverter. The simulation results depicted that the system modeling is quite appropriate and results are highly suitable. However, loop experiments with DSP coding show that no major distortion occurs and system remains stable with smooth output across all condensers and inductors in case of no load and resistive load, R_L conditions. At the end, the proposed technique is found comparatively better with less harmonic distortion and prompt response for a stand-alone LC integrated three-phase voltage source inverter.

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