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A two-step offset calibration in dynamic comparator using body voltage control

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Abstract: An accurate two-step offset calibration technique based on body voltage control for PMOS and NMOS devices is presented for dynamic latch type comparator. An efficient implementation of calibration logic is also introduced. Design issues and the function of the proposed scheme are discussed and simulated in 90 nm CMOS.

Keywords: comparator, offset calibration, flash ADC

Classification: Integrated circuits

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1 Introduction

As CMOS technologies have been developed, designs that utilize the advantages of digital circuits have increased steadily [1, 2, 3]. One example is the comparator design of the flash ADC. A comparator has been designed with a small size for low power consumption at the cost of an increased offset, and it has been digitally calibrated, which has become a generalized design technique in recent years [4, 5, 6, 7, 8]. Nevertheless, flash ADCs still suffer from large hardware overhead since the number of comparators to be calibrated grows exponentially with the ADC resolution. The calibration circuit area is mostly occupied by the number of D-flip-flops (DFFs) that store calibration data, and the number of DFFs is related to the calibration resolution, which is a reference for how accurately calibration is conducted. Ultimately, there is a trade-off between the area and accuracy. Since the one least-significant bit (1 LSB = ADC input full scale/2^N, N = ADC resolution) of the ADC decreases with an increase in the ADC resolution, the calibration resolution has to be increased further. The above-mentioned issue is well explained in the authors' papers [4] and [5]. [4] describes a 6-bit resolution ADC, and the number of DFFs required for approximately 3-bit calibration for each comparator was nine. Since a total of 34 comparators had to be calibrated, 306 DFFs were needed, and the layout area was 0.19 mm^2. [5] describes a 7-bit resolution, which was increased by 1 bit compared with that of [4]. Even though only 35 comparators required for calibration thanks to the cascaded latch interpolation technique, the offset requirements became tighter due to an increase in the ADC resolution, thereby performing 5-bit calibration. Thus, the total number of required DFFs was significantly increased to 1,190. However, the area was decreased to 0.12 mm^2 instead, even if the number of DFFs was increased by four times as a result of the sophisticated layout, although the reason for this was due to a finer process. However, because the area was still 1.5 times larger than the ADC core size (0.08 mm^2), a fundamental measure was still needed to reduce the area.

2 Circuit implementation

Fig. 1(a) shows the dynamic comparator that is widely used in ADCs [9]. The operation is explained briefly as follows: when the CLK is low, the M1 switch is off, and the M8 and M9 switches are turned on so that the outputs (V_{OP}, V_{ON}) are reset by pre-charging to the supply voltage (VDD). On the other hand, when the CLK becomes high, M1 is turned on and both M8 and M9 are off so that a different current according to the input voltages (V_{IP}, V_{IN}) is generated in the input pair, and the output nodes (V_{OP}, V_{ON}) are discharged. Once the output is discharged to VDD–$V_{TH,P}$ (the threshold voltage of M6 and M7), the transistors of M6 and M7 are turned on so that the outputs converge to VDD and the ground through positive feedback with an exponential function and the comparison is completed. Here,

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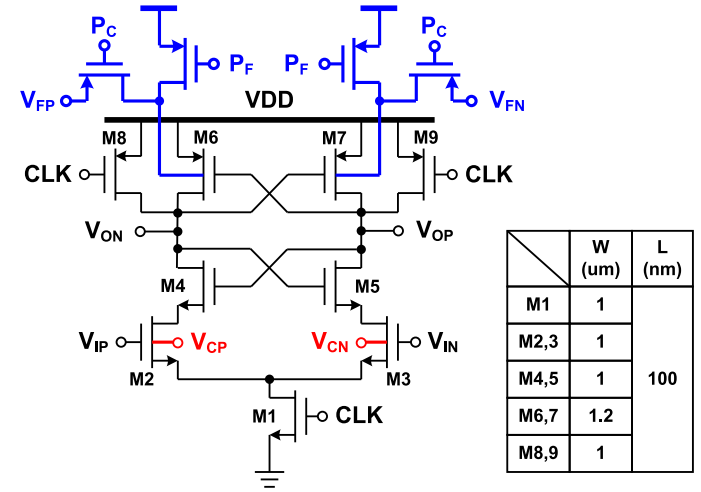
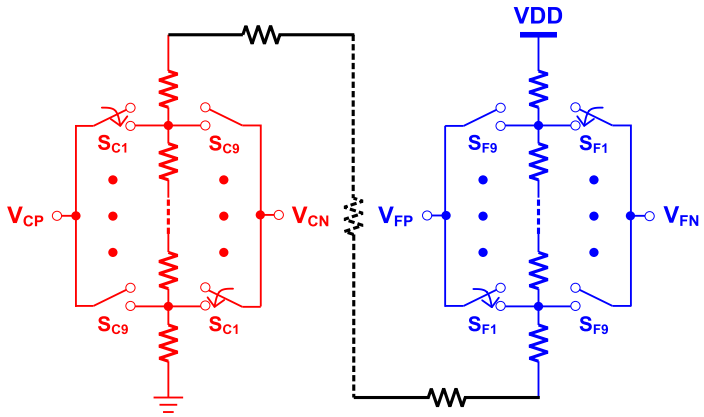
some conventional methods to calibrate the offset of the dynamic comparator that performs the above operation are discussed. In [4], a body voltage of input transistor was controlled, and in [5], the gate voltage of an additional input pair was adjusted. Another method using different capacitors is applied to the drain nodes of the input transistors [6] or a difference in the switch-off time is used to reset the input transistor drain node as reported in [10]. As found in the above methods, the wide calibration range can be generated through the input transistor whose offset contribution is the largest. As shown in Fig. 1, the present design performed a coarse calibration by controlling the body voltages (V_{CP}, V_{CN}) of the input transistors (M2, M3) differentially as verified by the author [4]. Furthermore, for a fine calibration, the body voltages of a cross-coupled PMOS (M6, M7) is used. The fine offset control can be achieved by changing $V_{TH,P}$, which is related to the turn-on voltage of M6 and M7 as explained in the above, while controlling the body voltages (V_{FP}, V_{FN}).

As shown in Fig. 1(a), there are switches connected to the body voltage of M6 and M7. The role of these switches is that when a coarse calibration is performed, P_F (fine calibration period) becomes low (P_C = High) so that the body voltage of



	W (um)	L (nm)
M1	1	
M2,3	1	
M4,5	1	100
M6,7	1.2	
M8,9	1	

(a)



(b)

Fig. 1. Proposed two-step offset calibration using body voltage control (a) dynamic comparator with the sizes of devices (b) coarse and fine DAC

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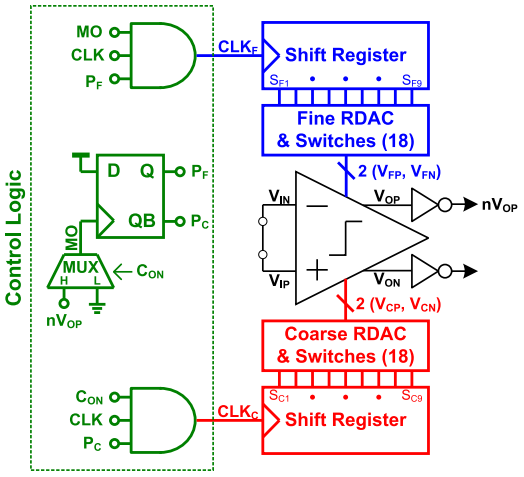
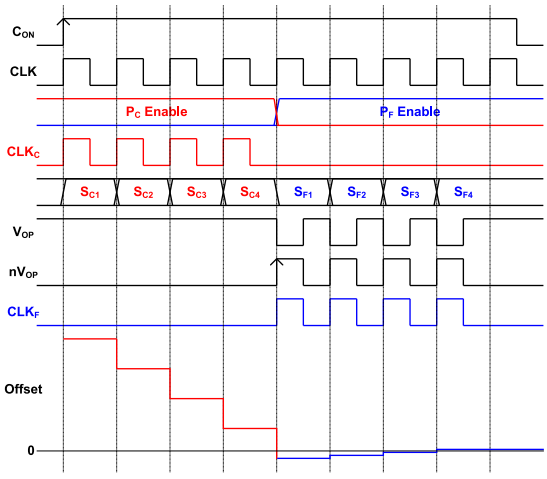
both M6 and M7 is connected to VDD. On the other hand, when a fine calibration is performed, P_C (coarse calibration period) becomes low (P_F = High) so that the body voltage is connected to the fine digital-to-analog converter (DAC) in Fig. 1(b). More details will be discussed later.

Fig. 1(b) shows the coarse and fine DACs for calibration reference generation. A required reference voltage can be generated efficiently via a single resistive ladder using the ground and VDD of the ADC without the need to separately generate a reference voltage for the calibration as reported in [4] and [5]. Although a total of 36 switches (18 coarse and 18 fine) are needed in nine steps of coarse and fine calibrations, only 18 DFFs are needed because the switches are differentially controlled. Since the two-step control in nine steps is used, it is equivalent to calibration of approximately 6 bits. If the conventional method is used, 81 DFFs are needed. Thus, the significant area reduction with same accuracy can be expected.

The two-step calibration logic and timing diagram that explains the operation in detail are shown in Fig. 2. The calibration logic consists of the coarse and fine DAC and a pair of shift registers that generate the timings and stores calibration data, and the control logic is marked in the dotted box. The DFF in the control logic



(a)



(b)

Fig. 2. Coarse and fine calibration logic and operation (a) block diagram (b) timing diagram

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is reset to be VDD at node P_C and ground at node P_F initially. Once the C_{ON} signal that determines the on/off state of the calibration becomes high, the comparator differential input is set to zero by connecting both inputs to the input common mode voltage. Furthermore, once the clock signal (CLK_C) from the coarse control logic is input through the shift register, the output of the shift register is turned on sequentially from S_{C1} to S_{C9}. When the first switch (S_{C1}) is turned on, the output V_{OP} of the comparator is made VDD initially by designing a coarse range wider than the offset due to the device mismatch. Once the offset of the comparator is calibrated as the switch turns on sequentially, zero-crossing occurs at the output of the comparator (nVop: low → high). Then, because P_F and P_C values are inverted by the DFF in the control logic, CLK_C stops clocking and the final output data are stored in the shift register to complete the coarse calibration. Simultaneously, the P_F signal becomes high and the fine-control logic that receives the nV_{OP} signal generates the clock signal (CLK_F) to start the fine calibration. The shift register turns the switch on sequentially from S_{F1} to S_{F9} until the fine calibration is complete as zero-crossing occurs at the output of the comparator again. Once the fine calibration is complete and C_{ON} is switched from high-to-low for normal operation of the comparator, the multiplexer (MUX) output (MO) in the control logic is changed to the ground so the comparator output no longer influences the calibration.

3 Function verification

The comparator with the two-step calibration is implemented and simulated in a 90-nm CMOS process with 1.2 V supply voltage. The calibration range of the proposed calibration scheme should be carefully designed, because the body voltage of the transistor must be lower than the turn-on voltage of the PN Junction. In order to verify this condition, the simulations are performed in 100°C, FF corner. Assume that when the body leakage current flows up to 100 nA is allowed, the NMOS (W/L = 1 um/100 nm) for coarse calibration is about 0.35 V and the PMOS (W/L = 1.2 um/100 nm) for fine calibration is about VDD-0.39 V.

The Monte-Carlo simulation results indicate that the $\pm 3\sigma$ input referred offset of the comparator with the transistor size in Fig. 1(a) is about 39 mV. Even if the offset is varied depending on the process and temperature, the coarse calibration range must be larger than the simulated 3σ offset of 39 mV. As a result, 0~0.3 V coarse range is decided and the results show that the narrowest range at −30°C, FF corner is 40.9 mV in Fig. 3. A redundancy is required for fine calibration range, so that the full scale of the fine calibration range is chosen to have a wider range than the 1 LSB of the coarse calibration range. In order to satisfy this condition, the fine calibration range is used to 0.9~1.2 V. As shown in Fig. 3, the narrowest fine calibration range is 7.17 mV at −30°C, SF corner, and 1 LSB of the coarse calibration range of 5.17 mV at the same corner can be covered. The largest residue offset (= fine calibration 1 LSB) is guaranteed to be less than 1.55 mV at 100°C, FF corner. In case of the 7b ADC design with the input range of 800 mVpp, the above results show that the comparator offset requirement can be designed robustly to 1/4 LSB for all process corners and temperature range (−30~100°C).

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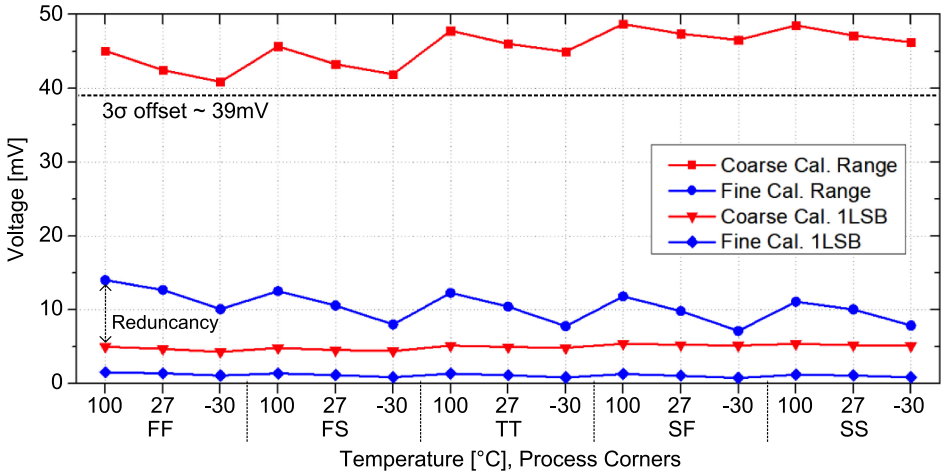

Fig. 3. Simulation result of coarse and fine calibration range depending on the temperature and all process corners

4 Conclusion

In this letter, high accuracy two step offset calibration, which can reduce the complexity of the logic significantly, is proposed and an implementation that practically uses the body voltages control in the comparator is introduced. The simulated results in 90 nm CMOS show that the offset can be reduced by 96.6~98.3% using the proposed technique for all process corners and a temperature range of −30~100°C. The proposed two-step offset calibration is particularly suitable for a 6–8 bit flash ADCs design.

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