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A novel coupled inductor Z-source three-level inverter

Xiaogang Wang[a)], **Hua Liu, and Yitao Li**

College of Mechanical and Electrical Engineering, Guangzhou University, 230 Waihuan Xi Road, Guangzhou 510006, China

a) *wxg@gzhu.edu.cn*

Abstract: A novel Z-source three-level inverter based on coupled inductors is proposed. The two inductors in traditional Z-source impedance network are replaced by two coupled inductors. The operating principle is described and the equations of boost factor and voltage stresses are deduced. Comparisons are made with other Z-source three-level inverters, especially the multicell switched inductor Z-source three-level inverter. The two topologies have same boost factor if a specific condition is met, but the proposed inverter uses less components and therefore the reliability is improved. SVPWM method for conventional three-level NPC inverter is easy to apply to the novel inverter after a simple modification. Simulations are conducted to verify the theoretical analysis.

Keywords: Z-source inverter, coupled inductor, switched inductor, three-level, neutral-point-clamped

Classification: Power devices and circuits

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1 Introduction

The three-level neutral-point-clamped (NPC) inverter has many advantages over two-level inverter: lower switching device voltage stress, better harmonic performance with lower operating frequency and smaller output filters [1, 2, 3]. However, the conventional three-level NPC inverter can only behave as a step-down converter, whose input dc voltage must be greater than its output ac line voltage amplitude, which limits its application.

Z-source inverter (ZSI) is one of the most promising topologies. An "X-shaped" impedance network is employed in conventional two-level ZSI, which consists of two inductors and two capacitors. The input dc voltage and the bridge circuit are connected to the two ports of the impedance network respectively. The impedance network can boost the input dc voltage with the help of shoot-through operation, thus the input dc voltage level can be reduced. Moreover, shoot-through becomes a normal state, so the reliability is improved.

The Z-source concept can also be applied to three-level inverters. P. C. Loh et al. proposed a dual-Z-source three-level inverter [4], which uses two sets of Z-source impedance networks and therefore increases the cost. The single Z-source topology is proposed in [5, 6] and it uses only half the passive elements and only one dc voltage source. Compared to the dual Z-source inverter, the single Z-source inverter has almost identical performance. Quasi-Z-source inverter is another topology derived from Z-source inverter. A single phase quasi-Z-source three-level inverter is studied in [7]; one of its advantages is the continuous input current

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because two inductors are directly connected to the dc voltage supply. One disadvantage of the above Z-source three-level inverters is the inter-constraint between its boost factor and modulation index, so their voltage gains are still not very high. W. Mo et al. proposed a Trans-Z-source NPC inverter and a Γ-Z-source NPC inverter [8]; each uses two coupled transformers to replace the two inductors in the conventional Z-source impedance network. The voltage gain can be increased by designing the turns ratio of the transformer. In literature [9], a three-level LC-switching-based voltage boost NPC inverter is discussed which uses less number of high-power passive components. However, two extra switches are introduced which need gating signals to turn them on and off. Another high boost factor topology is multicell switched inductor Z-source three-level inverter [10]. Its boost factor increases with the cell number significantly, but the number of Z-source network components increases apparently too. Converters utilizing coupled inductors have many advantages, such as low output current and voltage ripple, fast load transient and low output decoupling capacitance [11]. Recently, many new topologies based on coupled inductors are proposed [12, 13, 14, 15].

This paper presents a novel coupled inductor (CL) Z-source three-level inverter. Section 2 introduces the inverter topology and its operating principle. Section 3 compares the proposed inverter with several other Z-source three-level inverters. Section 4 describes the space vector pulse width modulation method. The performance of the proposed inverter is evaluated through simulation, and the results are shown in Section 5.

2 Principle of coupled inductor Z-source three-level inverter

Fig. 1 shows the main circuit of the proposed CL Z-source three-level inverter. The two inductors in conventional Z-source three-level inverter are replaced by two coupled inductors and four diodes (D_1, D_2, D_3 and D_4). Each coupled inductor has two windings, the numbers of turns of the primary and the secondary windings are n_p and n_s respectively. The turns ratio is greater than 1:

$$N = \frac{n_s}{n_p} > 1 \tag{1}$$

The square of the coupling factor k can be expressed as

$$k^2 = \frac{L_m}{L_m + L_k} \tag{2}$$

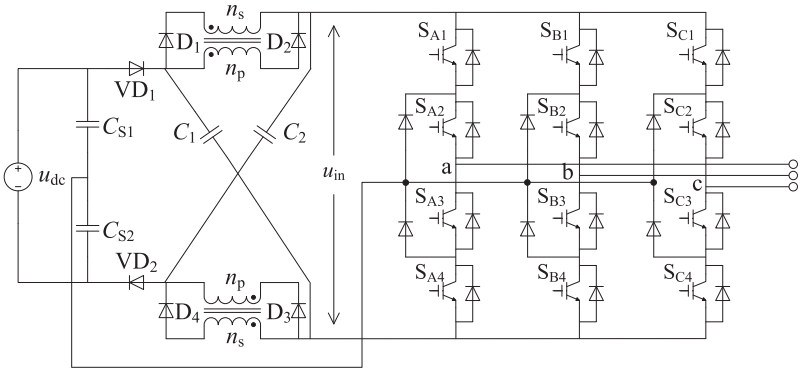

Fig. 1. Topology of coupled inductor Z-source three-level inverter

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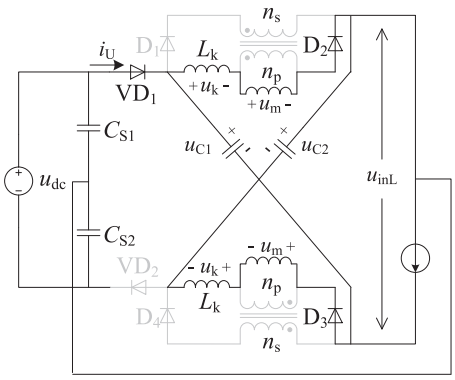
where L_m and L_k are the excitation inductance and the leakage inductance respectively.

The CL Z-source three-level inverter can operate in three states: upper shoot-through state, lower shoot-through state and nonshoot-through state. Fig. 2 shows their equivalent circuits for analysis, the NPC inverter is represented by one or two ideal current sources for simplification.

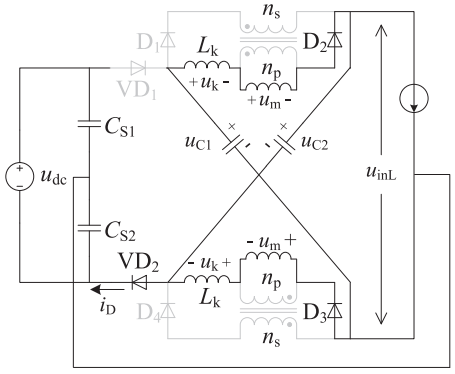
The equivalent circuit for upper shoot-through state is shown in Fig. 2(a). It is assumed that phase A operates in upper shoot-through state, switches S_{A1}, S_{A2}, S_{A3} and diode VD_{A2} in Fig. 1 conduct. In the impedance network, VD_1 and D_2 are forward biased; the voltage of capacitor C_{S1} is applied to the leakage inductance along with the excitation winding. The voltage across the excitation winding is denoted as u_m and the voltage across the secondary winding is Nu_m, so diode D_1 block. Current i_U flows into the impedance network through diode VD_1. For the negative bus, VD_2 and D_4 block while D_3 conducts. Fig. 2(b) shows the equivalent circuit for lower shoot-through state. Now suppose phase A operates in lower shoot-through state, switches S_{A2}, S_{A3}, S_{A4} and diode VD_{A1} in Fig. 1 conduct. In the impedance network, VD_2, D_2 and D_3 conduct, VD_1, D_1 and D_4 block. Current i_D flows out of the impedance network through diode VD_2.

In shoot-through states, the energy stored in split capacitors is delivered to the coupled inductors. The voltage equations in both states are

$$\begin{cases} u_k + u_m = u_{dc}/2 \\ u_{inL} = u_{C2} - u_m - u_k \end{cases} \tag{3}$$



(a) Upper shoot-though state



(b) Lower shoot-through state

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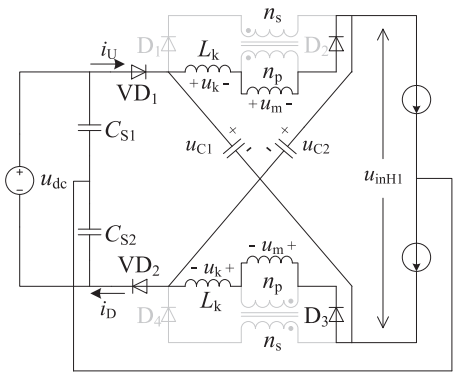
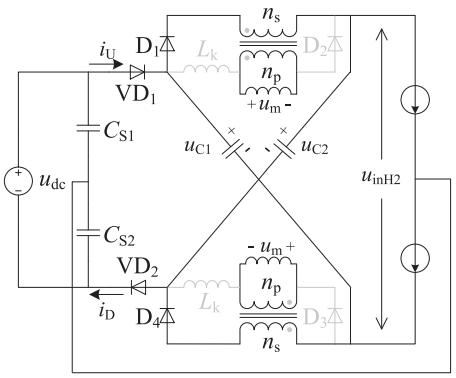


(c) Nonshoot-through state (leakage inductance releasing energy)



(d) Nonshoot-through state (leakage inductance finishes releasing energy)

Fig. 2. Equivalent circuits of the inverter in different operating states

where u_{inL} is the low peak value of the dc-link voltage, u_k is the leakage inductance voltage. From (2) and (3), we have $u_m = k^2 u_{dc}/2$.

The equivalent circuit of the inverter operates in nonshoot-though state is shown in Fig. 2(c) and Fig. 2(d). In Fig. 2(c), diodes VD_1, VD_2, D_1 and D_4 conduct, diodes D_2 and D_3 block. The energy in the leakage inductance begins to release and the excitation winding voltage during which is

$$\begin{cases} u_m = k^2(u_{dc} - u_{C2}) \\ u_{inH1} = u_{C2} - u_m - u_k \end{cases} \tag{4}$$

where u_{inH1} is the high peak value of the dc-link voltage during the release of the leakage inductance energy.

It takes time T_1 for the leakage inductance energy to reach zero. Switching period and the duty ratio of T_1 are denoted as T_s and d_1 respectively, so $T_1 = d_1 T_s$. After that, the equivalent circuit is shown in Fig. 2(d). The voltage equations in nonshoot-through state are as follow.

$$\begin{cases} u_m = (u_{dc} - u_{C2})/N \\ u_{inH2} = u_{C2} - N u_m \end{cases} \tag{5}$$

where u_{inH2} is the high peak value of the dc-link voltage after the release of the leakage inductance energy.

The duty cycles for the upper and lower shoot-through states are identical and denoted as d_s. Applying volt-second balance to the excitation winding we have

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$$\frac{k^2 u_{dc}}{2} \cdot 2d_s + k^2(u_{dc} - u_{C2}) \cdot 2d_1 + (1 - 2d_s - 2d_1) \cdot \frac{u_{dc} - u_{C2}}{N} = 0 \tag{6}$$

The impedance network capacitor voltage u_{C2} is deduced from (6) as

$$u_{C2} = \frac{1 - 2(1 + k^2 N)d_1 + (k^2 N - 2)d_s}{1 - 2d_s + 2(k^2 N - 1)d_1} u_{dc} \tag{7}$$

Because the symmetry of the impedance network, the two capacitors have equal voltages, that is, $u_{C1} = u_{C2} = u_C$. From (5) and (7), the high peak value of the dc-link voltage is written as

$$u_{inH2} = \frac{1 - 2d_1 + 2(k^2 N - 1)d_s}{1 - 2d_s + 2(k^2 N - 1)d_1} u_{dc} = B_{CL} u_{dc} \tag{8}$$

where B_{CL} is the boost factor. If $k^2 = 1$ and $d_1 = 0$, (8) is simplified as

$$u_{inH2} = \frac{1 + 2(N - 1)d_s}{1 - 2d_s} u_{dc} = B_{CL} u_{dc} \tag{9}$$

The diode VD_1 in lower shoot-through state and diode VD_2 in upper shoot-through state have same voltage stresses:

$$u_{VD1} = u_{VD2} = u_C - \frac{u_{dc}}{2} = \frac{1}{2} \cdot \frac{1 + 2(N - 1)d_s}{1 - 2d_s} u_{dc} \tag{10}$$

Diodes D_1 and D_4 have equal voltage stresses in two shoot-through states:

$$u_{D1} = u_{D4} = (N - 1)u_m = \frac{N - 1}{2} u_{dc} \tag{11}$$

Diodes D_2 and D_3 have identical voltage stresses in nonshoot-though state:

$$u_{D2} = u_{D3} = (1 - N)u_m = \frac{N - 1}{N}(u_{dc} - u_C) = \frac{(N - 1)d_s}{1 - 2d_s} u_{dc} \tag{12}$$

Fig. 3 illustrates the curves of impedance network capacitor voltage stress, voltage stress of diodes (VD_1 and VD_2) and voltage stress of diodes (D_2 and D_3) versus shoot-through duty cycle d_s and turns ratio N. The voltage stress of D_1 and D_4 expressed in (11) is simple and only relies on N, so it is not shown in Fig. 3. As seen in Fig. 3, the three surfaces have similar shapes. All the voltage stresses increase with turns ratio N when the duty cycle d_s is fixed and increase with d_s when N is fixed.

3 Comparisons with other Z-source three-level inverters

Several Z-source three-level inverters have been proposed to achieve some advantages. Some of them use transformers [8], which are similar to the proposed CL Z-source three-level inverter. A trans-Z-source three-level topology and a Γ-Z-source topology are shown in Fig. 4 and Fig. 5 respectively. One obvious drawback of the two inverters is that the transformer turns ratio and the shoot-through duty ratio interact on each other. The boost factors of the two inverters are expressed as

$$B_T = \frac{2}{1 - (1 + N_T)d_s} \tag{13}$$

$$B_\Gamma = \frac{2}{1 - [1 + 1/(N_\Gamma - 1)]d_s} \tag{14}$$

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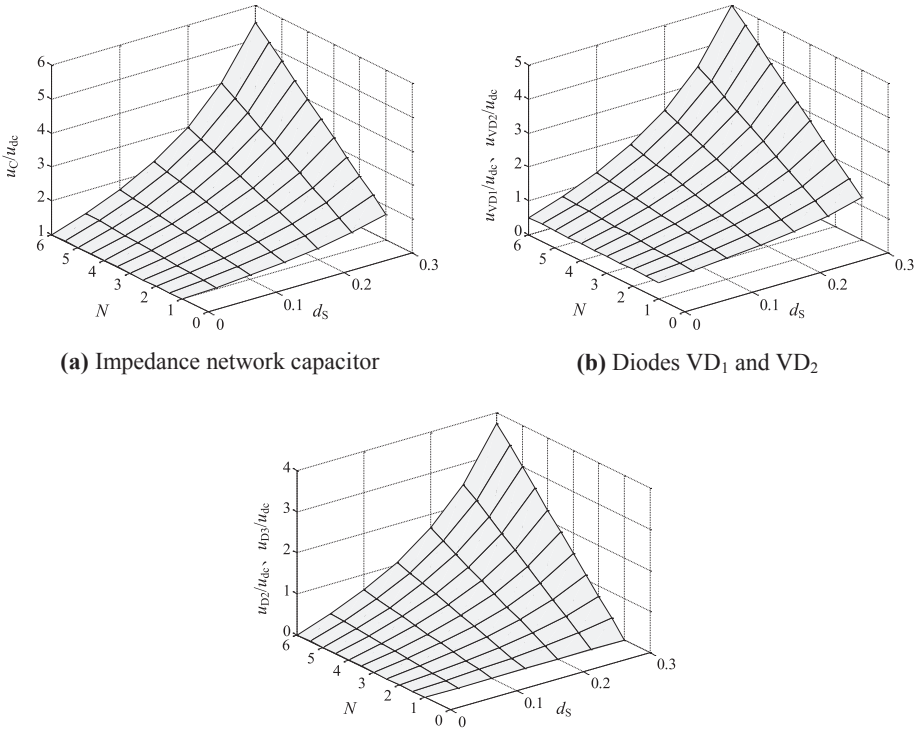

(a) Impedance network capacitor

(b) Diodes VD_1 and VD_2

(c) Diodes D_2 and D_3

Fig. 3. Impedance network capacitor voltage stress and diode voltage stresses versus turns ratio N and shoot-through duty cycle d_s.

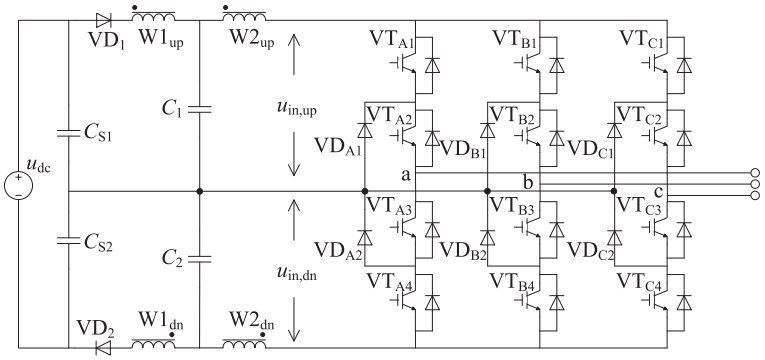

Fig. 4. Trans-Z-source three-level inverter

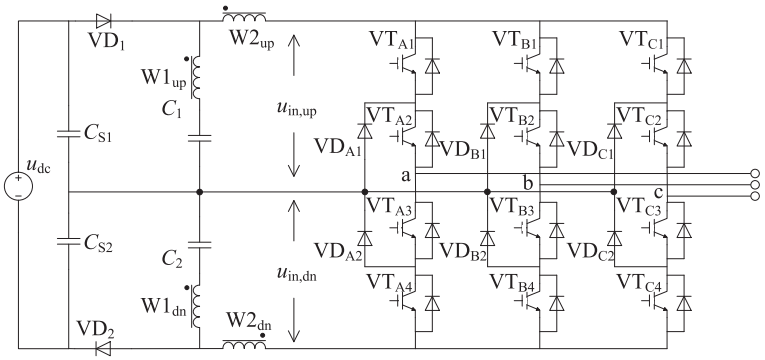

Fig. 5. Γ-Z-source three-level inverter

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where N_T and N_Γ are the turns ratios of the transformers used in Trans-Z-source and Γ-Z-source topologies respectively. Their shoot-through duty ranges are $0 \le d_s < 1/(1+N_T)$ and $0 \le d_s < 1/[1+1/(N_\Gamma - 1)]$ respectively. Such interactions restrict their voltage boost capabilities. For CL Z-source three-level inverter whose boost factor is expressed in (9), the turns ratio is eliminated in the denominator. Therefore its boost factor can be very high by choosing a large N.

Another topology of Z-source three-level inverter base on switched inductor (SL) is studied in [10] and is drawn in Fig. 6. The two switched inductors are connected in the positive and negative buses; each of them consists of two inductors and three diodes.

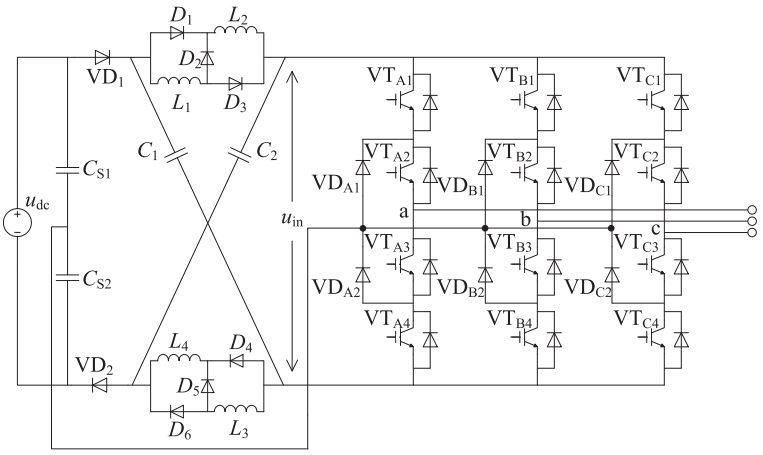
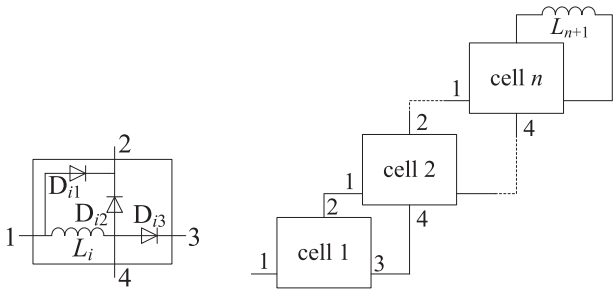


Fig. 6. Switched inductor Z-source three-level inverter

In order to improve the voltage boosting capability, multiple switched inductor cells can be cascaded, as illustrated in Fig. 7(b). Each cell in Fig. 7(b) consists of one inductor and three diodes, as shown in Fig. 7(a). The boost factor for the multicell SL Z-source three-level inverter is

$$B_{SL} = \frac{1+2nd_s}{1-2d_s} \tag{15}$$

where n is the number of SL cells. The cell number is not included in the denominator, so high boost factor can be achieved as CL Z-source three-level inverter.



(a) SL cell **(b)** Connection of SL cells

Fig. 7. Multicell switched inductor

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These two inverters are compared in detail to identify the relationships between them. Table I lists the main parameters of the two inverters. As seen from Table I, if the turns ratio of the coupled inductor equals the cell number of the switched inductor plus one, that is, $N = n + 1$, the two inverters have equal boost factors. In addition, the impedance network capacitors in two inverters have identical voltage stresses with $N = n + 1$. Under this condition, diodes VD_1 and VD_2 in two inverters also have same voltage stresses. The voltage stresses of diodes D_1 and D_4 in CL inverter increase with N while the voltage stresses of diodes D_{i2} and D_{i5} in SL inverter increase with n and d_s. Voltage stresses of diode D_2 and D_3 in CL inverter are larger than those of D_{i1}, D_{i3}, D_{i4} and D_{i6} in SL inverter if $N = n + 1$ and $n \geq 2$. Although the CL inverter has no reductions in component voltages stresses, it uses fewer components in Z-source network than the SL inverter.

Table I. Comparisons between SL and CL Z-source three-level inverters

	CL	SL
Boost factor	$\frac{1+2(N-1)d_s}{1-2d_s}$	$\frac{1+2nd_s}{1-2d_s}$
Impedance network capacitor voltage stress	$\frac{1+(N-2)d_s}{1-2d_s}u_{dc}$	$\frac{1+(n-1)d_s}{1-2d_s}u_{dc}$
Diode voltage stress 1 (u_{VD1} and u_{VD2} for both inverters)	$\frac{1}{2}\cdot\frac{1+2(N-1)d_s}{1-2d_s}u_{dc}$	$\frac{1}{2}\cdot\frac{1+2nd_s}{1-2d_s}u_{dc}$
Diode voltage stress 2 (u_{D1} and u_{D4} for CL inverter, u_{Di2} and u_{Di5} for SL inverter)	$\frac{N-1}{2}u_{dc}$	$\frac{(n+1)d_s}{2(1-2d_s)}u_{dc}$
Diode voltage stress 3 (u_{D2} and u_{D3} for CL inverter, u_{Di1}, u_{Di3}, u_{Di4} and u_{Di6} for SL inverter)	$\frac{(N-1)d_s}{1-2d_s}u_{dc}$	$\frac{(n+1)d_s}{n(1-2d_s)}u_{dc}$

4 SVPWM method

NPC inverter can be modulated by carrier-based PWM methods or space vector PWM (SVPWM) methods. This paper uses SVPWM algorithm to modulate the CL Z-source three-level inverter. With only a slight modification to the PWM method for conventional three-level NPC inverter, the CL Z-source three-level inverter can operate with maximum boosting ability. The reference voltage vector rotates anti-clockwise in each cycle and its vertex passes through six large sectors S_1~S_6. Each large sector is divided into six small triangles. When the reference voltage vector vertex is located in a specific small triangle, it is synthesized by the three nearest active voltage vectors. For example, if the reference voltage vector vertex is located in triangle C_1 of sector S_1 (S_1-C_1), it is synthesized by active vectors $\boldsymbol{V}_1$, $\boldsymbol{V}_2$ and $\boldsymbol{V}_7$, as shown in Fig. 8. The 12 gating signals for S_1-C_1 are shown in Fig. 9. Compared with traditional gating signals, the lower shoot-through states are inserted by turning on VT_{C4} early and turning off VT_{C4} late at time t_1 and t_4 respectively. While the upper shoot-through states are inserted by turning on VT_{A3} early and

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turning off VT_{A3} late at time t_2 and t_3 respectively. The durations of upper and lower shoot-through in half a switching period are t_{US} and t_{DS} respectively, and $t_{US} = t_{DS}$.

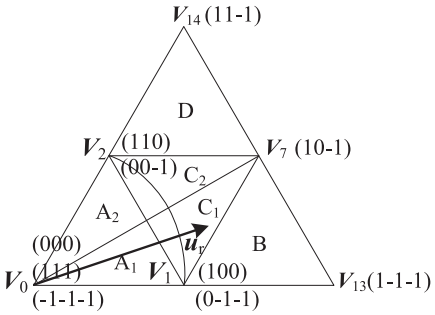

Fig. 8. Division of large sector S_1

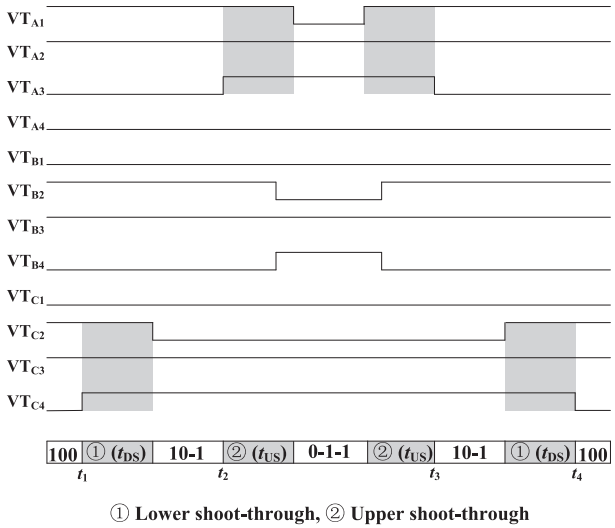

Fig. 9. Modulation of CL Z-source three-level inverter (sector S_1, triangle C_1)

5 Simulation studies

The features of the proposed CL Z-source three-level inverter are verified under MATLAB/Simulink environment. As a comparison, the switched inductor Z-source three-level inverter is also studied. The two inverters use same main parameters: The dc side voltage u_{dc} is 200 V. The Z-source impedance network capacitances are $C_1 = C_2 = 2200\,\mu F$. The CL Z-source impedance network has no inductors while the inductances in SL Z-source impedance network are $L_1 = L_2 = \ldots = L_{2(n+1)} = 1.2\,mH$. The switching frequency $f_s = 10\,kHz$. The turns ratios of the two coupled inductors are $N = 3$, while the number of SL cells is $n = 2$. Thus the condition $N = n + 1$ is met. For both inverters, the boost factors are $B = 12.13$, i.e. $d_s = 0.3938$.

The waveforms of the two inverters are almost identical, so only results of the CL Z-source three-level inverter are shown in Fig. 10. As shown in Fig. 10(a), the dc-link voltage is composed by many pulses whose high peak and low peak values

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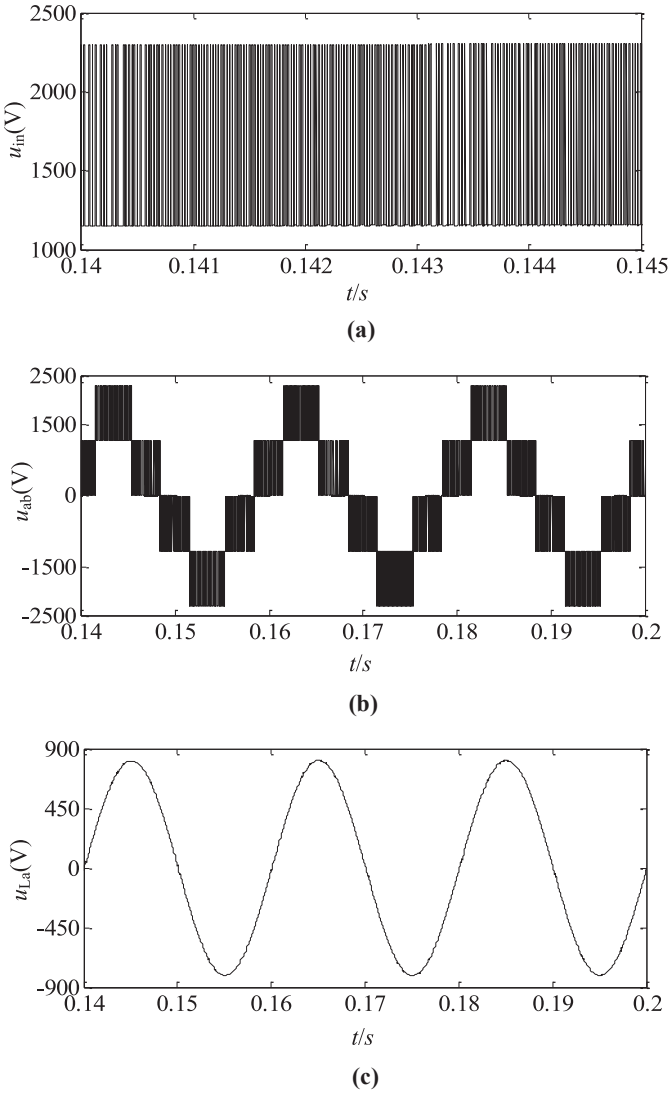

Fig. 10. Simulation results

are about 2382 V and 1191 V respectively. According to the given boost factor, the expected dc-link voltage high peak value is $u_{inH2} = 12.13 \times 200 = 2426$ V. The difference between the expected value and the actual value (2426 V − 2382 V = 44 V) is caused by voltage drop across the equivalent resistances, since no closed loop control is introduced. Fig. 10(b) shows the line voltage before the output filters. It can be seen that the line voltage amplitude is 2382 V. Fig. 10(c) shows the load phase voltage; its amplitude is about 831 V, also a bit smaller than its expected value 849 V ($0.7 \times 12.13 \times 200/2$). The simulations results show that the theoretical analysis is correct. The CL Z-source three-level inverter has strong voltage boosting capability.

6 Conclusions

In this paper, a novel coupled inductor Z-source three-level NPC inverter is studied. Two coupled inductors are used to replace the two inductors in conventional single Z-source impedance network. Compare to the single Z-source impedance network, the proposed inverter has higher boost factor. The novel topology also can achieve

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same boost factor as multicell switched inductor Z-source three-level inverter if $N = n + 1$ is satisfied, but its reliability is improved due to the smaller number of components. SVPWM method for conventional three-level NPC inverter is easy to apply to the novel inverter with only a slight modification. Simulation results are provided to verify the features of the proposed topology. For future work, experimental verification will be carried out.

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