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Adaptive supply and body voltage control for ultra-low power microprocessors

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Abstract: Power dissipation is a dominant aspect that limits the performance of microprocessors. In this work adaptive supply and body voltage control is used by applying optimum V_{dd} and NMOS-PMOS body bias voltages ($V_{BB\text{-}N}$ & $V_{BB\text{-}P}$) to the microprocessor unit, which compensate the threshold voltage and clock frequency for ultra-low power design. SPICE simulation measurements on a 22-nm technology are used to evaluate the theoretical basics and fundamentals. The results show that, optimal amount of power consumption and temperature reduction have been obtained for different workload and simulation environments.

Keywords: adaptive voltage scaling, body bias, power dissipation

Classification: Integrated circuits

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1 Introduction

The advanced high performance technology translates into high power dissipation of microprocessors at a dramatic alarmingly rapid rate, and bringing forth extra temperature generation, procreate a vast demand into low power adaptive design for maximal power efficiency in real time.

The scaling of supply voltage (V_{dd}) for power aware processors reduces dynamic power consumption to very low limits but reduces the system performance simultaneously. V_{dd} scaling requires a reduction in threshold voltage (V_{th}) and consequently increasing leakage power exponentially. In order to ensuring low power operation for efficient power and temperature aware design, finding optimal combination set of V_{dd} and possibly body bias voltages (V_{BB}) that ensures the required performance of the portable processors is compulsory [1].

The theory and design of power dissipation reduction has strong face validity in recent publications such as; minimize the leakage power using supply and body-bias voltage using a look-up-table method for nanoscale VLSI systems [2], determining a set of supply-body bias voltage combinations to achieve the minimum energy consumption for a target frequency [3], analysis and determination of the best switching management strategy for dynamic set of operating environment in terms of process choices, circuit activity, and temperatures [4], particle swarm optimization (PSA) algorithm for leakage power reduction in VLSI circuits [5], finally, a method and flow for implementing a clock tree inside an application-specific integrated circuit (ASIC) for near-threshold/subthreshold technology with optimal power dissipation [6].

This study proposed theoretical and practical limits of combined body bias/threshold and supply voltage for optimal power dissipation contribution. Voltage scaling and body biasing are efficient low power/thermal management technique used in processors and digital designs. It offers an optimum solution for the CPU power and temperature issues. SPICE simulator is used to verify the theoretical approach and confirm the design operations. The results show that, optimal considerable amount of power consumption reduction as well as thermal reduction challenges are obtained as compared to previous studies, and it shows the greatest promise in processor's thermal-energy optimization effectively.

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2 Optimal supply and body voltage control

Techniques for lowering power dissipation of today's high performance and portable computation processors are the most important issues facing manufactures. Power, temperature and performance are steadily correlated. Achieving ultra-low power is essential concurrently with maintaining the target performance for different workloads characterization.

The main sources of power dissipation in CMOS circuits are; dynamic, and static power. Dynamic power results from the charging and discharging of parasitic load capacitances between different voltage levels, while static power is primarily caused by subthreshold leakage current between voltage supply and ground. As the transistor is scaled down to the deep sub-100 nm and below technologies, the tunneling oxide leakage appears and increases leakage power significantly. The gate leakage power is significant in portable electronic devices that executing dynamic workloads, correspondingly generating high temperatures [7]. The total power dissipation can be written as given in Eq. (1).

$$P_{total} = P_{dynamic} + P_{static} = \alpha C {V_{dd}}^2 f + {V_{dd}}^2 K_1 e^{\left[\frac{V_{gs}-V_{th}}{nV_T}\right]}\left[1 - e\frac{V_{ds}}{V_T}\right]T_c \quad (1)$$

Where, $P_{dynamic}$ is the dynamic power, P_{static} is the static dissipation, α is the activity factor of the output node, C is load capacitance, V_{dd} is the supply voltage, f is the operating clock frequency, K_1 is the technology related factor, V_T is the thermal voltage that is equal to kT/q $\approx$ 26 mV, and T_C is the clock period [8].

Static/leakage current has an exponential relation to the threshold voltage and a quadratic relation to temperature (T). The total power can be reduced dramatically using threshold voltage scaling through modulating the body bias voltage. Reverse body bias (RBB) raises the threshold voltage and makes the transistor slower and lower leakage, concurrently maintaining the target performance based on the voltage and frequency scaling [9]. Increasing threshold voltage (V_{th}) through body bias voltage variation is efficient for reducing leakage current as well as the total power dissipation. The RBB affects V_{th} through body effect, and subthreshold leakage current has an exponential dependence on V_{th} as given in Eq. (2).

$$I_{subthreshold} = \frac{\mu W C_{dep}}{L} {V_T}^2 e^{\frac{|V_{gs}|-|V_{th}|}{nV_T}}\left(1 - e^{\frac{-|V_{ds}|}{V_T}}\right) \quad (2)$$

Where, Where $C_{dep} = \sqrt{\varepsilon_{si} q N_{sub}/(4\phi_B)}$ is capacitance of depletion region under the gate area, ε_{si} is the permittivity of Si, q is the electron charge, N_{sub} is the doping concentration of the p-substrate, ϕ_B is the built-in potential, C_{ox} is the oxide capacitance per unit area between the gate and the bulk surface, and n is the subthreshold parameter and is expressed as $1 + C_{dep}/C_{ox}$ [10].

The energy delay product (EDP) is a metric multiplied the average energy per instruction by the average inter-instruction delay, and their product reflects the success of the optimal design of low power MOSFET circuits. For optimal supply and threshold voltage scaling, EDP expression can be differentiate with respect to V_{dd} and V_{th} and set to zero to obtain $V_{dd\text{-}opt}$ as given by Eq. (3).

$$V_{dd\text{-}opt} = \frac{3}{3-\alpha} V_{th} + \frac{3\alpha}{3-\alpha} \quad (3)$$

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This equation provides the optimal supply voltage ($V_{dd\text{-}opt}$) as a function of V_{th}. The $V_{dd\text{-}opt}$ can be easily regulate for each corresponding V_{th} value. While, the optimal threshold voltage ($V_{th\text{-}opt}$) varies due to the corresponding body bias voltage (V_{BB}) and it can be approximated in the Eq. (4).

$$V_{th\text{-}opt} = V_{th0} - k_2 V_{BB} \tag{4}$$

Where, V_{th0} is the threshold voltage with the zero body bias, and k_2 is a coefficient of the back gate bias [11].

The maximum operating frequency (f_{max}) for the optimal supply voltage is proportional to the reciprocal of the Delay, as given in the Eq. (5).

$$f_{\max} = \frac{1}{k_3} \frac{(V_{dd\text{-}opt} - V_{th\text{-}opt})^{\alpha}}{V_{dd\text{-}opt}} \tag{5}$$

Where k_3 is are fitting coefficients.

These equations are crucial, it provide the combination of $V_{th\text{-}opt}$, $V_{dd\text{-}opt}$ and maximum possible clock f_{max} yielding an efficient optimal power design.

3 Adaptive supply and body voltage controller design

The $V_{dd\text{-}opt}$ and $V_{th\text{-}opt}$ relations are found theoretically in the previous section of a MOSFET transistor. Therefore, it is necessary to design adaptive supply and body bias voltages to control microprocessor's temperature and power dissipation. Body biasing is effective in taking advantage of the body effect of MOS transistors to modulate and adjust supply and threshold concurrently to be operate whenever the processor reaches a certain temperature or average power consumed under dynamic computational workloads.

The controller built on a temperature sensor and threshold voltage monitor to monitor and sense the variation of chip temperatures that can be placed at the hottest environment to detect the average hotspot of the chip. The configuration of the temperature sensor/leakage current monitor, Threshold extractor, and saturation voltage (V_{sat}) extractor is shown in Fig. 1.

The temperature sensor generates two output voltages V_A and V_B for monitoring the relative contribution of the subthreshold current (I_{SUB}) and band-to-band current (I_{BTBT}) to determine optimal value of body bias voltage. The body bias voltage for which the total leakage is minimized occurs when ($\delta I_{eak}/\delta V_{BB} = 0$),

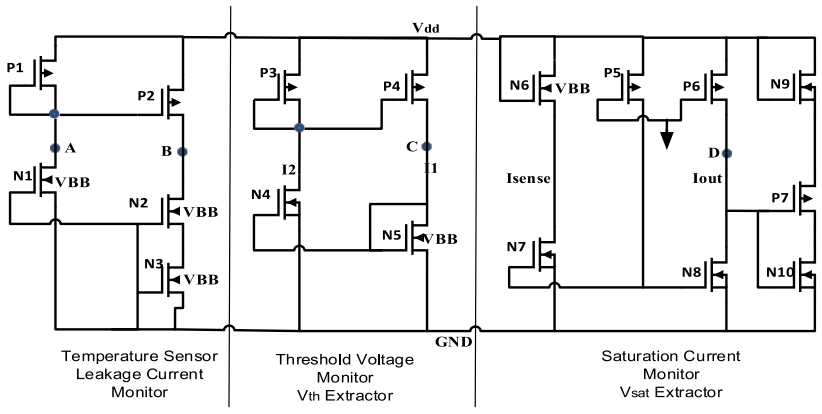

Fig. 1. Temperature sensor/leakage current monitor, Threshold extractor, and saturation voltage (V_{sat}) extractor

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therefore for the same technology dependence constants at the same body bias voltage, the condition of optimal minimum leakage current and dissipated power is ($I_{SUB} = I_{BTBT}$).

The output voltage of the threshold voltage monitor (V_C) carries the temperature information of N5. This circuit requires two n-channel transistors N4 and N5 with different threshold voltages based on the V_{BB} injection, and two p-channel transistors P3 and P4 with modestly equal threshold voltages. Therefore, n-channel transistor has a higher threshold voltage than the p-channel transistors. The threshold extractor working based on a current-voltage relationship valid for any operating condition.

For saturation current sensor; transistors N6 is in saturation. So when a small current from the sensor flows, the current is mirrored into the N7 and N8. P5 supply a sufficient bias current to keep N7 and N8 in saturation. The output voltage V_D is the saturated voltage equal to V_{dd} minus the voltage drop across drain and source of transistor P6. The complete block diagram of the adaptive supply and body voltage controller is shown in Fig. 2.

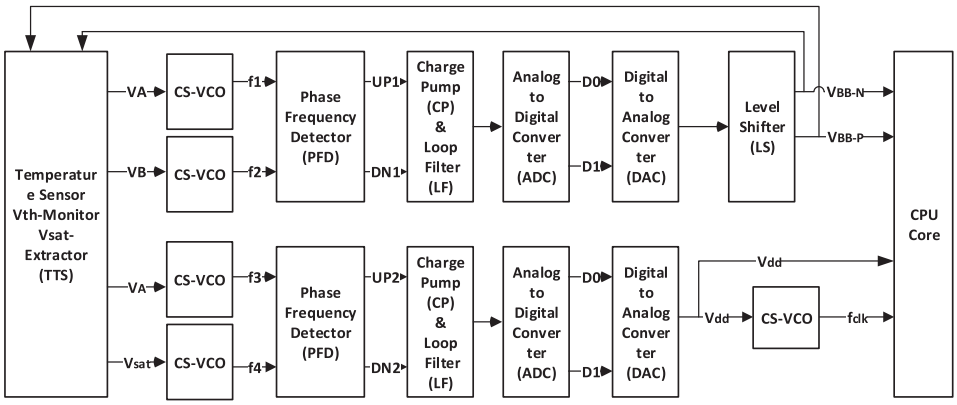

Fig. 2. The complete block diagram of the adaptive supply and body voltage controller

The temperature sensor, V_{th} Extractor and V_{sat} extractor circuit is monitoring the relative contribution of the leakage current and generates optimal body bias voltage by adjusting this value according to the saturated voltage. The temperature sensor is monitoring the relative contribution of the leakage current and generates optimal body bias voltage by adjusting this value according to the saturated voltage.

To make the controller system operate with accurate response of V_A, V_B, and V_D variations, these voltages are converted to high frequencies using current starved oscillator (CS-VCO) because the generated frequencies are in great relation with the sensor voltages. The 9-stages CS-VCO are required to generate 2 GHz oscillation frequency at the control voltage of approximately Vdd. Fig. 3 shows a CS-VCO circuit.

The frequency detector (FD) detects any difference between the two input signals f_1 and f_2, and generates two control signals UP and DN to the charge pump to modulate the amount of charge stored in the low pass filter. If the frequency of

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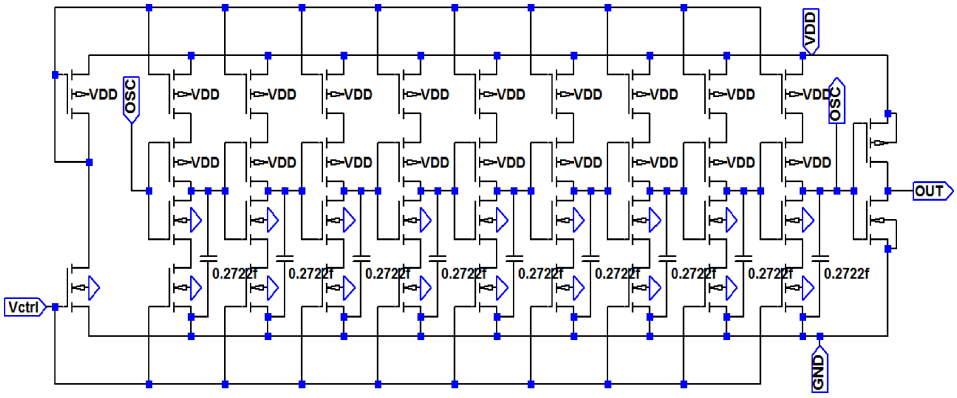

Fig. 3. The circuit diagram of 9-stage CS-VCO

f_2 is less than f_1, the FD produces positive pulses at UP, while DN remains at zero. Conversely, if the frequency at input f_2 is higher than f_1, the FD produces pulses at DN and UP remains at zero. If both frequencies are equal, then either the circuit generates pulses at UP or DN with a width equal to the phase difference between the two frequencies. Thus, the average value of UP and DN is an indication of the frequency difference between f_1 and f_2. The charge pump (CP) is used to sink and source current into the loop filter (LF) based on the output of the FD, it serves to convert the two digital output signals UP and DN of the FD into analog signal as charge flows, whose quantity is proportional to the frequency difference. The schematic diagram of the FD is shown in Fig. 4.

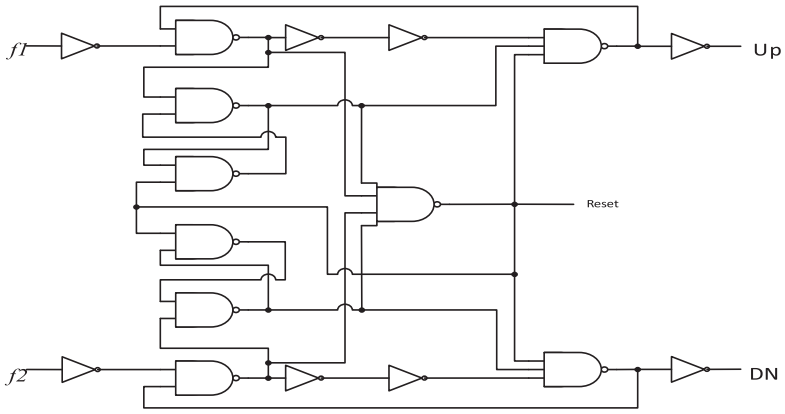

Fig. 4. The Schematic diagram of the FD circuit

A passive filters shape the output current signal of the charge pump to suppress the useless messages buried in that signal. The CP supplies a current to the LF that changes to a voltage by the LF. The task of CP is to charge and discharge the LF capacitor. Thus, the LF output signal will increase and decrease according to the switches activity in the CP, which affected by the outputs of FD. A second-order filter is used since; it is stable for any value of loop gain, and the maximum phase shift is −180°. The proposed LF is shown in Fig. 5.

To stabilize the body-bias and supply voltages, digitalize the LF output into four possible value is proposed using a 2-bit analog to digital converter (ADC) in conjunction with the 2-bit digital to analog converter (DAC). The flash (parallel) ADC is known for its fastest speed compared to other ADC architectures. There-

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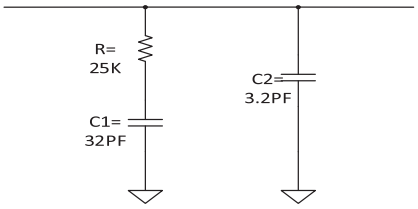

Fig. 5. The circuit diagram of the loop filter

fore, it is used for high-speed applications such as digital systems and integrated circuit designs with small device sizes that reduce parasitic capacitances and provide acceptable accuracy. The digital to analog converter (DAC) is a crucial building block in the loop. The output digital pulses of ADC, Do, and D1 became inputs for DAC, Which convert these digital pulses to a stable analogue voltage; consequently, this block will generate four voltage levels of voltages. The produced voltage by DAC is the desired reverse body bias voltage and supply voltage for the microprocessor.

The adaptive loop relies on controlling both PMOS and NMOS body terminals. Because this is essentially a two dimensional control problem, there exists an infinite number of $V_{BB\text{-}N}$ and $V_{BB\text{-}P}$ values that will still satisfy the performance through the matched supply voltage V_{dd}. For generating entire voltage, level shifters were designed and implemented to allow chip core signals $V_{BB\text{-}N}$, $V_{BB\text{-}p}$ using a single power supply. It t can shift any voltage level signal to a desired higher level for different voltage domains. The circuit diagram of The ADC and DAC is shown in Fig. 6 and Fig. 7 respectively. The level shifter circuit diagram is shown in Fig. 8.

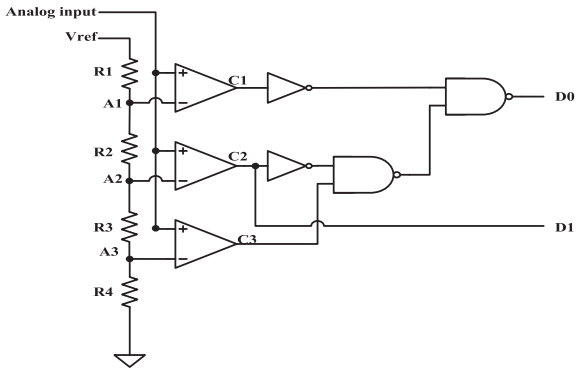

Fig. 6. The circuit diagram of the ADC circuit

For the proposed scaling loop, The NMOS body bias voltage, $V_{BBN\text{-}N}$, is generated from the output of the DAC for different reverse body bias domain. Thus, generate $V_{BB\text{-}P}$ is a very essential for different reverse body bias domain. The design employed using a single supply, multiple outputs level shifter (usually 4-outputs), with a data selector using an four-to-one (4-1) multiplexer that can be controlled through the digital bits Do, and D to determine the voltage domain set of $V_{BB\text{-}N}$ in conjunction with $V_{BB\text{-}P}$. The proposed single-supply level shifter is shown in Fig. 9 for generating $V_{BB\text{-}N}$ and $V_{BB\text{-}P}$.

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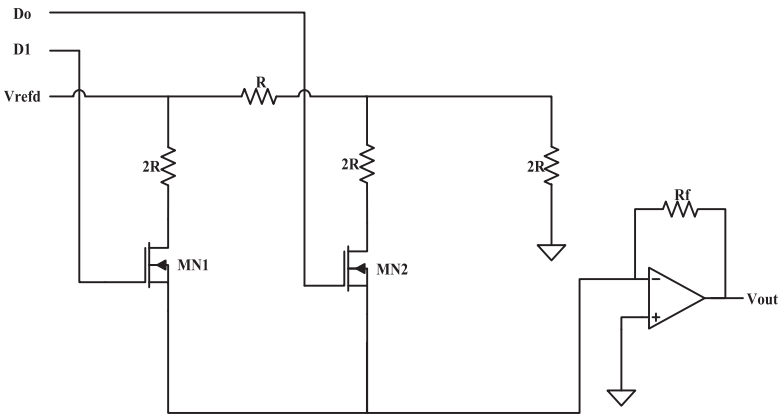

Fig. 7. The circuit diagram of the DAC circuit

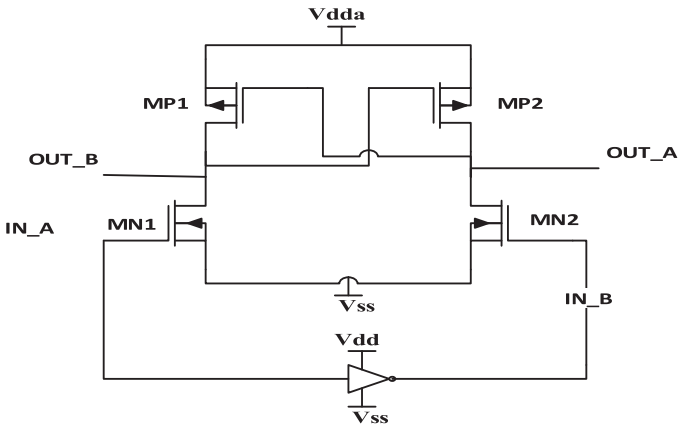

Fig. 8. The circuit diagram of the level shifter circuit

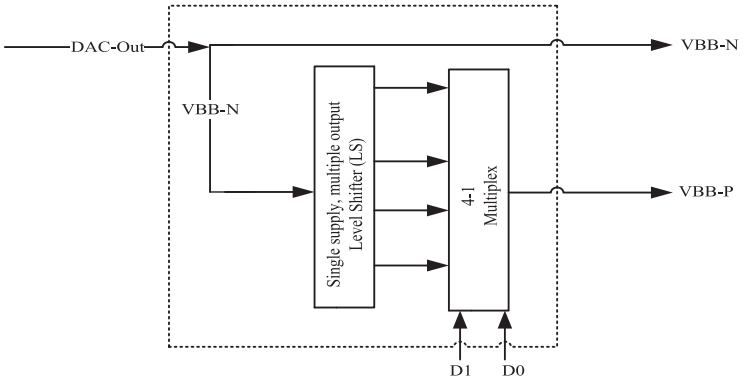

Fig. 9. The level shifter circuit with $V_{BB\text{-}N}$ and $V_{BB\text{-}P}$

Microprocessors have different ranges of temperature: idle, normal range, and maximum range, a two-bit ADC is required to generate four states in the output, 00, 01, 10, and 11, one state is for idle and normal temperature range, whereas the other three states are used for maximum temperature range, including three subranges. The digital pulses of ADC (D0 and D1) become inputs to DAC circuit, which converts the digital pulses to analogue voltage; consequently, four levels of voltages are generated depending on thermal status of the chip. The DAC analogue output voltage is the desired supply V_{dd}, body V_{BB} for the microprocessor core to

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minimize its temperatures, and dissipated power. The desired clock frequency (f_{clk}) is generated through a specific CS-VCO from $V_{dd\text{-}opt}$ as shown in Fig. 2.

4 Simulation results

All internal blocks of the complete block diagram of the adaptive supply and body voltage controller shown in Fig. 2 are designed using 22 nm Low Power Predictive Model (22 nm-LPTM) for different temperatures and simulated to generate optimal supply and body bias/threshold voltages ($V_{dd\text{-}opt}$ & $V_{th\text{-}opt}/V_{BB\text{-}opt}$) using specification of the Intel Core i7 microprocessor chip.

Fig. 10 and Fig. 11. Shows the temperature sensor voltages V_A-V_B and V_A-V_D for different body voltages and different temperatures.

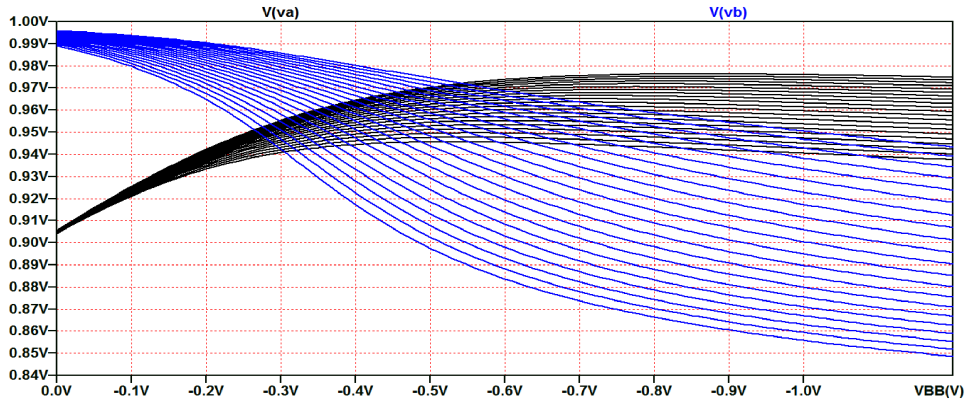

Fig. 10. The temperature sensor voltages V_A & V_B for different body voltages and different temperatures

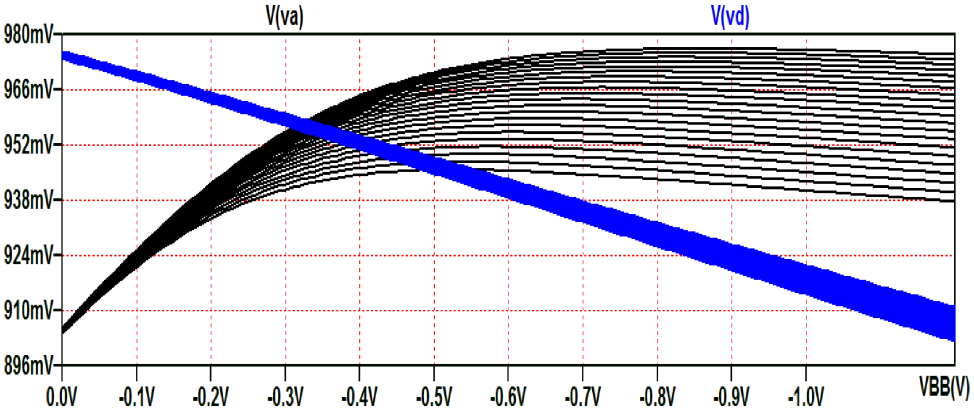

Fig. 11. The temperature sensor voltages V_A & V_D for different body voltages and different temperatures

The simulation results of the adaptive supply and body voltage controller are shown in Table I.

Table II shows the power dissipation/transistor for different temperatures, and Fig. 12. Shows the bias voltage and power dissipation per single transistor for different temperatures and V_{BB} to validate a strict limitation of power and temperatures.

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Table I. The simulation results of the adaptive supply and body voltage controller

V_{BB} (V) Optimal	Temp (°C)	V_A (V)	V_B (V)	V_{th} (V)	V_D (V)	V_{dd} (V) Optimal	f_{CLK} (GHz)
−0.539	66–80	0.966	0.966	0.376	2.855	1.200	1.623
−0.372	51–65	0.958	0.958	0.356	2.779	1.151	1.592
−0.235	35–50	0.953	0.953	0.341	2.704	1.149	1.556
0.0	>35	0.938	0.938	0.318	2.585	1.073	1.536

Table II. The power dissipation/transistor for different temperatures and V_{BB}

Temp (°C)	Power Dissipation (nW) Per Transistor	Temp (°C)	Power Dissipation (nW) Per Transistor
32°C	5.515	54°C	11.737
34°C	5.897	56°C	12.442
36°C	6.277	58°C	13.556
38°C	6.575	60°C	14.320
40°C	7.244	62°C	15.138
42°C	7.774	64°C	16.351
44°C	8.338	66°C	17.235
46°C	8.967	68°C	18.342
48°C	9.642	70°C	19.720
50°C	10.184	71°C	20.372
52°C	10.929	72°C	20.872

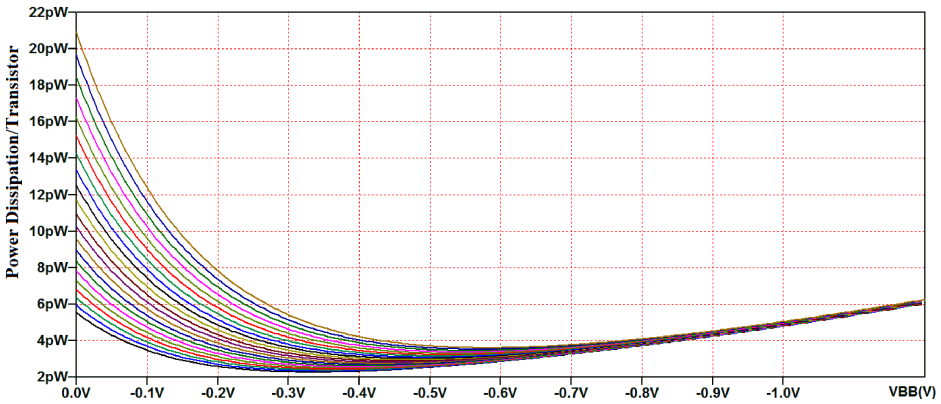

Fig. 12. Power dissipation/transistor for different temperatures and V_{BB}

The simulation results verifying that, during the dynamic computational workload/temperature periods, the processor have a low average power dissipation with adaptive V_{dd}-V_{th} and led to high performance estimation. These results verify adaptive V_{dd}-V_{th} for power-temperature aware to the processor designers in their verification efforts because of the parallel nature of workloads and active/idle states of portable processors.

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5 Conclusion

High performance processors are the chief demands driving today's electronic designs. This leads to exponential increase of power densities across process generations and results in higher die temperatures and even higher temperatures of today's microprocessor chips. Therefore, reduction of microprocessor's power and temperature has been dominant consideration in digital system design. Adaptive V_{BB}/V_{th} technique has emerged as an effective way to achieve optimal energy consumption as well as low temperature designs.

This study has provided an optimal power/temperature solution; the controller has been designed and tested with different simulation environments, and for different temperatures, which were categorized into four possible levels. The obtained results have shown significant improvements of both power and temperature. Power saving was obtained up to (20%), and the thermal reduction was in the range of (8C°) for each body bias step voltage. These results confirm an optimal improvement in power and temperatures compared to previous works.

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