Thermal Impact on the Power Device Behaviour: Application on the IGBT

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***Abstract*—The functional limits of an IGBT are defined by an essential parameter: the maximum junction temperature permitted. The technical specifications of each IGBT type provide the limit values of the functional temperature for example, from -55°C to 150°C. The electrical energy dissipated by the IGBT for any current direction, appears in form of thermal energy at the junctions level. But we should bear in mind that the ambient temperature represents an energetic level through which is insured the raise of the junction temperature.**

***Index Terms*—punch-trough IGBT, high frequency, temperature of junction, tailing current.**

I. INTRODUCTION

The Insulated Gate Bipolar Transistor (IGBT) is a MOS controlled bipolar transistor structure. The IGBT offers excellent performances in terms of conduction characteristics and gate drive requirements, as they basically behave as BJTs with the ease of drive of power MOSFETs.
Its low on-state voltage drop and relatively high switching speed are obtained by the injection of minority carriers into the drift region which induces a reduction of its resistance during on-state current conduction. The prediction of the stresses arising from the heating conditions represents a challenging issue, among the tasks of the power converter designers, since a heating can lead to the failure of the devices. Since high temperature forming in the device junction interacts with latch-up and avalanche induced second breakdown phenomena, a regenerative mechanism, lead to the destruction of the device.
Recently, the demand for high voltage and high power IGBTs has been increasing in order to achieve a device structure with high voltage blocking capability in the 1200V range with the NPT type IGBT and in the 600 V range are mainly PT type.
Since ten years, several works were carried out on the mechanisms of degradation by thermo-mechanical constraints and the consequence of these constraints on the measurable thermal and electric parameters. The tests are related preferentially to active cycling, i.e. by self-heating. The thermal cycling is practiced by the component makers in small case (TO220/247, ISOTOP), such as those currently practiced by the ST Microelectronics. Today, there are several studies in progress on certain aspects of the reliability of the IGBT. This work gave birth to publications showing that, according to conditions of appearance of short-circuit (temperature, current, tension), it exists a certain critical energy beyond which the number of shorts-circuit acceptable by the component is very limited.
Other studies were undertaken on problems of ageing of the component applied by the component makers. These tests are: High Temperature Transfers Bias requesting the silicon part of the component, High Temperature Gate Bias requesting gate oxide, and finally of the tests of thermal tiredness requesting the assembly of the components, [5].

In all the demonstrations, we have used a punch-trough (PT) IGBT, because the stored charge in PT devices is more temperature sensitive than in NPT devices. Power devices operate within a large temperature range. For that reason, it is important to understand the relationship between the device temperature and its electrical characteristics [1].

This paper offers a new explanation on the temperature effect on the device performance. Our calculation using the two-dimensional device simulator shows that the leakage current through the IGBT is one of the dominant causes of losses in function of the temperature.

In any particular situation, the reliability of a power semiconductor is affected by the junction temperature Tj; during its operating life. Note that the forward and off-state blocking capability of the device determines the maximum junction temperature *Tjmax*. Maximum blocking voltage and leakage current ratings are established at elevated temperatures near to the maximum junction temperature. Therefore, operation in excess of these limits may result in unreliable operation of the IGBT.

II. IMPORTANT THERMAL NOTES

At normal temperatures, in an extrinsic semiconductor, electrons are excited from donor levels to the conduction band or from the valence band to the acceptor levels by a relatively small amount of energy. As a temperature increases, the donor levels become exhausted, or the acceptor levels saturated. As the temperature increases even more, the electrons become excited from the valence band to the conduction band in large numbers by now abundant thermal energy.

At low intermediate temperatures, the conduction electrons are the majority carriers. The beginning of the intrinsic conduction is linked to the energy gap *Eg* which is equal to 1.1 eV for silicon semiconductor, at approximately 200°C. This temperature is the maximum limit at which the

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semiconductor can work. By approaching this temperature, the device's operating properties start to degrade. Actually several silicon components are characterised for the maximum junction temperature, *Tj* =150 °C.

We notice that the junction temperature is usually many degrees higher than the case and ambient temperature. When we understand the effect of the temperature on the life of product, we can arrive at a compromise between cost and life. Thus we can increase the competitiveness upon the cost of the device [2].

The semiconductor manufacturer specifies the junction-to-case thermal resistance *Rjc* and the maximum junction temperature *Tjmax*. The case-to-heat sink thermal resistance *Rch* is also specified.

We have also to note that the maximum storage temperature Ts is very superior to the maximum operating temperature. Maximum storage temperature is restricted by material limits defined not so much by the silicon but by peripheral materials .The forward and Off-State blocking capability of the device determines the maximum junction temperature. The establishment of leakage current and maximum blocking voltage ratings are realised when the temperature is increased.

III. PUNCH-TROUGH STRUCTURE DEVICE

A punch-trough IGBT has an N+ buffer layer between the P+ substrate and N- drift region; figure 1.The N+ buffer layer improves turn-off speed by reducing the minority carrier injection quantity and by raising the recombination rate during the switching transition.

Too, in a transistor Punch-Through IGBT, the region of depletion reached a buffer zone strongly doped N^+ in which the electric field decrease quickly high dE/dt. It does not reach visibly the region of collector. The electric field has overall a trapezoidal pace. Neglecting the electrical field portion in the buffer layer ($N_d >> N_D$) the relation binding the electric field maximum E_0 to the supply voltage V_{in} is [11].

$$V_{in} = W_b \cdot E_O - \frac{q \cdot N_D \cdot W_b^2}{2\varepsilon} + \sqrt{\frac{8 \cdot \varepsilon}{9 \cdot q \cdot k}} \left(|E_O|\right)^{1,5} \quad (1)$$

Where: W_b is the width of the base.

In addition, latch-up characteristics are also improved by reducing the current gain of the PNP transistor [2] [3].

For same behaviour in terms of direct voltage, and with an asymmetrical diffusion structure, it is possible to reduce the commutation losses for devices of the same velocity.

It is also possible to realise faster IGBT without leading to unacceptable losses. This structure presents an acceptable compromise between the different major electrical parameters: time of extinction, high frequency commutation losses, and the behaviour in terms of direct voltage.

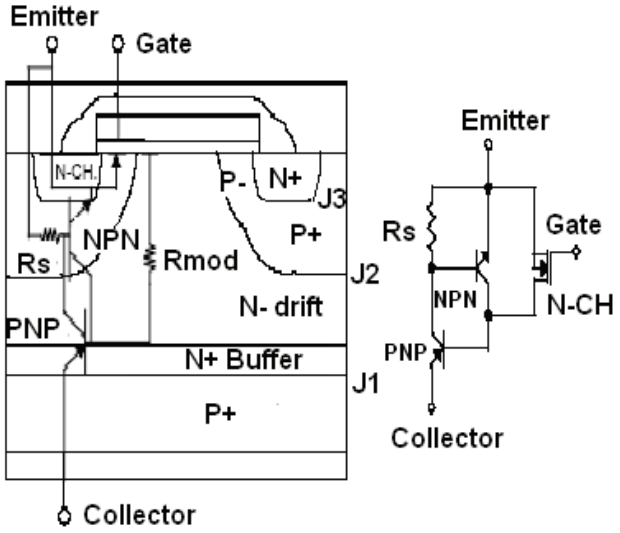

Figure 1. IGBT punch-trough structure.

IV. TEST CIRCUIT

A semiconductor switch for circuit may be used for other aims different from that of switching the circuit on and off at many moment. If the switches cyclically triggered and quented at a special switching frequency, the power drawn by a load from a direct voltage source can be controlled. **DC** power controllers perform the basic function of **dc-dc** conversion.

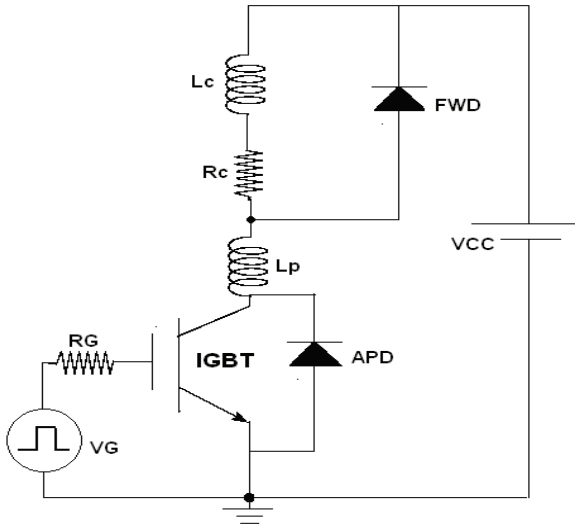

Figure 2. Test circuit.

V. RESULTS AND DISCUSSION

Figure 3 shows the voltage across the IGBT for variable junction temperatures *Tj*. *Tj*=150 °C is chosen as the design maximum value, because above this value the current begins to increase rapidly, causing by this way the degradation of the voltage rating. The IGBT becomes very sensitive to over-voltage transients, as well as to high dv/dt, and di/dt. In the case of the forward blocking junction there is an increasing possibility of forward recover triggering [5].

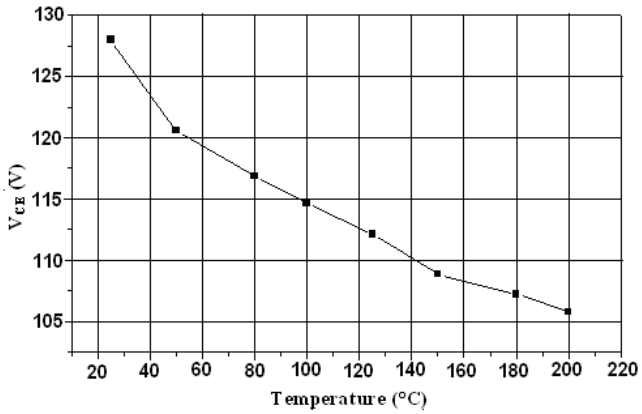

Figure 3. V_{CE} versus temperature.

According to the waveform, we notice that up to given temperature value, the voltage across the device rapidly decreases to become very poor above some values. We can say that above of the operating temperature there will be a very important thermal agitation created by the excessive behaviour of the carrier causing an excessive heating then an eventual destruction.

Operating at low temperature is not harmful, but we should allow it be for increased gate trigger current, latching current and holding current as well as slow turn-on. So operating in the range between ambient temperature and 150°C gives the best compromise between the quality and the operational life [8].

Figure 4 shows the characteristic in direct conduction system for different temperatures (*Tj*= 25°C, 100°C and 150°C).

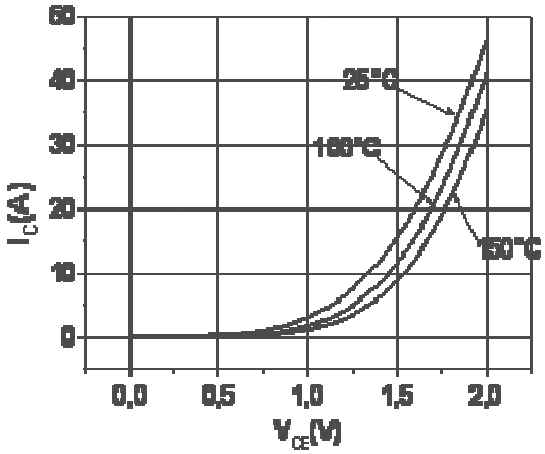

Figure 4. Current vs. Voltage (Tj =25 °C 100 °C and 150 °C)

We notice that the voltage V_{CE} is relatively reduced for the less high temperatures, while the current does not stop growing. Starting from a given point the voltage V_{CE} is reduced for the strong temperatures while the collector current I_C increases quickly to reach rather high values, figure 5 illustrates this fact for *Tj* = 22 °C, 100 °C, 150 °C.

This behaviour leads to losses of energy, increasing by this way the heating of the device and limiting consequently its possibilities of conduction for a given temperature.

During the conduction of the IGBT, a portion of its current flows via the effective MOSFET, at the time where the rest of this current flows through the PNP transistor.

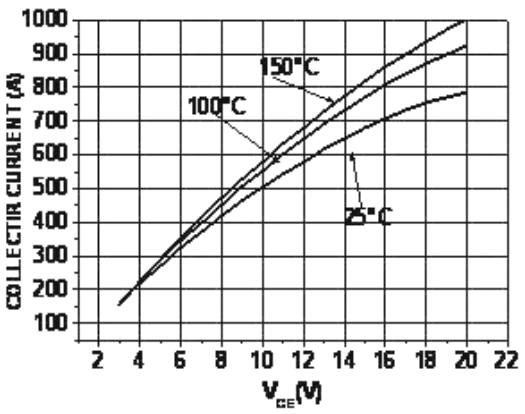

Figure 5. Increasing collector current for high temperatures.

During the turn-off transition, the MOSFET turn-off is very fast, and thus its on-state current is quickly stopped. Therefore, the PNP current follows its flow till the recombination of the stored minority charge in the N-region.

The decreasing rate of the tail current that follows depends on the carrier lifetime in the IGBT base and the reverse injection efficiency of the anode-base junction. According the dynamic behaviour, the total turn-off loss can be approximated by:

$$E_{OFF} = \frac{1}{2} \cdot I_C \cdot V_C \left(t_{vr} + t_{if} \right) + V_C \cdot \left(\frac{t_{if} \cdot I_{tail}}{2} + Q_{tail} \right) \text{J} \quad (2)$$

Figure 6, shows the variation of the tailing current.

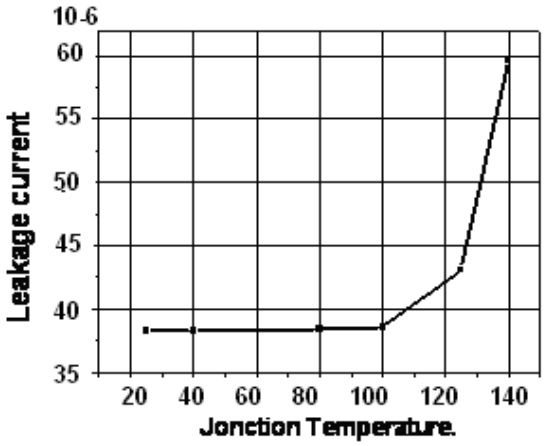

Figure 6. Tailing current at different temperatures.

We have seen that when the device is enough doped, the recombination mechanism of electron hole pairs determines the recovery time in volume. We can say then that recovery charge and the recovery time depend greatly on the junction temperature where its effects are also important on a localised basis. Thus, if the IGBT is accidentally switched on before recovery, this self-switching will occur near the gate where the localised temperatures are higher than in the surrounding regions.

We can say that it also depends on the temperature and on gate bias during the turn-off interval [6]. To obtain an

optimised turn-off, we must reduce the lifetime in layer N^-.

The short duration tail current is typical of a PT-IGBT with lifetime control processing. Optimization of the lifetime control also allowed the reduction of the turnoff d*i*/d*t* to prevent the severe transient voltages typical of many NPT designs [9]. The N+ buffer layer is necessary to secure a sufficiently high breakdown voltage and low leakage current in the presence of an optimally thin drift region.

To achieve low switching losses in a PT-IGBT, you must accelerate the rate of recombination of charge (carrier lifetime) in the buffer layer. Recombination sites in the buffer layer, which yields increased turnoff speed and lower tail current losses. The recombination rate is temperature dependent increasing switching losses at elevated temperatures [10].

In some applications the device is protected by fuse. In this case, if the current is interrupted by this latter, little or no reverse voltage appears across the device. Then, very high reverse recovery power dissipation can result from the reapplication of voltage if temperature is higher. Some overloads require that the device survives with forward voltage being reapplied [7].

At the time of the switch-on process, the conduction area is reduced to a portion of the emitter nearly the command electrode [4]. If the exterior circuit imposes a fast intensity increase during this phase, the current density across the switched-on surface may reach an important value.

Moreover, the power decrease at the device bounds, at the time of the passage from the blocking state of the condition state, does not happen instantaneously. However, there will be a simultaneous presence of the current and the voltage.

Through these two parameters the instantaneous power can reach very high value. The dissipated energy in a poor volume begets then a considerable heating. When the critical thermal limit is reached, this heating will destroy by the silicon fusion the conductor area, it is the destruction by d*i*/d*t*. Figure 7 shows the evolution of this power at different temperatures (*Tj*= 25 °C, 100 °C and 150 °C). There are other important temperatures among which the temperatures under *Tjmax* where ion migration on the silicon surface under passivation an expected degradation, or the continuous temperature tolerated before thermal runaway occurs.

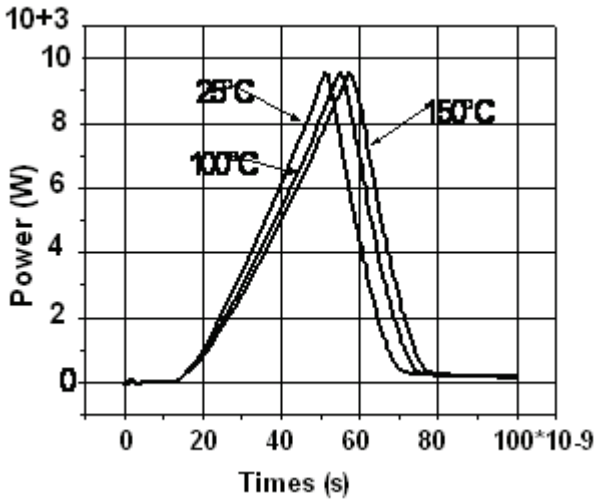

Figure 7. Evolution of power at variable temperatures

VI. CONCLUSIONS

Actually, in this research phase realised on the optimisation on the power devices, we are oriented towards the realisation of structures which are capable of switching at very high frequencies that the ones allowed by the first generation. The new structures of the actual generations have allowed having much more poor switching losses, by trying to reduce mainly the ones caused by the relative increase slowness of the residual parasitic current.

These new asymmetrical structures with reference to the conventional ones, will accept at the time of the current turn-off, that the voltage would be reapplied at their bounds without an allowed time, as soon as the current is interrupted.

Calculation of temperature rise for short pulses needs more complex analysis, possibly involving finite element analysis techniques. Device turn-on behaviour and its dependency on voltage, temperature, d*i*/d*t* and gate drive has to be taken into account. If the semiconductor junction is over 230 °C, the operation properties begin to degrade. Many silicon semiconductors on today's market are characterised for the maximum junction temperature, *Tj*=125 °C. A few go as high as 170 °C.

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