Investigation on Fuzzy Logic Based Centralized Control in Four-Port SEPIC/ZETA Bidirectional Converter for Photovoltaic Applications

Mahendran VENMATHI, Ramabadran RAMAPRABHA
Department of Electrical and Electronics Engineering, SSN College of Engineering, 603 110, India
venmathim@ssn.edu.in

***Abstract*—In this paper, a new four-port DC-DC converter topology is proposed to interface renewable energy sources and the load along with the energy storage device. The proposed four-port SEPIC/ZETA bidirectional converter (FP-SEPIC/ZETA BDC) converter comprises an isolated output port with two unidirectional and one bidirectional input ports. This converter topology is obtained by the fusion of SEPIC/ZETA BDC and full-bridge converter. This converter topology ensures the non-reversal of output voltage hence it is preferred mostly for battery charging applications. In this work, photovoltaic (PV) source is considered and the power balance in the system is achieved by means of distributed maximum power point tracking (DMPPT) in the PV ports. The centralized controller is implemented using fuzzy logic controller (FLC) and the performance is compared with conventional proportional integral (PI) controller. The results offer useful information to obtain the desired output under line and load regulations. Experimental results are also provided to validate the simulation results.**

Index Terms—bidirectional power flow, DC−DC power converters, fuzzy control, photovoltaic systems, pi control.

I. Introduction

Nowadays most of the power is generated from the renewable energy sources like photovoltaic system, fuel cell, biomass, wind etc. The energy produced from the renewable energy sources are unpredictable and time varying. But the loads require constant input power supply under all atmospheric conditions. In order to supply the load smoothly without any interruption, energy storage devices like batteries or super capacitors are utilized. By integrating the PV ports and the storage device with the load, multiport converter is used in many applications [1-3]. Depending upon the applications the ports in the converter are treated as bidirectional or unidirectional.

Considering the advantages like less number of components, less conversion steps, etc., the multiport converters are preferred to the conventional two-port converter [4-5]. Multiport converter can be built by using different types of topologies like fully isolated topology, partially isolated topology, and non-isolated topology. Also, different types of DC-DC converters are used to realize the multiport converter [6-8].

In this work, the partially isolated topology is considered in which the input ports are isolated from the output port using high frequency isolation transformer. The proposed converter topology can interface four ports, viz., two PV ports as unidirectional input ports, a battery as bidirectional port, and the load as output port. FLC is implemented to provide individual control as well as overall control of the system. The FLC based centralized controller provides easy control over various operating conditions and the performance of the system could also be improved when compared with the conventional centralized PI controller. To extract maximum power from PV ports, DMPPT algorithm is used [9-10]. The proposed converter provides high voltage gain under different operating modes with reduced ripple current in the voltage obtained on the output port. The detailed analysis of the FP-SEPIC/ZETA BDC is presented in the following sections.

II. Analysis Of FP-SEPIC/ZETA Bidirectional Converter

The switching legs in the full-bridge converter and the SEPIC/ZETA BDC are capable of generating the square wave output voltage [11]. Fig. 1 shows the SEPIC/ZETA BDC consisting of two power devices in one switching leg. The proposed four-port converter has been derived by integrating the two SEPIC/ZETA BDCs with the full-bridge converter.

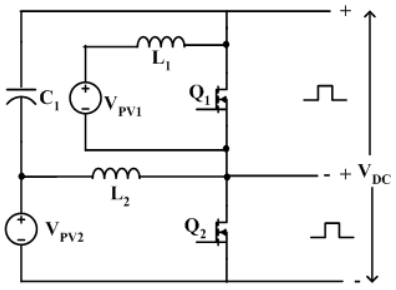

Figure 1. Schematic diagram of SEPIC/ZETA BDC

Fig. 2 shows the derived FP-SEPIC/ZETA converter topology connecting PV array, battery and the load. The power devices Q_3, Q_4 and the passive elements L_2, L_4, C_1 constitute the components of the ZETA converter by which the source PV1 is interfaced with the battery. The power devices Q_1, Q_2 and the passive elements L_1, L_3, C_2 constitute the SEPIC converter by which the source PV2 is interfaced with the battery. The SEPIC/ZETA converter is promising with the view point of producing the non-inverted output voltage with reduced ripple current in the output port. The output voltage has reduced settling time, rise time and increased step-up and step-down voltage gains. The conversion ratio of the SEPIC/ZETA BDC is expressed as

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$$V_b = \frac{V_{PV1} D_{PV1}}{1 - D_{PV1}} = \frac{V_{PV2} D_{PV2}}{1 - D_{PV2}} \quad (1)$$

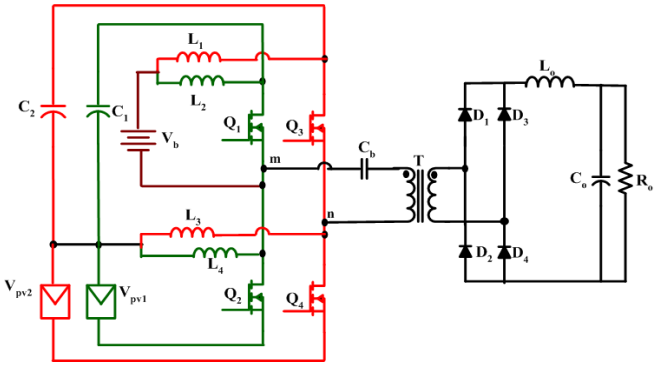


Figure 2. Configuration of FP-SEPIC/ZETA BDC

The D_{PV1} and D_{PV2} correspond to the duty cycle under various modes of operation, and it is used for power management in the system. The operating key waveforms of the proposed converter are given in Fig. 3. Each switching cycle comprises six switching states and the corresponding equivalent circuits are shown in Fig. 4.

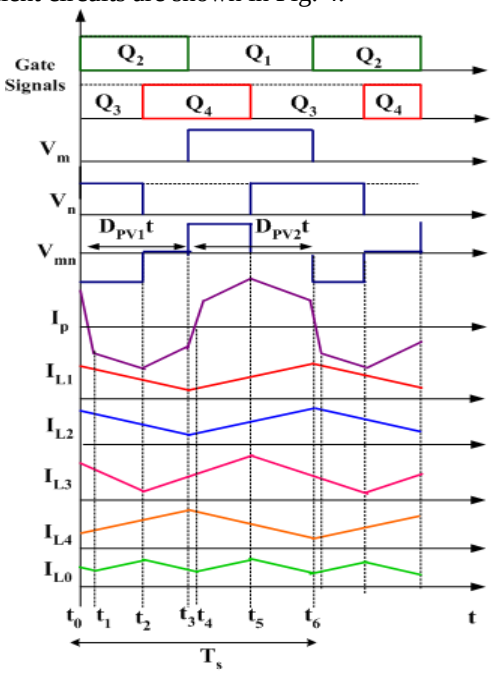


Figure 3. Operating key waveforms

State 1 [$t_1 \le t \le t_0$]: The condition of the power devices during this state is shown in Fig. 4 (a). The inductor L_4 charges, whereas L_1, L_2 and L_3 discharge. The negative voltage is applied across the transformer primary side. The diodes D_1-D_4 conduct and the filter inductor current i_{Lo} charges and freewheels through the rectifier diodes. The main equation governing the circuit in switching state 1 is:

$$\frac{dI_{L4}}{dt} = \frac{V_{PV1}}{L_4} \quad (2)$$

State 2 [$t_2 \le t \le t_1$]: The condition of the power devices during this state is shown in Fig. 4 (b), which is similar to switching state 1, but the diodes D_2 and D_3 are forward biased. The transformer is supplied with the negative voltage. The main equations governing the circuit in switching state 2 are:

$$\frac{dI_{L1}}{dt} = \frac{V_{PV1} - V_b}{L_1} \quad (3)$$

$$\frac{dI_{L2}}{dt} = \frac{V_{PV1} - V_b}{L_2} \quad (4)$$

$$\frac{dI_{L3}}{dt} = \frac{V_{PV1} - V_b}{L_3} \quad (5)$$

$$\frac{dI_{Lo}}{dt} = \frac{n\,[V_{PV1} + V_{PV2} + V_b] - V_o}{L_o} \quad (6)$$

State 3 [$t_3 \le t \le t_2$]: The schematic diagram of this state is shown in Fig. 4 (c), in which the inductors L_1 and L_2 discharge, whereas L_3 and L_4 charge. The diodes present in the full-bridge rectifier remains the same as those of the earlier state, and there is no voltage being applied to the transformer primary. The main equations governing the circuit in switching state 3 are:

$$\frac{dI_{L1}}{dt} = \frac{V_{PV1} + V_{PV2} - V_b}{L_1} \quad (7)$$

$$\frac{dI_{L2}}{dt} = \frac{V_{PV1} + V_{PV2} - V_b}{L_2} \quad (8)$$

$$\frac{dI_{L3}}{dt} = \frac{V_{PV1} + V_{PV2}}{L_3} \quad (9)$$

$$\frac{dI_{L4}}{dt} = \frac{V_{PV1} + V_{PV2}}{L_4} \quad (10)$$

State 4 [$t_4 \le t \le t_3$]: The schematic diagram of this state is shown in Fig. 4 (d), in which the rising edge of the current is experienced in the three inductors L_1, L_2, L_3 and the falling edge in the inductor L_4. The transformer primary side is provided with the positive voltage. The current i_{Lo} freewheels through the diodes D_1–D_4, thereby short circuiting the transformer secondary side. The main equation governing the circuit in switching state 4 is:

$$\frac{dI_{L4}}{dt} = \frac{V_{PV1} + V_{PV2} - V_b}{L_4} \quad (11)$$

State 5 [$t_5 \le t \le t_4$]: The condition of the power devices during this state is shown in Fig. 4 (e). The inductor current during this state remains the same as that of state 4. But positive voltage is applied to the primary of the transformer. The diodes D_2 and D_3 are reverse biased. Hence the filter inductor current flows through the remaining diodes. The main equations governing the circuit in switching state 5 are:

$$\frac{dI_{L3}}{dt} = \frac{V_{PV1} + V_{PV2} - V_b}{L_3} \quad (12)$$

$$\frac{dI_{L4}}{dt} = \frac{V_{PV1} + V_{PV2} - V_b}{L_4} \quad (13)$$

$$\frac{dI_{L1}}{dt} = \frac{V_{PV1} + V_{PV2}}{L_1} \quad (14)$$

$$\frac{dI_{L2}}{dt} = \frac{V_{PV1} + V_{PV2}}{L_2} \quad (15)$$

$$\frac{dI_{Lo}}{dt} = \frac{V_b - V_{PV1} - V_{PV2} - V_o}{L_o} \quad (16)$$

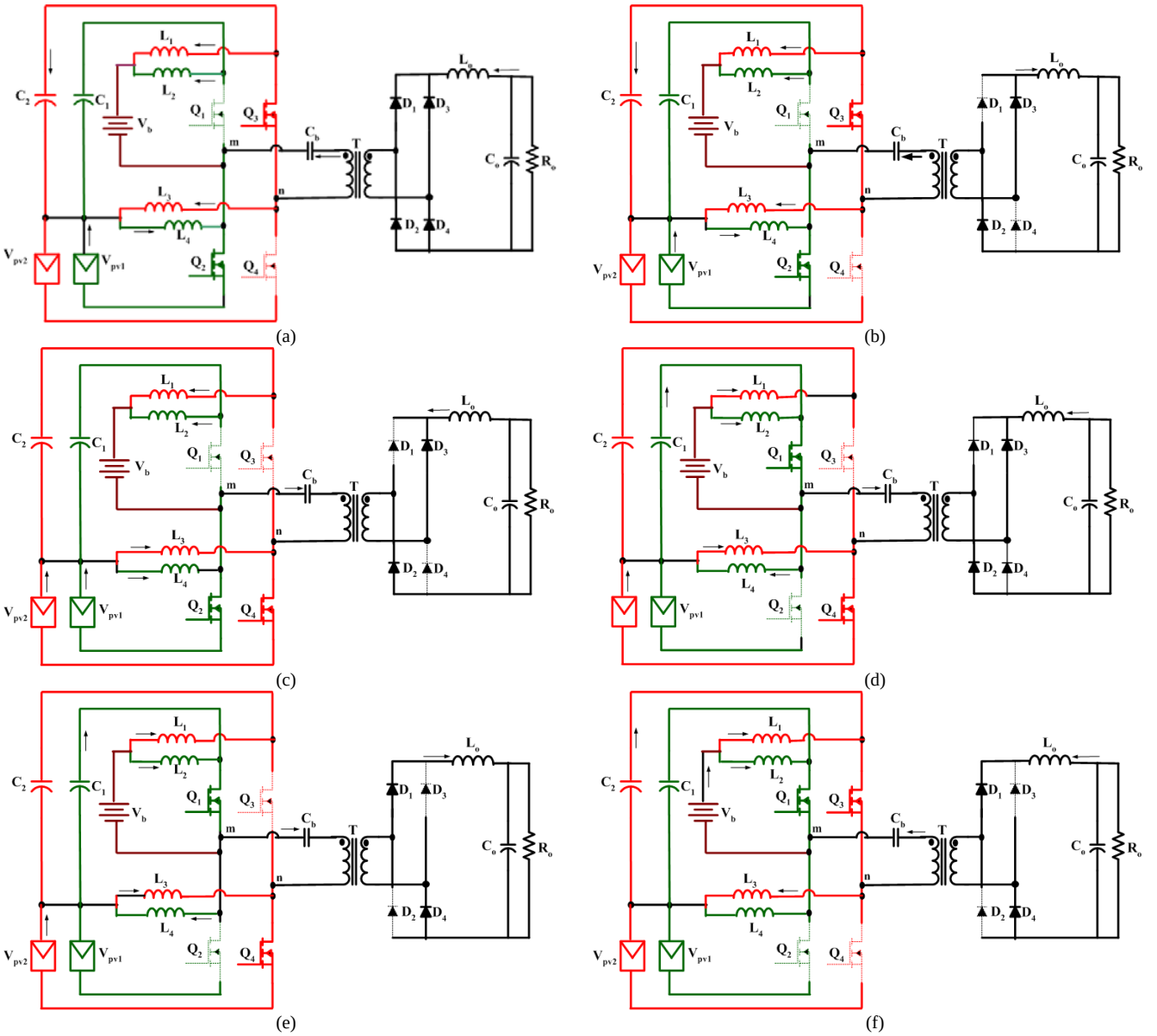


Figure 4. Equivalent circuits under different switching states

State 6 [$t_6 \le t \le t_5$]: The schematic diagram of this state is shown in Fig. 4 (f). During this state no voltage is applied to the transformer primary side. The current i_{Lo} flows through the diodes D_1 and D_4.

III. Proposed Control Strategy and Pulse Width Modulation Scheme for Power Management

The control structure built for the FP-SEPIC/ZETA converter is shown in Fig. 5. It comprises input voltage regulators (IVR), output voltage regulator (OVR), battery voltage regulator (BVR) and the battery current regulator (BCR). These regulators are used to maintain power balance in the system [12-13]. Assuming the system to be lossless the power balance equation is given as

$$P_{PV1} + P_{PV2} + P_b = P_o \quad (17)$$

The control structure enables the power flow in the FP-SEPIC/ZETA converter in any one of the three ways, i.e., from PV ports to the battery port and load; from PV ports and battery to the load; from battery port to the load. Hence this has been termed as dual output (DO), dual input (DI), and single input and single output mode. In single input single output (SISO) mode the power produced by $P_{PV1} + P_{PV2} = 0$. But in dual output mode $P_{PV1} + P_{PV2} > P_o$, whereas in dual input mode $P_{PV1} + P_{PV2} < P_o$.

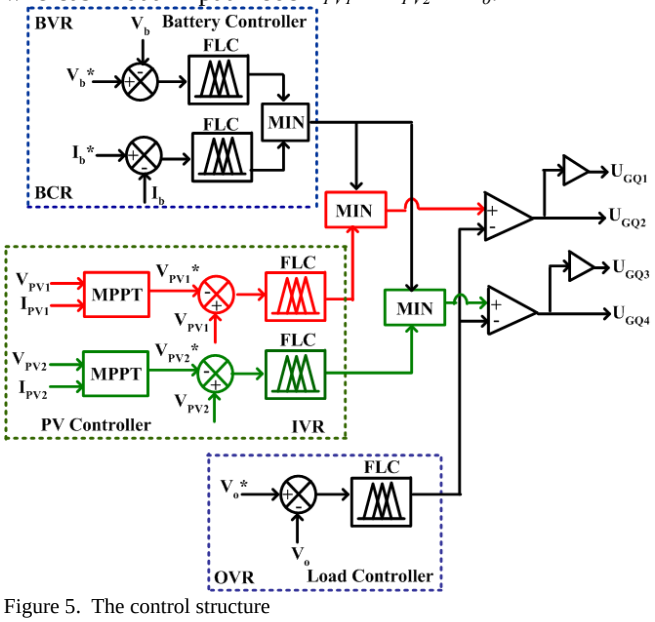


Figure 5. The control structure

A pulse width modulation (PWM) along with phase shift modulation (PSM) control strategy is used to control power flow in the multiport converter [14-15]. The phase angle and the duty cycle were the control variables used for simultaneous power management and to regulate the output voltage. Hence in the proposed control structure, BVR and BCR loops regulate the charging and discharging profile and the output voltage regulated using OVR loop. IVR regulates each panel voltage to the reference value using perturb and observe (P&O) algorithm [16-17]. The output voltage is designed, modeled and simulated to power the specific load of 100 V. In this study, all the control loops like IVR, OVR, BCR, and BVR are analyzed using FLC and the results are compared with those of the conventional PI controller [18-20]. The performance parameter analysis of the proposed converter have revealed that the parameters like steady state error and settling time of FLC are less compared with the values obtained using the centralized PI controller.

Fig. 6 shows the phase shifted pulse width modulation structure used for the proposed converter. In which the input ports are controlled by the control signals V_{DPV1} and V_{DPV2} and the output port by the control signal V_{C1}. The carrier voltages are indicated by V_{S1} and V_{S2}. As the DO and the DI modes involve three ports, there are three degrees of freedom. The three degrees of freedom includes the duty cycle D_{PV1}, D_{PV2} and the phase angle ϕ.

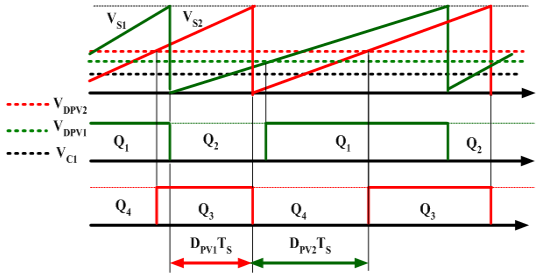


Figure 6. Pulse width modulation scheme

IV. Design of Fuzzy Logic Control

FLC gives solution to the non-linear system by means of mathematical principles and the interpretation of the experts. The FLC control algorithm depends on a linguistic control strategy, and derived from expert knowledge into an automatic control strategy. It is used to solve the complex problem using expert's knowledge by means of simple calculation. Thus fuzzy logic control may be viewed as a step towards an approach between the conventional, precise, mathematical control and human-like decision-making. However, at present there is no systematic procedure for the design of a fuzzy logic controller as in the case of the conventional PI controller. The FLC contains three different stages to process the system under control as shown in Fig. 7.

The actual values of all the control loops are compared at each sampled interval with their corresponding reference value to determine the error (e) and the change in error (Δe), which acts as the input to the FLC to produce the desired signal (u) [21-22]. The output signal (u) is the control action generated by FLC of each regulator. The stages of fuzzification, fuzzy inference, and defuzzification are performed for each loop using the algorithm described through the flowchart in Fig. 8. To simulate FLC, five triangular membership functions, namely *NS* (Negative small), *NL* (Negative Large), *ZE* (Zero), *PS* (Positive Small), and *PL* (Positive Large) are used for input variables and for the output variable. As the OVR loop is used to power the required load, only the membership function of the OVR loop is shown in Fig. 9. The rule base developed for OVR control loop is listed in Table I.

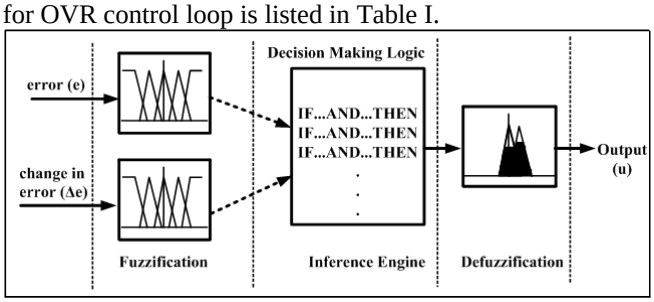


Figure 7. Schematic diagram of fuzzy control scheme

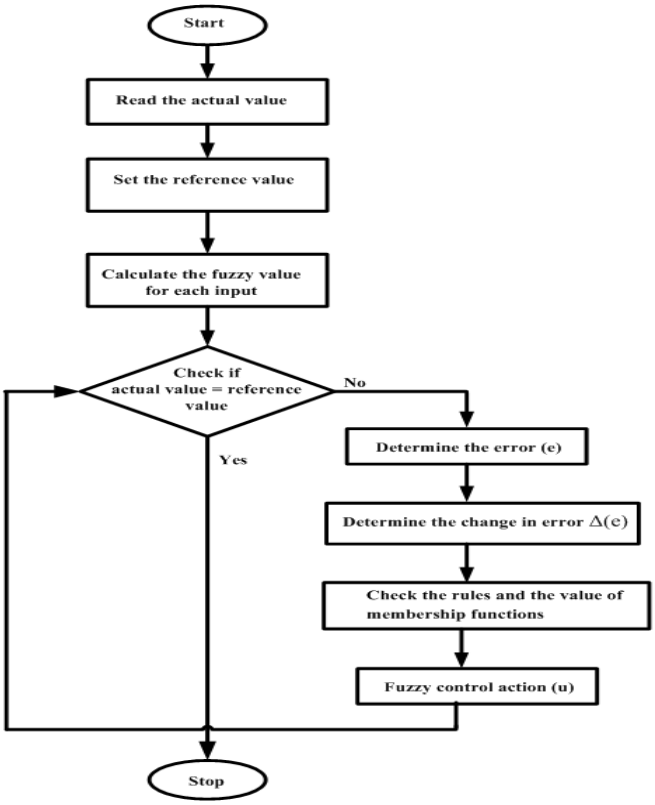


Figure 8. Flowchart for the FLC based control

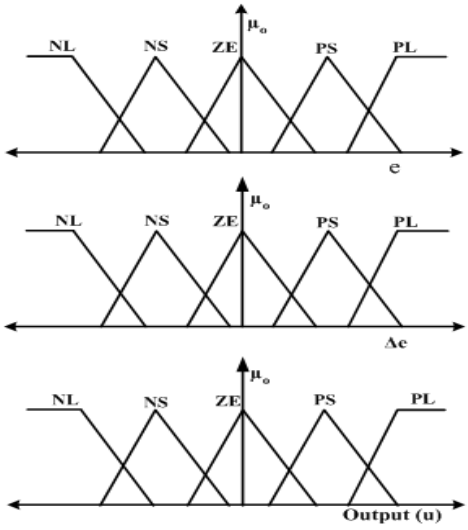


Figure 9. Membership functions of the input and the output variables of the FLC in the OVR loop

Table I. Fuzzy rule base for OVR loop

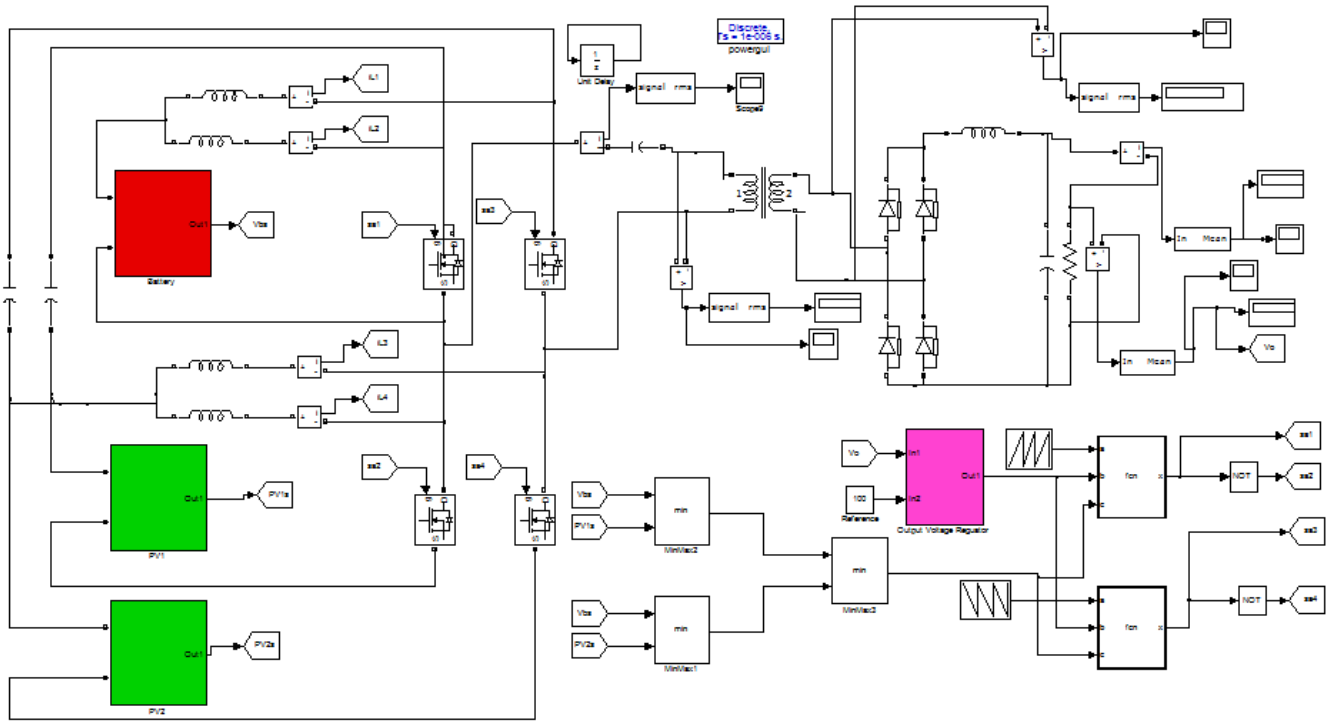
e/Δe	*NS*	*NL*	*ZE*	*PS*	*PL*
NS	*NS*	*ZE*	*NS*	*PS*	*NL*
NL	*NL*	*PL*	*NS*	*ZE*	*PS*
ZE	*NS*	*NL*	*ZE*	*PS*	*PL*
PS	*PL*	*NS*	*NS*	*PS*	*ZE*
PL	*NL*	*PS*	*PL*	*ZE*	*PL*

V. SIMULATION RESULTS AND DISCUSSION

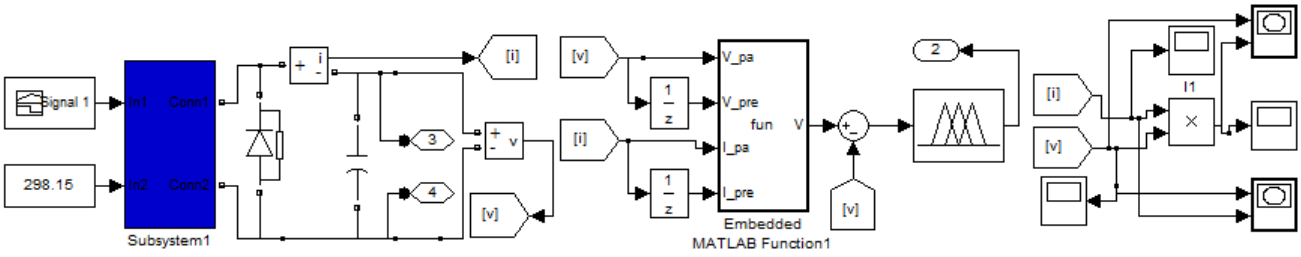
Using MatLab/Simulink environment, the PV model was developed and interfaced to the proposed four-port converter [23-24]. To supply the required load power under various operating conditions, optimal sizing of the battery and the PV ports was done. To achieve the required voltage in the PV ports, three panels were connected in series, since the maximum required load current of the converter was to be 5 A and the source current was chosen to be twice that of the maximum load current. Hence four panels were connected in parallel to supply the required current. Therefore the PV array size became 3×4. The parameters of FP-SEPIC/ZETA converter are given in Table II. The Simulink model of the converter incorporating centralized control loops using FLC is shown in Fig. 10. The surface plot corresponding to OVR is shown in Fig. 11.

TABLE II. PARAMETERS OF FP-SEPIC/ZETA CONVERTER

Parameter	**Value**
PV port & output port power, P_{PV1}, P_{PV2} & P_o	(0-500) W
Battery voltage, V_b	72 V ±10 %
Turns ratio, n	1.66
PV voltage, V_{PV1}, V_{VP2}	(40-50) V
Output voltage, V_o	100 V
Switching frequency, f_s	100 kHz
Capacitance, C_1, C_2, C_b, C_o	470 µF
Inductance, L_1,L_2,L_3,L_4, L_o	220 µH
Voltage at Maximum power, V_{mp}	16.48 V
Current at Maximum power, I_{mp}	2.25 A
PI parameters of OVR loop, K_P & K_I	130 & 1100



(a)



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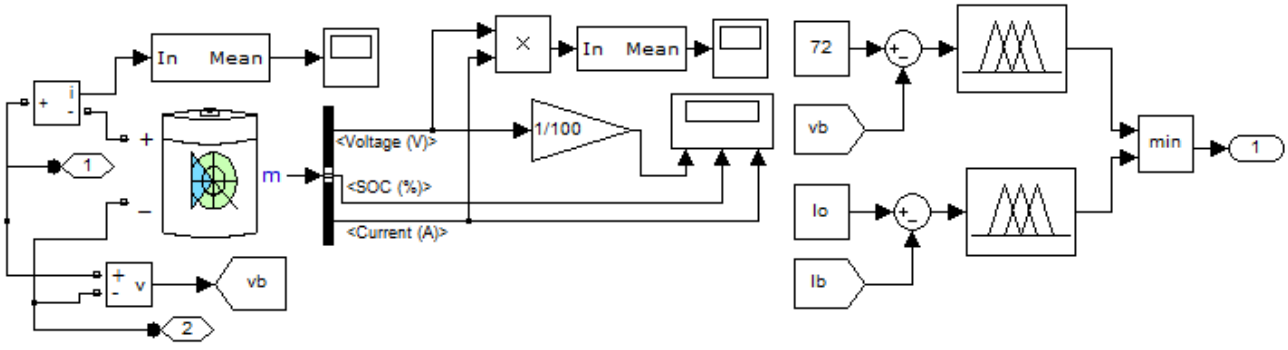
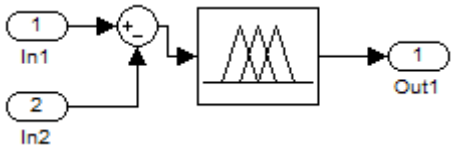


(c)



(d)

Figure 10. Simulink model (a) FLC based centralized control system (b) IVR loop of PV port 1 and port 2 (c) BVR and BCR loop (d) OVR loop

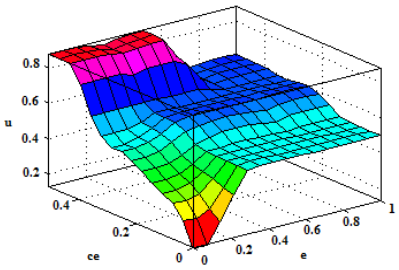
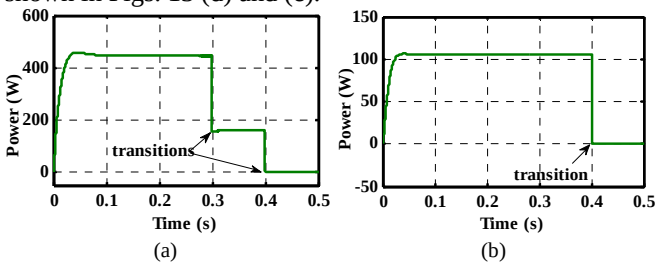


Figure 11. Surface plot for error, change in error, and control variable of OVR loop

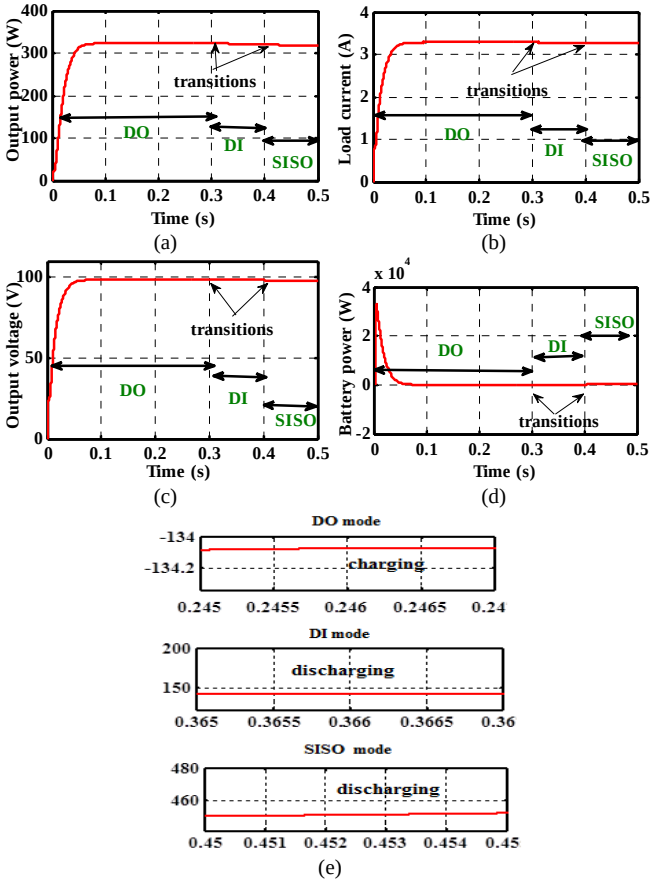
To test the feasibility of the FP-SEPIC/ZETA BDC, the required output power and voltage for powering the DC load were chosen to be 100 V and 330 W respectively. The work state switching among DO, DI, and SISO modes was also tested. The test was performed by changing the insolation of the two PV ports under constant loaded condition. To verify the operation of the DO mode the total power produced by the two PV ports was fixed around 555 W such that the PV port 1generated a power of 440 W and PV port 2 generated a power of 115 W. This additional power supplied the load and also charged the battery. Hence after supplying the load of 330 W, a power of about 134 W was stored in the energy storage device. Similarly when the generated power on the PV ports was varied, the DI and the SISO modes of operation were verified. The generated power was reduced just by shading the PV panel, thereby changing the insolation consequently.

Figs. 12 (a) and (b) show the PV power of port 1 and port 2 in which the 2 transitions were given at 0.3 s and 0.4 s. Till first transition the amount of power produced by the PV ports was 555 W and from the first transition to the second transition the amount of power produced by the PV ports was 370 W and after second transition there was no insolation and hence no power have been generated in the PV ports. In all these conditions the output voltage was maintained constant at the desired value of 100 V, so as to enable the centralized controller to achieve power balance in the system. The required load power and the corresponding load current are also shown in Fig. 13 (a) and (b) respectively. The voltage obtained at different modes of operation is illustrated in Fig. 13 (c). The battery power along with the zoomed view in different operating modes is shown in Figs. 13 (d) and (e).



(a) (b)

Figure 12. Generated power in the PV ports (a) Port 1 (b) Port 2

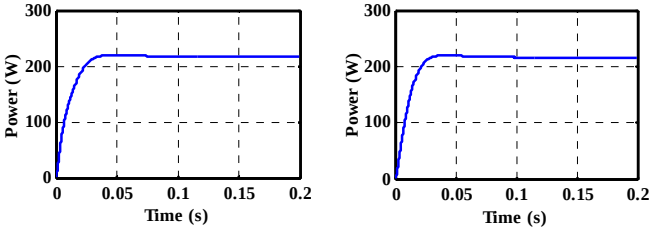


(a) (b) (c) (d)

(e)

Figure 13. Simulated results (a) Output power (b) Output current (c) Output voltage (d) Battery power (e) Zoomed view of the battery power

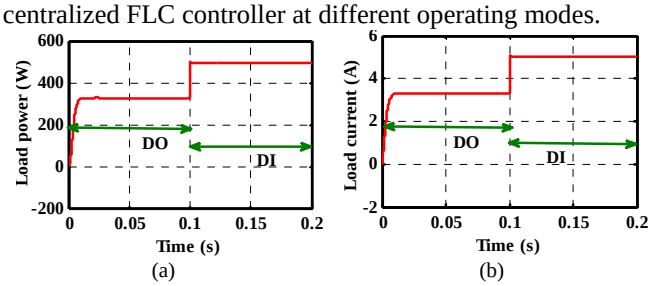
The flexibility of the centralized FLC controller was also analyzed under different load conditions. Under this condition, the input power in both the PV ports was maintained constant as shown in Figs. 14 (a) and (b) respectively. Hence each PV port could generate the constant power of 220 W, thereby generating the total power of 440 W.



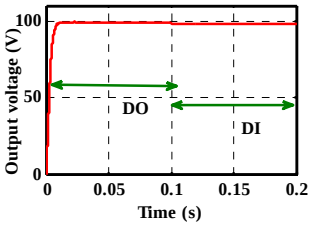
(a) (b)

Figure 14. Generated power in the PV ports (a) Port 1 (b) Port 2

The step change in load at 0.1 s from 350 W to 500 W is given in Fig. 15 (a) and the corresponding change in the load current is shown in Fig. 15 (b). The obtained desired output voltage at different load conditions is shown in Fig. 15 (c), thereby validating the effectiveness of the centralized FLC controller at different operating modes.



(a) (b)



(c)

Figure 15. Simulated results (a) Output power (b) Load current (c) Output voltage

VI. Experimental Verification And Discussion

An experimental set-up with the same design parameter values as used in the simulation was built to complement the numerical results. The constructed prototype was controlled using DSPIC30F4011. Fig. 16 shows the photograph of the hardware set-up developed based on a digital PWM using DSPIC30F4011 microcontroller. The controller has provided the necessary switching signals to the driver circuit. Fig. 17 (a) shows the generated control signal for the two power devices. The performance parameters of two PV ports and the control signal of other power devices along with the inductor current characteristics are shown in Figs. 17 (b) and 17 (c) respectively. The transformer primary voltage and the inductor current characteristics are shown in Fig. 17 (d).

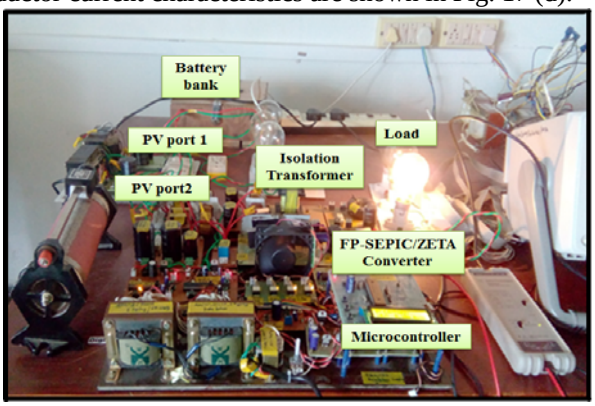
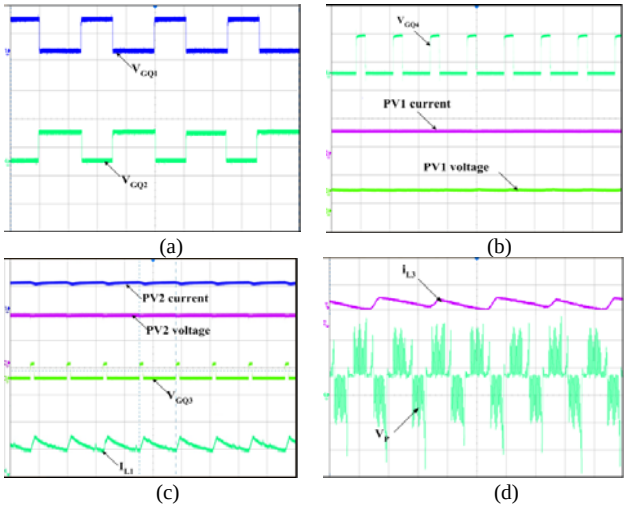


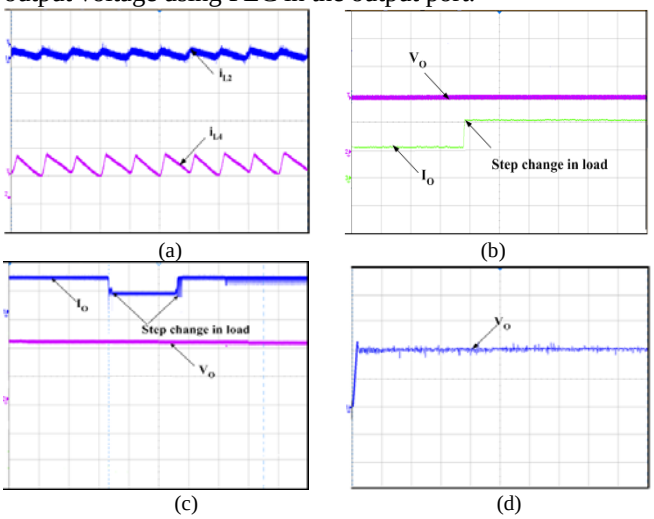
Figure 16. Photograph of experimental set-up



(a) (b) (c) (d)

Figure 17. Experimental results (a) Generated PWM control signal (X axis = 5 µs/div; Q_1 and Q_2 : Y axis = 10 V/div) (b) Control signal along with PV voltage and current in port 1 (X axis = 10 µs/div, PV voltage : Y axis = 50 V/div; PV current : 10 A/div; Q_4 : Y axis = 10 V/div) (c) Control signal and the inductor current along with PV voltage and current in port 2 (X axis = 10 µs/div, PV voltage : Y axis = 50 V/div; PV current : 10 A/div; Q_3: Y axis = 10 V/div and i_{L1} : Y axis = 5 A/div) (d) Inductor current i_{L3} along with the voltage across the primary of the transformer (X axis = 5 µs/div; i_{L3} : Y axis = 5 A/div; V_p : Y axis = 50 V/div).

The remaining inductor currents namely, i_{L2} and i_{L4} characteristics are shown in Figs. 18 (a). Fig. 18 (b) and 18 (c) show the measured output voltage and the load current when there is change in load power from 350 W to 500 W and from 500 W to 350 W. Fig. 18 (d) shows the obtained output voltage using FLC in the output port.



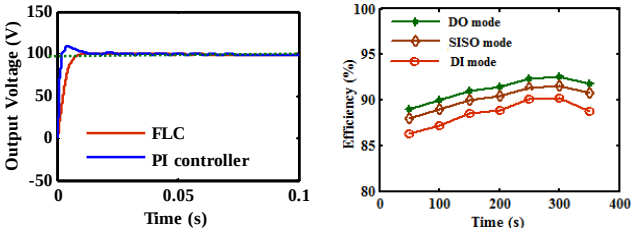
(a) (b) (c) (d)

Figure 18. Measured experimental results (a) Inductor current in L_2 and L_4 (X axis = 5 µs/div; i_{L2} and i_{L4} : Y axis = 5 A/div) (b) Output voltage under step increase in load (X axis = 5 µs/div; I_o : Y axis = 2 A/div; V_o : Y axis = 50 V/div) (c) Output voltage under step decrease and increase in load (X axis = 5 µs/div; I_o : Y axis = 5 A/div; V_o : Y axis = 50 V/div) (d) Response of the system with FLC for the load power of 350 W (X axis = 5 µs/div, Y axis =50 V/div).

The performance of the FP-SEPIC/ZETA BDC with the centralized FLC controller was also compared with the centralized PI controller and the output voltage waveform is shown in Fig. 19 (a). The time domain specifications for the voltage waveforms obtained using centralized FLC and PI controllers and the comparison is given in Table III.

Table III. Time domain parameters of two controllers

Parameter	PI	FLC
Maximum overshoot, M_p	6.8 %	0
Settling Time, t_s	50 ms	12 ms
Peak Time, t_p	5.2 ms	0
Output Voltage, V_o	98.72 V	98.88 V
Steady state error, e_{ss}	1.28 V	1.12 V



(a) (b)

Figure 19. (a) Output voltage waveform with FLC and PI controller (b) Converter efficiency under different operating modes using FLC

It can be seen from the waveform that the FLC based system has improved dynamic response compared with the PI controlled system. The efficiency of the system was calculated with respect to the different power flow paths like PV ports to the load, PV ports to the battery, and battery port to the load. By analysis the efficiency of the PV ports to the load was less when compared with the other power flow paths. Since the loss involved in the PV ports to the load is high as it is isolated topology. The measured efficiency of the converter under three different modes of operation is

illustrated in Fig. 19 (b). It was observed that the maximum efficiency of the converter under the output power of 350 W was 92.6 % with the average efficiency being around 91 %.

VII. Conclusion

In this paper, a new partially isolated FP-SEPIC/ZETA converter for photovoltaic applications with less number of switches. The performance was analyzed using centralized FLC controller. The power balance could be achieved in different operating modes, as the proposed topology is capable of achieving MPPT, maintaining SoC under battery charging and discharging operation and besides regulating the output voltage. The time domain specifications and the steady state parameters of the voltage obtained on the load port were analyzed using centralized FLC controller and the results were compared with the centralized PI controller. The FLC based centralized controller was found to be more efficient for wide variations in the insolation and load currents. The settling time obtained in the output voltage using centralized FLC was 76 % less when compared with the PI controller. The effectiveness of the FLC based centralized controllers was also verified with different parameter variations. The simulation results were validated by the experimental results. The proposed converter can also be extended to interface several sources.

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