High Performance Wideband CMOS CCI and its Application in Inductance Simulator Design

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***Abstract*—In this paper, a new, differential pair based, low-voltage, high performance and wideband CMOS first generation current conveyor (CCI) is proposed. The proposed CCI has high voltage swings on ports X and Y and very low equivalent impedance on port X due to super source follower configuration. It also has high voltage swings (close to supply voltages) on input and output ports and wideband current and voltage transfer ratios. Furthermore, two novel grounded inductance simulator circuits are proposed as application examples. Using HSpice, it is shown that the simulation results of the proposed CCI and also of the presented inductance simulators are in very good agreement with the expected ones.**

***Index Terms*—CCI, first generation current conveyor, grounded inductance simulator.**

I. INTRODUCTION

The circuit concept of the first generation current conveyor (CCI) as an active element suitable for the design of instrumentation and communication building blocks has been presented by Smith and Sedra in 1968 [1], where also basic implementation of the CCI using BJT transistors has been discussed. Due to the progress in microelectronics and the designers moved to CMOS transistors and an AB class CMOS first generation current conveyor without and with bias stabilization has been presented in [2]. In this paper new accurate and wideband CMOS realization of the first generation current conveyor is proposed. The main feature of the presented CCI is the low impedance of the input current port X. This property is achieved using the principle of super source follower configuration [3]. First, describing the internal structure of the CCI, the performance and parameters of the active element are given. Subsequently using the AMS 0.35 μm CMOS technology simulation results of the proposed CCI are presented that show high voltage swing possibilities on input and output ports and wideband current and voltage transfer ratios.

Furthermore, two grounded inductance simulator circuits are presented as application examples. The design of inductance simulators is still attractive since the behavior of physical inductors cannot be close to ideal component behavior in comparison to resistors and capacitors and in terms of spatial dimensions. They are larger than the other circuit elements, if the inductance value is not sufficiently small. Actively simulated inductors find application areas like oscillators and active filter design problems. For this reason, there are many publications on the active simulation of inductances [4]-[30] using various current-mode active elements. One of these active elements is the CCI that has not found enough application areas in the design of the inductance simulators except [10]. Therefore, two supplementary inductance simulators are presented with CCI in addition to a novel CMOS CCI implementation. HSpice simulations are performed to verify the theory.

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II. THE PROPOSED CMOS CCI

The CCI is a three terminal active device which ensures two functionalities between its terminals. The voltage applied to Y port is copied to X port and the current flowing through X port is copied to Y and Z ports all with unity gains. The port relations of a CCI can be described by the following equation:

$$\begin{aligned} V_X &= \beta V_Y, \\ I_Y &= \gamma I_X, \\ I_Z &= \alpha I_X. \end{aligned} \tag{1}$$

where β, γ, and α are unity for an ideal CCI and they represent the voltage and current transfer gains, where all currents defined to flow into the device.

The proposed CMOS CCI (Fig. 1) depends on differential pairs to provide high voltage swings on ports X and Y. The operation of the circuit can be explained as follows: transistors M_4 and M_{13} provide DC biasing currents for the differential pairs. Active load transistors M_2-M_3 and M_{20}-M_{21} force equal currents to source coupled transistors M_7-M_{10} and as a result gate-to-source voltages of M_7, M_{10} and M_8, M_9 have equal values, $v_{gs7} = v_{gs10}$ and $v_{gs8} = v_{gs9}$. This operation allows the voltage at output port to follow the voltage at input port.

The CCI employs two source followers, M_{11} and M_{12}, to obtain low equivalent impedance at X port. A well known method to reduce the impedance is to use feedback. This technique can be conveniently applied to the source followers M_{11} and M_{12}. When local feedback is applied to the source follower transistors improved output stages can be obtained. These new configurations are called super source followers [3]. The gain stage amplifies the difference

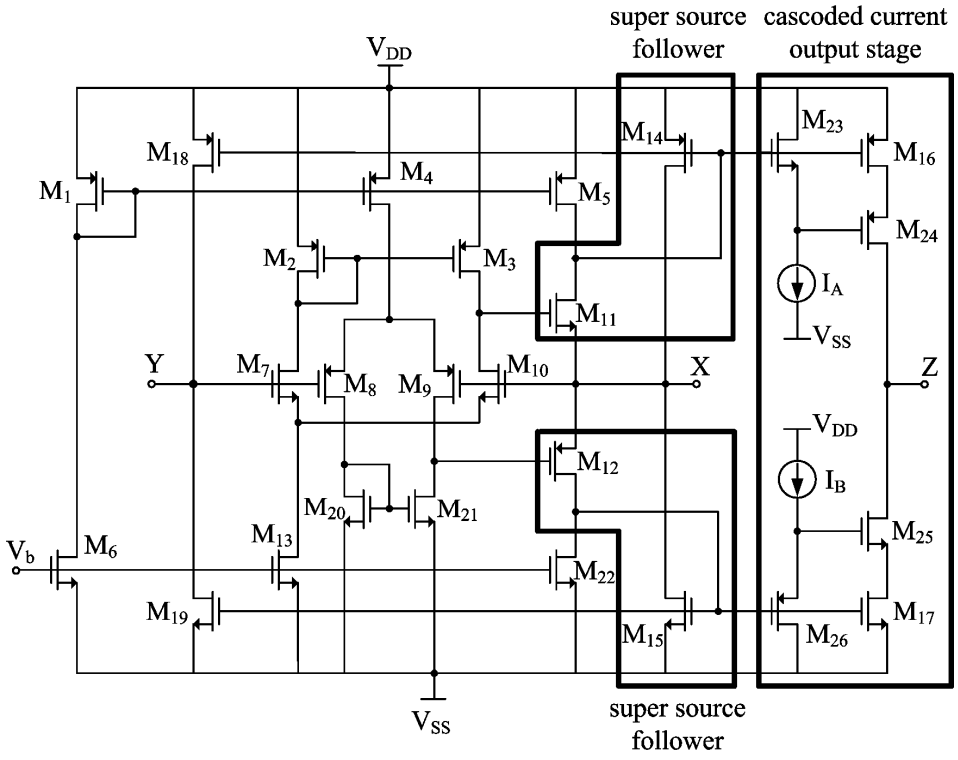

Figure 1. The proposed high performance CMOS CCI

between the input and output of the source follower, thus reducing the output impedance by the amplification factor of the gain stage itself. The improved differential pair based CMOS CCI that employs super source followers is shown in Fig. 1. Just like the conventional source follower, the input signal is replicated at the sources of M_{11} and M_{12}, but it is also amplified at the drains of same transistors. The amplified signal is fed to the inputs of M_{14} and M_{15} which operate as the input elements of the second gain stage [3]. Feedback loops are thus established through transistors M_{11}, M_{14} and M_{12}, M_{15}. With the improved configuration, the equivalent resistance on port X, when the Y terminal is grounded is equal to:

$$R_x = \frac{1}{g_{m11}g_{m14}r_o(1+g_{m10}r_o/2)} \Big\| \frac{1}{g_{m12}g_{m15}r_o(1+g_{m9}r_o/2)}. \quad (2)$$

The β parameter of the proposed CCI can be easily derived and it is equal to:

$$\beta \cong \frac{v_X}{v_Y} = \frac{g_{m7,8}}{g_{m9,10}}. \quad (3)$$

Transistors with large output resistances are required to obtain a β value that depends only on the input pair transconductance ratios. The β parameter is given by the transconductance ratios of the input transistors, so it is very close to the ideal unitary value.

A cascoded current output stage with dynamic matching [31-32] is employed at Z port to provide both high current swing and high output impedance. The equivalent resistance seen on port Z is equal to:

$$R_Z \cong g_{m25}r_{o25}r_{o17} \| g_{m24}r_{o24}r_{o16}. \quad (4)$$

The α parameter is equal to:

$$\alpha \cong \frac{i_Z}{i_X} \cong \frac{g_{m16,17}}{g_{m14,15}}. \quad (5)$$

If the load impedance connected to high impedance port Z is negligible with respect to the transistor output resistances, the α parameter can be given by the transconductance ratios of the current mirror transistors and it is very close to the ideal unitary value.

Transistors M_{18} and M_{19} are used to copy the current flowing through X port to Y port. The equivalent resistance seen on port Y, when X terminal is left open circuit is equal to:

$$R_Y \cong \frac{r_{o18}r_{o19}}{r_{o18}+r_{o19}}. \quad (6)$$

Similar to (5), the γ parameter can be calculated as:

$$\gamma \cong \frac{i_Y}{i_X} = \frac{g_{m18,19}}{g_{m14,15}}. \quad (7)$$

III. Application Examples: Grounded Inductance Simulator Circuits

The proposed grounded inductance topologies are given in Fig. 2. The circuit in Fig. 2(b) employs a voltage buffer [3]. For the proposed circuit in Fig. 2(a), the following input impedance function is obtained for the matching conditions of $R_1 = R/3$, $R_2 = R_4 = R/2$, and $R_3 = R$:

$$Z_{L1} = \frac{V_{in1}}{I_{in1}} = \frac{sCR^2}{10} = sL_{eq1}. \quad (8)$$

Hence:

$$L_{eq1} = \frac{CR^2}{10}. \quad (9)$$

Thus, a lossless grounded inductance simulator is realized.

The impedance transfer function for the circuit shown in Fig. 2(b) is equal to:

$$Z_{L2} = \frac{V_{in2}}{I_{in2}} = R_1 + R_2 + sCR_1R_2 = R_s + sL_s. \quad (10)$$

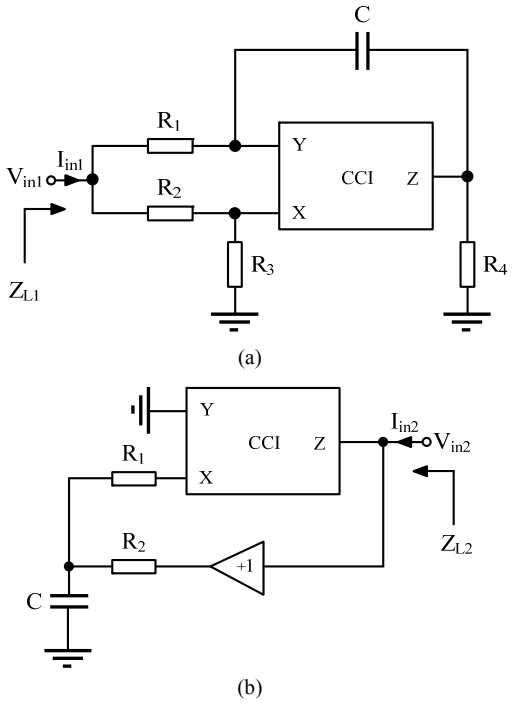

Figure 2. The proposed inductance simulator circuits: (a) lossless one, (b) lossy one

Therefore, the circuit simulates an inductor in series with a resistor calculated as:

$$L_s = CR_1R_2, \quad R_s = R_1 + R_2. \quad (11)$$

Taking into consideration the non-ideal affects, the input impedance functions of the inductance simulators in Figs. 2(a) and 2(b) will be respectively equal to:

$$Z'_{L1} = \frac{V_{in1}}{I_{in1}} = \frac{sCR^2\left(5-3\alpha\beta-3\beta\gamma\right)+6R\left(1-\beta\gamma\right)}{sCR\left(16+6\alpha+6\gamma-6\beta-11\alpha\beta-11\beta\gamma\right)+}, \quad (12)$$
$$+2\left(6+6\gamma-6\beta-11\beta\gamma\right)$$

$$Z'_{L2} = \frac{V_{in2}}{I_{in2}} = \frac{R_1 + R_2 + sCR_1R_2}{\alpha\beta}, \quad (13)$$

where the β in (13) denotes the non-ideal transfer gain of the additional voltage buffer. From (12) and (13) it can be observed that both proposed inductance simulators are affected by the non-idealities of the CCI. However, they can be minimized by precision design of the active element.

In (12) only taking α into account with $\beta = 1$ and $\gamma = 1$, then the equivalent admittance becomes:

$$Y'_{L1} = \frac{1}{Z'_{L1}} = \frac{5\left(1-\alpha\right)}{R\left(2-3\alpha\right)} + \frac{10}{sCR^2\left(3\alpha-2\right)} = \frac{1}{R_p} + \frac{1}{sL_p}, \quad (14)$$

where $R_p = R(2-3\alpha)/(5(1-\alpha))$ and $L_p = CR^2(3\alpha-2)/10$. Thus, the circuits can realize an inductor in parallel with a resistor. The quality factor Q for the proposed inductor is calculated as:

$$Q_{L1} = \frac{R_p}{\omega L_p} = \frac{2}{\omega CR\left(\alpha-1\right)}. \quad (15)$$

Considering that the α becomes a variable, four types of inductors can be obtained:

(1) If α is equal to unity, a pure inductor is obtained, equivalent to the case given in (9).
(2) If α is greater than unity, a lossy inductor with a parallel positive resistor is obtained.
(3) If α is less than unity and greater than 2/3, a lossy inductor with a parallel negative resistor is obtained.
(4) If α is less than 2/3 and greater than zero, a lossy negative inductor with a parallel positive resistor is obtained.

IV. Simulation Results

To show the performance of the new CCI, it has been designed using the AMS 0.35 μm CMOS technology. The aspect ratios of the transistors from Fig. 1 are given in Table I. The supply and bias voltages are $V_{DD} = -V_{SS} =$ 1.65 V and $V_b = -0.97$ V. The current source I_A is implemented with a NMOS transistor with a bias voltage $V_A = -0.8$ V connected to its gate and similarly the current source I_B is implemented with a PMOS transistor with its gate connected to $V_B = 0.75$ V.

The simulation results of the equivalent impedance magnitudes on port X are given in Fig. 3. Its value is only 5.2 Ω at 1 MHz, 10.3 Ω at 10 MHz and 115 Ω at 100 MHz. Port Y parasitic impedance value is about 118 kΩ at low frequencies and its value decreases as the frequency increases. Its value is about 126 kΩ at 10 MHz and 21 kΩ at 100 MHz. With the improved current output stage, port Z impedance has a value of about 20.8 MΩ at low frequencies. Its value is about 172 kΩ at 10 MHz and 18 kΩ at 100 MHz. It is seen that the impedance values of the proposed CCI are very similar to the ideal CCI values in a wide frequency range. The simulation results of the equivalent impedances on ports Y and Z are given in Fig. 4 and Fig. 5, respectively.

In Fig. 6 the linear operation region of the voltage follower stage is given for the ideal CCI, the proposed CCI and the difference between the two. The proposed circuit has a linear voltage following action between ±1.1 V with less than ±6 % error.

TABLE I. THE ASPECT RATIOS

Transistor	**W/L (μm/μm)**
M_1, M_5, M_{14}, M_{16}, M_{18}	30/0.5
M_{11}	30/0.35
M_{12}	90/0.35
M_7, M_{10}, M_{13}	20/0.5
M_8, M_9, M_4	60/0.5
M_2, M_3	60/0.35
M_{20}, M_{21}	20/0.35
M_6, M_{15}, M_{17}, M_{19}, M_{22}	10/0.5
M_{23}, M_{25}	20/0.7
M_{24}, M_{26}	60/0.7

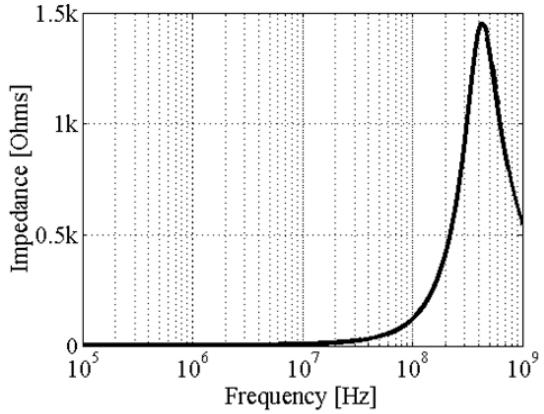

Figure 3. Frequency variation of the port X impedance magnitude

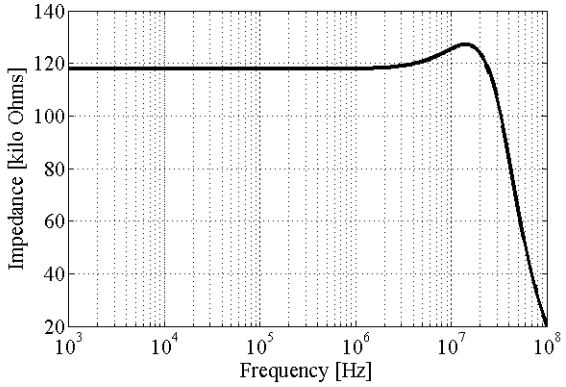

Figure 4. Frequency variation of the port Y impedance magnitude

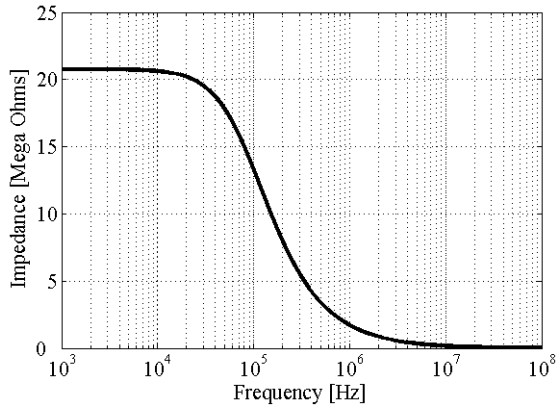

Figure 5. Frequency variation of the port Z impedance magnitude

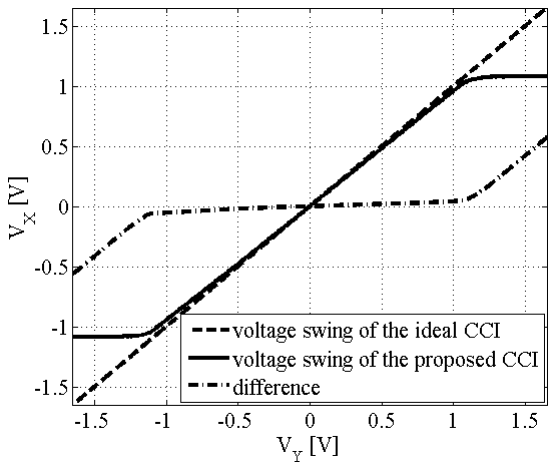

Figure 6. DC voltage transfer characteristics from port Y to port X

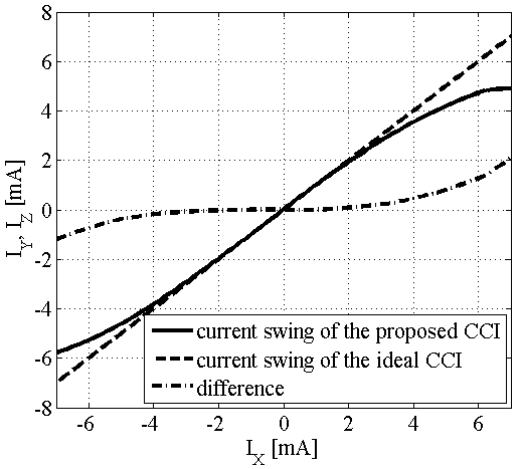

Figure 7. DC current transfer characteristics from port X to ports Y and Z

The linear current swings of ports Y and Z are identical and they are between ±4 mA with less than 5 % error as shown in Fig. 8. From the DC transfer characteristics, offset voltage on port X and offset currents on ports Y and Z are obtained. When port Y is grounded, the offset voltage obtained at port X is about 0.8 mV. Similarly, when the current applied at port X is zero, the offset currents flowing through port Y and Z are obtained as 2.5 μA.

The current and voltage transfer ratios, α, γ and β, are found to be 0.99, 0.99 and 0.98, respectively; with 625 MHz current transfer bandwidth from port X to port Z, 700 MHz current transfer bandwidth from port X to port Y and 770 MHz voltage transfer bandwidth from port Y to port X are obtained as given in Fig. 8 with about 985 μW power consumption.

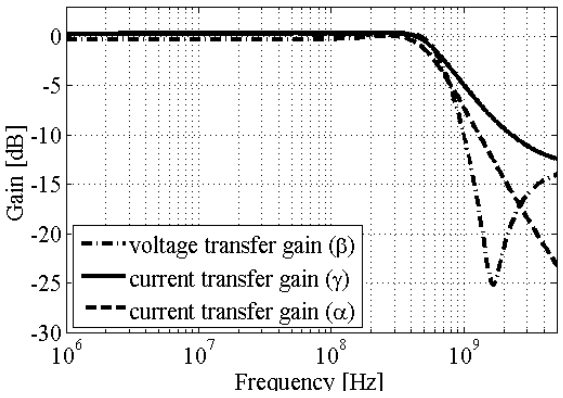

Figure 8. AC voltage and current transfer gains

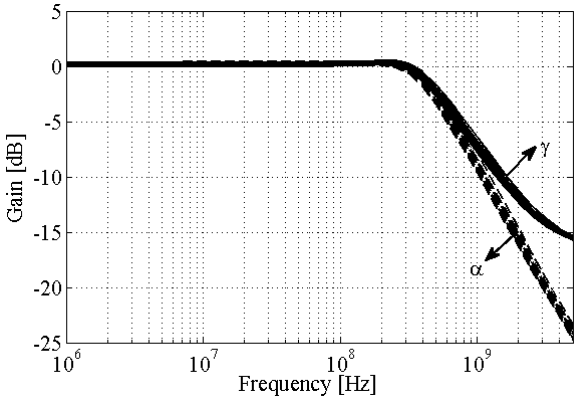

Figure 9. Monte-Carlo analyses of the current transfer gains

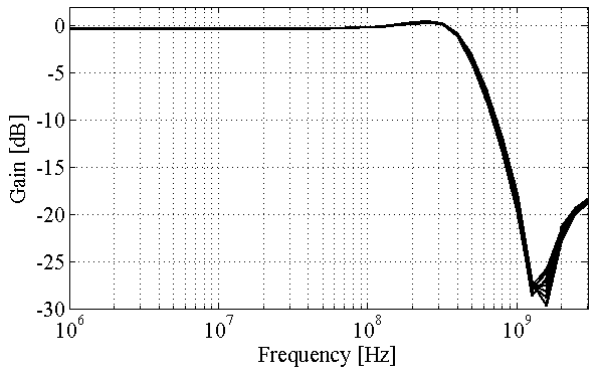

Figure 10. Monte-Carlo analysis of the voltage transfer gain

Monte-Carlo simulations of the proposed circuit are also performed to look at the effects of the process variations of W, L, t_{ox} and V_{T0} parameters of each transistor are varied by using the values supplied by the AMS. Simulation results are given in Fig. 9 and Fig. 10. Variations on the current and voltage transfer ratios are below 5 %.

The total harmonic distortion (THD) of the proposed circuit is determined by applying 1 MHz sinusoidal input signals to Y and X ports with various amplitudes. THD is found less than 10 % for the current signals below 7.5 mA and it is found less than 10% for the input voltages below 1.5 V. Simulation results are given in Fig. 11.

The functionality of the proposed lossless grounded inductance simulator circuit given in Fig. 2(a) is tested both in time and frequency-domain. Time-domain functionality of the circuit is illustrated with element values $R_1 = 1\text{k}\Omega$, $R_2 = 1.5\ \text{k}\Omega$, $R_3 = 3\ \text{k}\Omega$, $R_4 = 1.5\ \text{k}\Omega$, and $C = 0.25\text{nF}$ to obtain an inductor of value 225 μH.

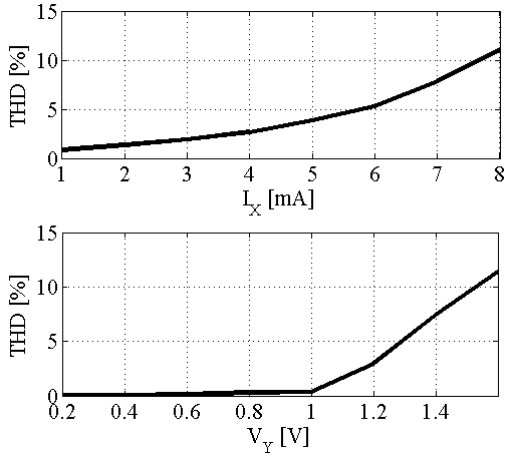

Figure 11. Output harmonic distortion versus input current and voltage at 1 MHz

A triangular current signal of 50 μA peak value is applied to the inductor. Also an equal current is applied to an ideal passive inductor. The input current and the ideal/simulated inductor voltages are shown in Fig. 12. The inductor voltage is a square wave with 22.5 mV peak value where $V_L = L_{eq} dI_L/dt$.

V. CONCLUSION

In this paper, differential pair based high performance wideband CMOS CCI is proposed. Moreover, two novel grounded inductance simulators that employ a single CCI are also given as an application example. It is shown that the simulation results are in very good agreement with the expected ones.

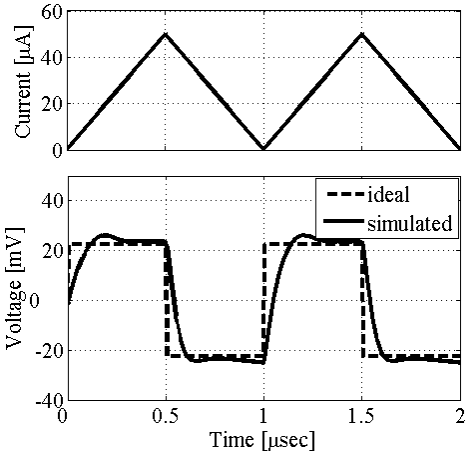

Figure 12. Time domain simulation results of the grounded inductance simulator given in Fig. 2(a)

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