BULLETIN OF THE POLISH ACADEMY OF SCIENCES
TECHNICAL SCIENCES, Vol. 61, No. 3, 2013
DOI: 10.2478/bpasts-2013-0074

Technique to improve CMRR at high frequencies in CMOS OTA-C filters

G. BLAKIEWICZ*

Department of Microelectronic Systems, Gdansk University of Technology, 11/12 Narutowicza St., 80-952 Gdansk, Poland

Abstract. In this paper a technique to improve the common-mode rejection ratio (CMRR) at high frequencies in the OTA-C filters is proposed. The technique is applicable to most OTA-C filters using CMOS operational transconductance amplifiers (OTA) based on differential pairs. The presented analysis shows that a significant broadening of CMRR bandwidth can be achieved by using a differential pair with the bodies of transistors connected to AC ground, instead of using a pair with the bodies connected to the sources. The key advantages of the technique are: no increase in power consumption (except for an optional tuning circuit), a small increase of a chip area, a slight modification of the original filter. The simulation results for exemplary OTAs and a low-pass filter, designed in a 0.35 μm CMOS process, show the possibility of broadening the CMRR bandwidth several times.

Key words: common-mode rejection ratio, CMRR, CMOS, OTA, differential pair, OTA-C filters, component mismatch.

1. Introduction

OTA-C filters are frequently used in mixed-signal systems on a chip (SoC) [1, 2]. These filters provide a necessary signal pre and post processing in a mixed analogue-digital environment, where the analogue signals have to be limited in frequency before and after the analogue to digital and digital to analogue conversions. Such an environment imposes extremely difficult working conditions for the analogue filters due to the presence of a high level, broadband noise generated by the digital sub-circuits. The digital noise, which propagates along a silicon substrate, can significantly degrade the dynamic range of the analogue filters [3, 4]. One of the most commonly used method to reduce the substrate noise interference is based on application of the fully-differential filters, capable of reducing the influence of the common-mode (CM) component of the noise. However, the effectiveness of the noise suppression by such filters is limited in magnitude and frequency. At low frequencies, the maximum attenuation is mainly limited by the degree of matching of the symmetrical signal paths. By careful design of such filters a relatively high attenuation (> 60 dB) can be achieved in this frequency range. At high frequencies, the filter working conditions further deteriorate because of the CMRR frequency response degradation [5, 6], which typically occurs at frequencies greater than several MHz. The aforementioned problems cause a relatively poor attenuation of substrate noise with a frequency spectrum which may reach the GHz range.

The problem of CMRR bandwidth optimisation has not been widely analysed in the literature so far. There are just a few circuit proposals for broadening the CMRR frequency response, [7, 8] for differential amplifiers using bipolar junction transistors (BJT), and [9] for a CMOS technology. However, none of these proposals can improve CMRR at tens of mega hertz. To address this important problem a new technique to improve CMRR characteristic at high frequencies is proposed in this paper.

Most circuit designers are convinced that there is no significant difference in CMRR characteristic of the two configurations of a differential pair, with the transistor bodies connected to their sources or connected to AC ground. The analysis presented in this paper shows that the latter configuration, under certain conditions, allows substantial improvement of the CMRR bandwidth.

The remaining part of this paper is organized as follows. Section 2 presents an analysis and comparison of CMRR characteristic for two configurations of a differential pair, and explains the main idea of the proposed improvement technique. Section 3 discusses the application of the improvement technique to the OTA-C filters. The last two sections present simulation results and the final conclusions.

2. CMRR improvement technique

2.1. CMRR frequency characteristic of a differential pair. In most cases a differential pair with the bodies of transistors connected to their sources (configuration BS) is used. To explain an important advantage of using the alternative configuration with the bodies connected to the AC ground (the configuration BG), the CMRR characteristic of both configurations are analysed and compared.

The analysis of CMRR of a differential pair has been carried out in [5, 6, 9], however the differential pair in BG configuration with mismatched transistors has not been analysed in detail. Therefore, a general configuration shown in Fig. 1 is considered. Additionally, a low impedance load of the differential pair is assumed, which directly corresponds to a cascode or a folded cascode configuration. A small signal

*e-mail: blak@eti.pg.edu.pl

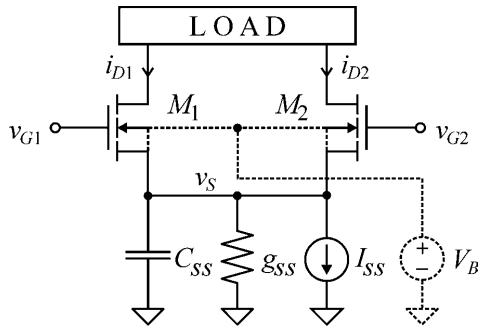

Fig. 1. Considered configuration of a differential pair

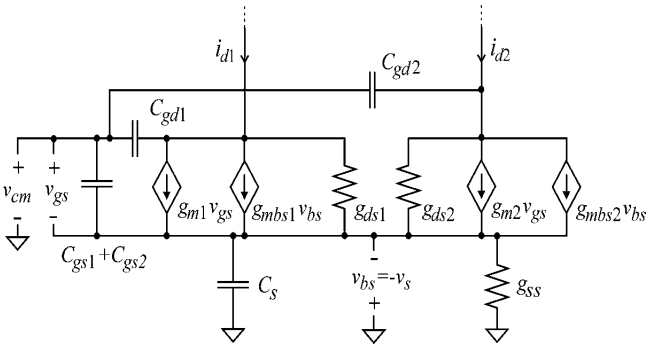

Fig. 2. Small-signal model of the basic differential pair for CM signal

model of such a circuit is depicted in Fig. 2, where each transistor is represented by: the gate $g_{m1(2)}$ and the body $g_{mbs1(2)}$ transconductances, the output conductance $g_{ds1(2)}$, and the internal capacitances $C_{gs1(2)}$, $C_{gd1(2)}$, $C_{bs1(2)}$. In further considerations, CMRR is defined for the CM input voltage $v_{CM} = (v_{G1} + v_{G2})/2$ and the differential-mode (DM) output current $i_{DDM} = i_{D1} - i_{D2}$, because this kind of rejection has the greatest impact on the substrate noise attenuation in mixed-signal systems. Based on the small-signal model, the differential output current $I_{ddm}(s)$ can be determined as

$$\begin{aligned} I_{ddm}(s) = I_{d1}(s) - I_{d2}(s) &= (g_{m1} - g_{m2})\, V_{gs}(s) \\ &+ (g_{mbs1} - g_{mbs2})\, V_{bs}(s) \\ &- (C_{gd1} - C_{gd2})\, sV_{cm}(s) \\ &- (g_{ds1} - g_{ds2})\, V_{bs}(s), \end{aligned} \tag{1}$$

where

$$V_{bs}(s) = -\frac{g_{m1} + g_{m2} + sC_i}{g_{m1} + g_{m2} + g_s + s\,(C_i + C_s)} V_{cm}(s), \tag{2a}$$

$$V_{gs}(s) = \frac{g_s + sC_s}{g_{m1} + g_{m2} + g_s + s\,(C_i + C_s)} V_{cm}(s) \tag{2b}$$

and $C_i = C_{gs1} + C_{gs2}$, $g_s = g_{ss} + g_{mbs1} + g_{mbs2} + g_{ds1} + g_{ds2}$, $g_{mbs1} = \eta g_{m1}$, $g_{mbs2} = \eta g_{m2}$. Depending on the differential pair configuration, $g_{mbs1(2)} = 0$ for BS or $g_{mbs1(2)} \neq 0$ for the other case. C_{well} represents the capacitance between the silicon substrate and the well where both transistors are located. In practical implementations of the differential pair there is always some degree of imbalance, due to technology variations, the mismatch of dimensions of the transistors, transistors non-linearity [10], or the existence of an input offset voltage $v_{G1} \neq v_{G2}$ [5]. To model such a situation it is assumed that the transistors M_1 and M_2 are mismatched, which is modelled by

$$\begin{aligned} g_{m1} &= g_m + \Delta g_m, \qquad & g_{m2} &= g_m, \\ g_{ds1} &= g_{ds} + \Delta g_{ds}, \qquad & g_{ds2} &= g_{ds}, \\ C_{gd2} &= C_{gd} + \Delta C_{gd}, \qquad & C_{gd1} &= C_{gd}. \end{aligned} \tag{3}$$

The mismatch of the internal capacitances of the transistors is restricted to ΔC_{gd}, because only capacitances C_{gd1} and C_{gd2} have the greatest influence on CMRR at low and medium frequencies [6]. The frequency characteristic of the differential output current (1) at this frequency range can be approximated by

$$\begin{aligned} I_{ddm}(s) &= I_{ddm1}(s) - I_{ddm2}(s) \\ &\cong A\frac{1 + s/\omega_z}{1 + s/\omega_p} V_{cm}(s) - s\Delta C_{gd} V_{cm}(s), \end{aligned} \tag{4}$$

where the expressions for A, ω_z, and ω_p are given in Table 1 for small mismatches between the transistors $\Delta g_m/g_m \ll 1$, $\Delta g_{ds}/g_{ds} \ll 1$, $\Delta C_{gd}/C_{gd} \ll 1$, and for a biasing current source of high resistance $g_{ss} \ll g_{ds}$. As indicated by (4), the differential output current consists of two components,

Table 1
Approximations of A, ω_z, ω_p for two configurations of the differential pair

Parameter	BS configuration ($\eta = 0$)	BG configuration ($\eta \neq 0$)
A	$(\Delta g_m/g_m - \Delta g_{ds}/g_{ds})\, g_{ds}$	$(\Delta g_m/g_m - \Delta g_{ds}/g_{ds})\, \frac{g_{ds}}{1+\eta}$
ω_z	$\frac{2g_{ds}}{C_s}$	$\frac{2g_{ds}}{C_s - \eta C_i}$
ω_p	$\frac{2g_m}{C_i + C_s}$	$\frac{2g_m}{C_i + C_s}$
C_s	$C_{ss} + C_{well}$	$C_{ss} + C_{bs1} + C_{bs2}$

$I_{ddm1}(s)$ related to Δg_m, Δg_{ds} mismatches, and $I_{ddm2}(s)$ associated with ΔC_{gd} mismatch. The main component $I_{ddm1}(s)$ has a single zero ω_z and a pole ω_p. The upper limit of CMRR at low frequencies is equal to g_m/A, which is a ratio of the gains for DM and CM input signals. As shown in Table 1 (1^{st} row), this limit is almost the same for both considered configurations of the differential pair ($\eta < 1$), and it depends on $\Delta g_m/g_m$ and $\Delta g_{ds}/g_{ds}$ mismatches. The zero frequency ω_z determines the -3dB drop of the CMRR frequency characteristic, because $g_m \gg g_{ds}$ and therefore $\omega_p \gg \omega_z$ (compare Table 1, and [6]). It is important to notice that for BG configuration, the zero frequency depends on the difference between C_s and C_i, and, as a result, can be shifted to high frequencies, if the following condition is satisfied

$$C_s = \eta C_i. \tag{5}$$

With (5) fulfilled, the degradation of CMRR at high frequencies can be significantly reduced. The exemplary characteristics of the components of the output current (4) are presented in Fig. 3 for both considered configurations, and with the condition (5) satisfied. In this figure the dashed lines refer to $C_{gd1} = C_{gd2}$ case, whereas the solid lines represent a 1% mismatch ($C_{gd2} = 1.01C_{gd1}$). The plots show that value of ΔC_{gd} limits the location of the dominant zero ω_z for the BG configuration. The BS configuration is almost insensitive to small mismatch ΔC_{gd}, because the effect of the current $I_{ddm2}(s)$ is masked by the effect of the zero ω_z, which is located at relatively low frequency. The characteristics for BG configuration show that increasing of ω_z can be achieved only if $I_{ddm1} > I_{ddm2}$. To estimate the significance of ΔC_{gd} mismatch, let us consider typical requirements for VHF transconductors, namely: CMRR = 60 dB with $\omega_z = 100$ MHz [11], and assume typical MOS transistor parameters $C_{gd} = 200$ fF, $g_m = 550$ μS for this frequency range. For this exemplary case, $I_{ddm1} > I_{ddm2}$ if $\Delta C_{gd}/C_{gd} < 0.44\%$ (calculated based on $CMRR = g_m/A$, $A > \Delta C_{gd}\omega_z$). In practical implementations of a differential pair the mismatch error, $\Delta C_{gd}/C_{gd}$ can be reduced to 0.05% [5] by careful design of a circuit layout using the common-centroid technique. Therefore, as long as the required CMRR is limited to 60–70 dB with the bandwidth below a hundred of MHz, the ΔC_{gd} mismatch has a much smaller impact in comparison to the dominant zero ω_z.

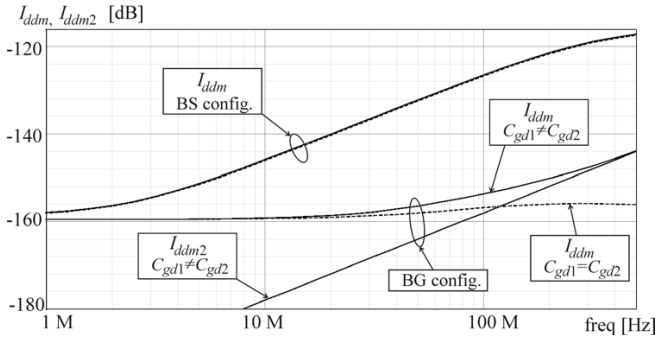

Fig. 3. Frequency characteristics of components of the differential current given by (4)

2.2. Influence of CMOS process variation on CMRR of a differential pair in BG configuration. The CMRR improvement for a differential pair in the BG configuration relies on the fulfilment of (5). To examine the influence of the process variation on CMRR, a typical 0.35 μm CMOS process is considered. In Table 2, the relative deviation $(\eta_{MC\,\max} - \eta_{MC\,\min})/\eta_{TM}$ between the maximum and minimum values of η, obtained using the Monte Carlo (MC) analysis, with respect to the typical mean (TM) value η_{TM} are shown for three exemplary body voltages V_B. It is seen that, in the worst case, η may differ by 7.2% ($V_B = 1$ V). This variation can be completely compensated by a proper change of V_B, because the tuning range is $\eta(V_B = 1) - \eta(V_B = 0)/\eta(V_B = 0.5) = 25.6\%$ in this case. The deviations $(\eta_{WS\,\max} - \eta_{TM})/\eta_{TM}$, and $(\eta_{WP\,\max} - \eta_{TM})/\eta_{TM}$ are also calculated for extremes of technology parameters, specified by the corners: WS – the worst case for a speed condition, and WP – the worst case for a power condition. Table 2 shows that for such corners, η may vary up to 25.3% (WP, $V_B = 1$ V), whereas the

Table 2
Deviation of η due to a 0.35 μm CMOS process variation[a]

V_B	$\frac{\eta_{MC\,\max} - \eta_{MC\,\min}}{\eta_{TM}}$	$\frac{\eta_{WS} - \eta_{TM}}{\eta_{TM}}$	$\frac{\eta_{WP} - \eta_{TM}}{\eta_{TM}}$	η_{TM}
0 V	4.3%	23.9%	−21.9%	0.2271
0.5 V	5.6%	25.0%	−23.0%	0.2530
1 V	7.2%	16.3%	−25.3%	0.2918
Range of η tuning: $\frac{\eta(V_B = 1V) - \eta(V_B = 0)}{\eta(V_B = 0.5V)}$		18.3%	20.9%	25.6%

[a] Calculated for n-channel MOS transistor with $W = 50$ μm, $L = 1$ μm, $I_D = 50$ μA, $v_G = 1.65$ V.

minimum tuning range is 18.3% (WS). This means that variation of η can be only partially compensated with a residual error of $25\% - 18.3\%/2 = 15.6\%$ in the worst case (WS). The realizable improvement of CMRR is also limited by tolerances of C_s and C_i. To determine this limit, the ratio *IF* of ω_z for both configurations is calculated

$$IF = \frac{[\omega_z]_{\text{BG - config.}}}{[\omega_z]_{\text{BS - config.}}} = \frac{1}{|\partial C_s/C_{s0}| + |\partial C_i/C_{i0}| + |\partial\eta/\eta_0|}, \tag{6}$$

where it is assumed that $C_i = C_{i0} + \partial C_i$, $C_s = C_{s0} + \partial C_s$, $\eta = \eta_0 + \partial\eta$ are actual values, and ∂C_i, ∂C_s, $\partial\eta$ represent deviations from the nominal values, which are related by $C_{i0} = \eta_0 C_{s0}$ (5). Using (6), one can easily determine that a 10% tolerance of the capacitances $\partial C_s/C_{s0} = \partial C_i/C_{i0} = 0.1$ leads to improvement of CMRR bandwidth equal to $IF \cong 3.7$ times for the BG configuration under an assumption of TM corner with $\partial\eta/\eta_0 = 7.2\%$. If a tuning of η is additionally applied ($\partial\eta/\eta_0 \to 0$), the improvement increases to $IF \cong 5$ times. For the worst case of the technology corners and applied tuning ($\partial\eta/\eta_0 = 15.6\%$), the improvement becomes $IF \cong 2.8$. The above considerations show that for the typical mean (TM) case the CMRR bandwidth can be extended at least several times, even without tuning of η.

3. Application of the CMRR improvement technique to the OTA-C filters

3.1. Basic concept. The fulfillment of (5) requires that C_i, the capacitance seen between the gate and source of M_1 or M_2, was equal to C_s/η, where C_s is the capacitance between the common sources and ground. For typical CMOS technologies, $\eta = 0.1...0.35$, which means that $C_i \cong 3...10C_s$. Such a relation is not normally satisfied in designs of OTA, where $C_s \cong C_i$. To meet the required condition, additional capacitors C_c must be connected between each gate and source in the input differential pair of OTA, as shown in Fig. 4. As a result, the input differential capacitance of such a modified OTA increases by $C_c/2$. The increased input capacitance is not a problem in most configurations of the OTA-C filters [5, 12, 13], where OTAs are connected in cascade with their outputs loaded by capacitors $C_{k-1}, C_k, \ldots$, as illustrated in Fig. 4. In such topologies the OTAs with increased input capacitances can be effectively exploited. To preserve a DM frequency characteristic of OTA-C filter, each original capacitance C_{k0} in its topology must be decreased by the OTA input capacitance, which means that the new capacitances become $C_k = C_{ko} - C_c$, $k = 1, 2, \ldots$. In such a modified filter, DM frequency characteristics remain unchanged, because the additional capacitors C_c are connected to the virtual ground (the common sources) and as a result they add up to the filter capacitances. The only change in the filter operation is a small reduction of the effective capacitance for CM, which may slightly modify the stability conditions for the common-mode feedback (CMFB) circuits.

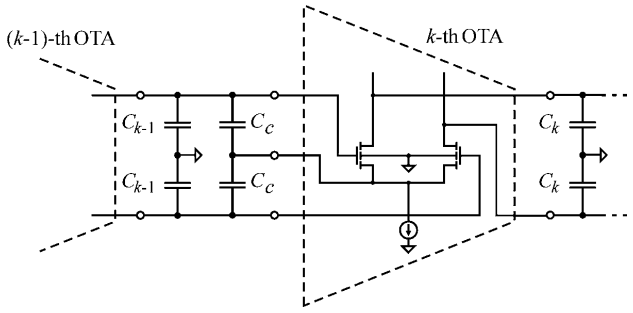

Fig. 4. Basic concept of application of the CMRR improvement technique to the OTA-C filters

3.2. Application of the CMRR improvement technique to other OTA configurations. The proposed CMRR improvement technique can be applied to any type of OTA based on a differential pair, as for example, the source degenerated [1] or the cross-coupled [11, 14] structures, presented in Figs. 5 and 6. In the case of the circuit in Fig. 5, each differential pair must be compensated by the individual capacitors C_{c1} and C_{c2}, properly adjusted to different dimensions of transistors M_1 and M_2 according to (5). The circuit in Fig. 6 requires only C_{c1} due to the fact that both differential pairs are in parallel for AC signals.

In order to investigate the effectiveness of the proposed improvement technique, the CMRR characteristics for selected OTAs were simulated assuming the input offset voltage $v_{G1} - v_{G2} = 3$ mV, and $\Delta C_{gd}/C_{gd} = 0.1\%$ for the transistors

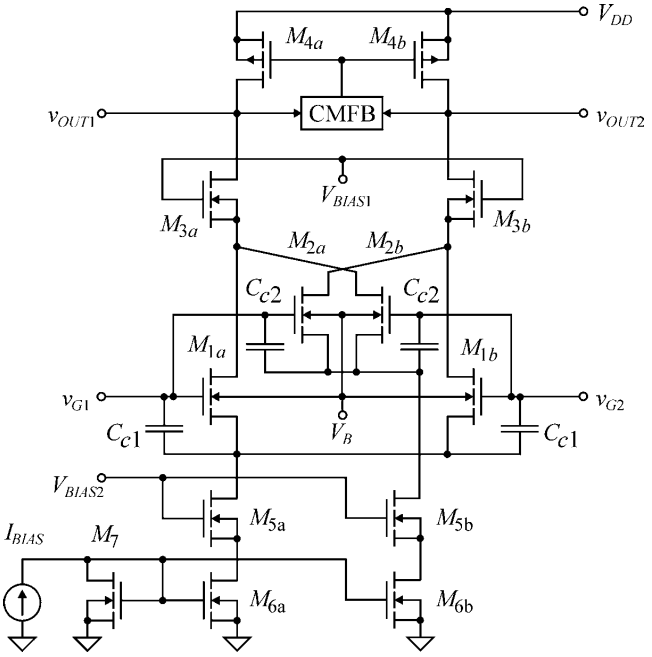

Fig. 5. Improved cross-coupled differential pair with differentiated biasing currents

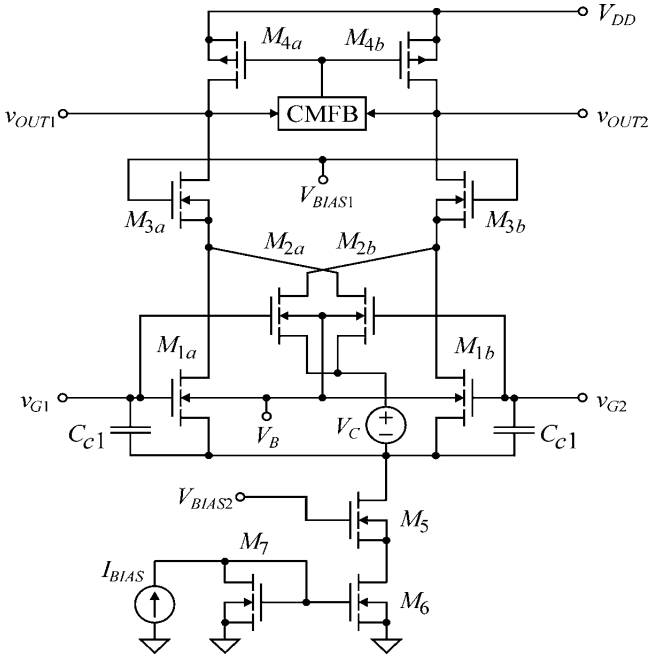

Fig. 6. Improved cross-coupled differential pair with a floating voltage source

in the differential pairs. The results are plotted in Fig. 7, for the compensated and uncompensated ($C_c = 0$, $C_{c1,2} = 0$) variants of OTA. The characteristics labelled C refer to the basic differential pair (Fig. 1), whereas those labelled A and B refer to the circuits in Figs. 5 and 6, respectively. As shown in Fig. 7, the frequency of zero ω_z is increased: from 8.8 MHz to 187 MHz for the basic differential pair, from 16.6 MHz to 97 MHz for OTA in Fig. 5, and from 11.7 MHz to 87 MHz for OTA in Fig. 6. All the simulations were curried out for the nominal compensation capacitances, calculated based on (5), and TM technology corner. The greatest improvement (over 20 times) is obtained for the basic pair, whereas for the linearized OTAs the improvement is limited to a factor of 7.4 times, in the worst case. As explained in Subsec. 2.1, the limitation in CMRR improvement for the linearized OTAs is caused by the $\Delta C_{gd}/C_{gd}$ mismatch, which for these circuits cumulates from two differential pairs. The summary of parameters of the simulated OTAs is listed in Table 3. The influence of a technology variation is illustrated in Fig. 8, where TM, WP, and WS corners are compared for circuit in

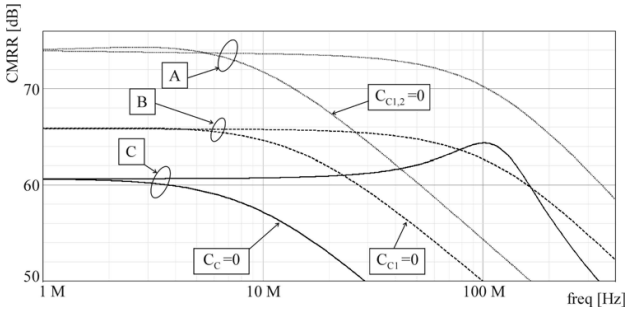

Fig. 7. Comparison of CMRR characteristics for: A circuit in Fig. 5, B circuit in Fig. 6, and C circuit in Fig. 1

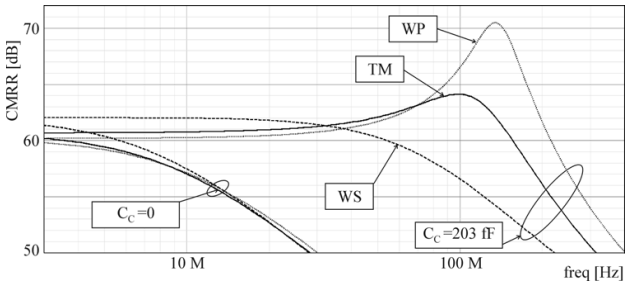

Fig. 8. Comparison of CMRR characteristics of the basic differential pair for technology corners: TM, WP, WS

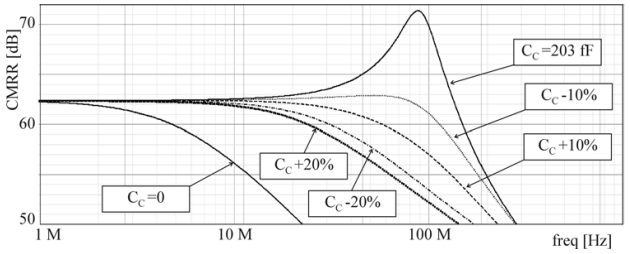

Fig. 9. Comparison of CMRR characteristics of the basic differential pair for selected tolerances of the compensation capacitors

Fig. 1. The frequency of the zero ω_z for the compensated ($C_C = 203$ fF) and uncompensated ($C_C = 0$) variants are: 8.8 MHz and 187 MHz for TM, 8.8 MHz and 240 MHz for WP, and 9.6 MHz and 86 MHz for WS. Figure 9 presents the influence of tolerance of the compensation capacitors for the TM corner. As a reference, the characteristic for the uncompensated ($C_C = 0$) differential pair is depicted. The other plots correspond to:

Table 3
Parameters of simulated OTAs

Parameter	Basic differential pair[a]	OTA in Fig. 5[b]	OTA in Fig. 6[c]
g_m	193 μS	171 μS	169 μS
CMRR(0)	60.7 dB	74 dB	66 dB
f_z	8.8 MHz	16.6 MHz	11.7 MHz
Improved f_z	187 MHz	97 MHz	87 MHz
Input differential capacitance	141 fF	252 fF	200 fF
M_1, M_2	$M_1 = 25$ μm/1 μm	$M_1 = 18$ μm/1 μm, $M_2 = 23$ μm/1 μm	$M_1 = 23$ μm/1 μm, $M_2 = 23$ μm/1 μm
C_{c1}, C_{c2}	$C_{c1} = 203$ fF	$C_{c1} = 127$ fF, $C_{c2} = 230$ fF	$C_{c1} = 230$ fF
$M_3 = 40$ μm/1 μm, $M_4 = 60$ μm/1 μm, $M_5 = 60$ μm/1 μm, $M_{5a} = M_{6a} = 30$ μm/1 μm, $M_{5b} = M_{6b} = 60$ μm/1 μm			

[a] $I_{BIAS} = 1.1\mu A$, [b] $I_{BIAS} = 3.5\mu A$, [c] $I_{BIAS} = 5\mu A$

0%, ±10%, and ±20% tolerances. The zero frequency ω_z is equal to 25 MHz and 5.7 MHz, respectively, for the worst case of the compensated, and the uncompensated circuits. The obtained results show that by using the proposed technique, a considerable broadening of CMRR bandwidth is achievable even under typical tolerances of the compensation capacitors and technology variation.

3.3. Application of tuning to the CMRR improvement. The degree of the CMRR improvement can be significantly increased by applying tuning of η to actual value of the capacitances ratio C_s/C_i. Such a tuning can also compensate change of η due to a technology variation, as discussed in Subsec. 2.2. To explain the principle of operation of the proposed tuning technique let us evaluate the phase shift $\varphi(\omega)$ between the CM input voltage $V_{cm}(\omega)$, and the source voltage $V_s(\omega) = -V_{bs}(\omega)$ define by (2a), which equals to

$$\begin{aligned}\varphi(\omega) = \angle V_s(\omega) &= \tan^{-1}\left(\frac{\omega\,(C_i + C_s)}{g_{m1} + g_{m2} + g_s}\right) \\ &\quad - \tan^{-1}\left(\frac{\omega C_i}{g_{m1} + g_{m2}}\right) \\ &\cong \frac{\omega\,(C_i + C_s)}{g_{m1} + g_{m2} + g_s} - \frac{\omega C_i}{g_{m1} + g_{m2}} \\ &\cong \frac{\omega}{2g_m\,(1+\eta)}\,(\eta C_i - C_s)\,.\end{aligned} \tag{7}$$

The last component in (7) was derived assuming that $\omega < \omega_p$. As indicated by (7) the condition (5) will be automatically fulfilled if the phase shift $\varphi(\omega)$ is nullified. Thus, the tuning system can be accomplished using the master-slave topology [15, 16] presented in Fig. 10. In this system the master OTA is tuned according to the principle (7), using the phase detector which controls the body voltage V_B. Due to all the slave OTAs in a filter are tuned by the same voltage, they will be also tuned to the optimal working conditions.

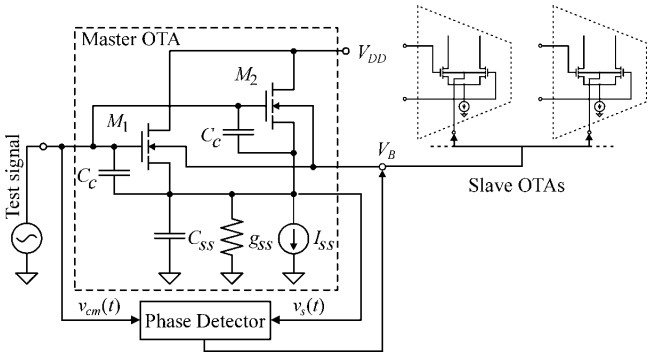

Fig. 10. Proposed automatic tuning system

4. Simulation results

To verify the effectiveness of the improvement technique and operation of the automating tuning, the second order low-pass OTA-C filter, presented in Fig. 11 ($g_{mA} = 100$ μS, $C_A = 9$ pF, $C_B = 4.5$ pF), has been simulated. The OTA shown in Fig. 5 is applied in this filter. The CMRR frequency characteristics were determined for TM, WP, and WS technology corners. The input offset voltage of 3 mV and the capacitance mismatch $\Delta C_{gd}/C_{gd} = 0.05\%$ are set for all OTAs in the filter. The tuning circuit presented in Fig. 10 is used to automatically adjust V_B. As the results of simulations, depicted in Fig. 12 show, the CMRR frequency characteristics are almost flat in the frequency range of up to 200 MHz. The tuning circuit is able to compensate for the technology variation, which results in only 5 dB degradation of CMRR for the WP corner.

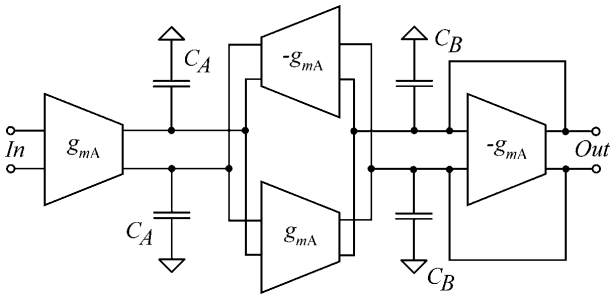

Fig. 11. OTA-C low-pass filter used in simulations

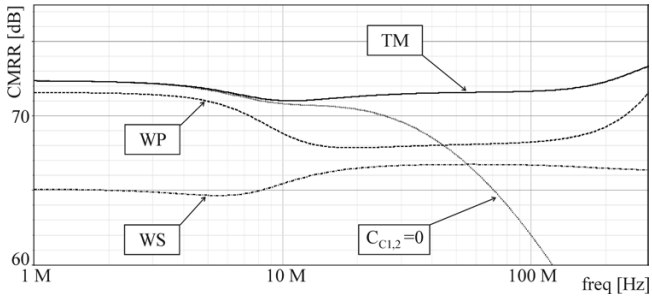

Fig. 12. Comparison of CMRR characteristics of the filter in Fig. 11

The characteristic for the uncompensated OTA ($C_{C1,2} = 0$) is also shown for reference. The filter with the compensated OTA reveals about 10 dB better CMRR at 100 MHz, and over 20 dB improvement at 200 MHz.

5. Conclusions

The presented technique for CMRR improvement is simple and applicable to most OTA-C filters, requiring only slight modification of the filter structures. The technique uses capacitive compensation which is different than used so far [11], because it directly compensates the dominant zero in the characteristic of a differential output current for the CM input signal. The previously known techniques are based on neutralization of a feedforward path via C_{gd} capacitances [11] for DM, which does not effect the CMRR frequency characteristic. The presented analysis and simulation results show that even in the simplest variant of the technique, with no tuning circuit, it broadens the CMRR bandwidth several times under a CMOS process variation and the typical tolerance of circuit components.

REFERENCES

[1] P. Pandey, J. Silva-Martinez, and A. Liu Xuemei, "CMOS 140-mW fourth-order continuous-time low-pass filter stabilized with a class AB common-mode feedback operating at 550 MHz", *IEEE Tran. Circ. Syst. I: Reg. Papers* 56, 811–820 (2006).

[2] V. Saari, M. Kaltiokallio, S. Lindfors, J. Ryynanen, and K.A.I. Halonen, "A 240-MHz low-pass filter with variable gain in 65-nm CMOS for a UWB radio receiver", *Tran. Circ. Syst. I: Reg. Papers* 56, 1488–1499 (2009).

[3] Afzali-Kusha, M. Nagata, N.K. Verghese, and D.J. Allstot, "Substrate noise coupling in SoC design: modeling, avoidance, and validation", *Proc. IEEE* 94, 2109–2138 (2006).

[4] E. Charbon, R. Gharpurey, P. Miliozzi, R.G. Meyer, and A. Sangiovanni-Vincentelli, *Substrate Noise: Analysis and Optimization for IC Design*, KAP, Boston, 2003.

[5] P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, Oxford, 2002.

[6] G. Giustolisi, G. Palmisano, and G. Palumbo, "CMRR frequency response of CMOS operational transconductance amplifiers", *IEEE Tran. Instrument. Measurement* 49, 137–143 (2000).

[7] C. Sripaipa and W.H. Holmes, "Achieving wide-band common-mode rejection in differential amplifiers", *Proc. IEEE* 58, 600–602 (1970).

[8] A.A. Ciubotaru, "Technique for improving high-frequency CMRR of emitter-coupled differential pairs", *IET Electronics Letters* 38, 943–944 (2002).

[9] F. You, S.H.K. Embabi, and E. Sanchez-Sinencio, "On the common mode rejection ratio in low voltage operational amplifiers with complementary N-P input pairs", *IEEE Tran. Circ. Syst. II: Analog Digital Signal Proc.* 44, 678–683 (1997).

[10] P.S. Crovetti and F. Friori, "Finite Common-mode rejection in fully differential operational amplifiers", *IET Electronics Letters* 42, 615–617 (2006).

[11] S. Szczepanski, J. Jakusz, and R. Schaumann, "A linear fully balanced CMOS OTA for VHF filtering applications", *IEEE Tran. Circ. Syst. Part II: Analog Digital Signal Proc.* 44, 174–187 (1997).

[12] S. Koziel and S. Szczepanski, "Dynamic range comparison of voltage-mode and current-mode state-space Gm-C biquad filters in reciprocal structures", *IEEE Tran. Circ. Syst. I: Regular Papers* 50, 1245–1255 (2003).

[13] J.F. Fernandez-Bootello, M. Delgado-Restituto, and A. Rodrıguez-Vazquez, "IC-constrained optimization of continuous-time Gm-C filters", *Int. J. Circ. Theory Applic.* 40, 127–143 (2012).

[14] A. Lewinski and J. Silva-Martinez, "OTA linearity enhancement technique for high frequency applications with IM3 below -65 dB", *IEEE Tran. Circ. Syst. Part II: Express Briefs* 51, 542–548 (2004).

[15] R. Schaumann and Mac E. Van Valkenburg, *Design of Analog Filters*, Oxford University Press, Oxford, 2001.

[16] A. Otin, S. Celma, and C. Aldea, "Continuous-time filter featuring Q and frequency on-chip automatic tuning", *Int. J. Circ. Theory and Appl.* 37, 221–242 (2009).