Low-power adiabatic 9T static random access memory

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Abstract: In this paper, the authors propose a novel static random access memory (SRAM) that employs the adiabatic logic principle. To reduce energy dissipation, the proposed adiabatic SRAM is driven by two trapezoidal-wave pulses. The cell structure of the proposed SRAM has two high-value resistors based on a p-type metal-oxide semiconductor transistor, a cross-coupled n-type metal-oxide semiconductor (NMOS) pair and an NMOS switch to reduce the short-circuit current. The inclusion of a transmission-gate controlled by a write word line signal allows the proposed circuit to operate as an adiabatic SRAM during data writing. Simulation results show that the energy dissipation of the proposed SRAM is lower than that of a conventional adiabatic SRAM.

1 Introduction

As the use of static random access memory (SRAM) L2 caches in current consumer processors tends to substantially increase chip size, reducing the power consumption of SRAM remains a critical area of research. Since logics [1–14] and memories [15–21] employing the adiabatic principle can lower the limit on energy consumption in static complementary metal-oxide semiconductors (CMOSs) devices, such structures show great potential for use in low-power very large-scale integration (VLSI) design. Adiabatic memories can be categorised into a number of types: static [15, 19, 20], latch [16, 17] and dynamic [18].

In this paper, we present a new ultra-low-power adiabatic SRAM. Although the proposed circuit is similar to a 4T-SRAM, it employs two trapezoidal-wave pulses to drastically reduce power dissipation relative to conventional SRAM circuits, as confirmed by our SPICE simulation results.

2 Adiabatic operation in LSI

Fig. 1 shows the main concept underlying adiabatic switching. In the figure, the transitions occurring are considered to be slow enough that the emission of heat is avoided, which is made possible by replacing a DC source by an LC driver, oscillator, clock generator or similar device. If a constant current delivers a charge $Q = C_L V_{dd}$ (where C_L is the parasitic capacitance and V_{dd} is the supply voltage) during the period ΔT, the energy consumption of the channel resistance R is given by

$$\begin{aligned} E_{\text{Adia}} &= \xi P \Delta T \\ &= \xi I^2 R \Delta T \\ &= \xi \left(\frac{C_L V_{dd}}{\Delta T} \right)^2 R \Delta T \end{aligned} \tag{1}$$

where ξ is a shaping factor that is dependent on the clock edge configurations [21]. If the charge value of the load capacitor is DC-modulated, the shaping factor attains a minimum value of $\xi_{\min}$ as 1; for a sinusoidal current, $\xi = \pi^2/8 = 1.23$. It is seen from (1) that, in the theoretical limit where the charging period (ΔT) is infinitely long, the energy consumption is reduced to zero. As the discharging mode operates in the same manner as the charging mode shown in Fig. 1, its energy dissipation is also given by (1).

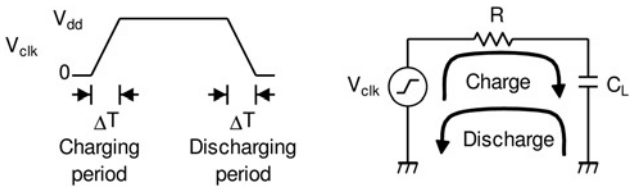

Fig. 1 *Charge/discharge timing RC model of adiabatic switching*

Together, these asymptotically zero-energy charging and discharging actions represent the principle of adiabatic switching [1].

3 Proposed 9T adiabatic SRAM

Figs. 2 and 3 show the structure and timing chart, respectively, of the proposed SRAM. The proposed SRAM cell consists of two high load-resistance p-type metal-oxide semiconductor (PMOS) transistors, MP1 and MP2, and a cross-coupled n-type metal-oxide semiconductor (NMOS), MN1 and MN2. The off-leak current of the PMOS is used to reduce power dissipation in the proposed cell. By using a resistor based on a PMOS transistor, the cell area can be reduced relative to that of a conventional 4T-SRAM by using a poly resistor. To reduce the short-circuit current, NMOS switch MN3 is inserted when data are written in the cell; although the proposed structure limits the decrease in signal voltage on the write (or read) line by using a transmission-gate, if voltage drop

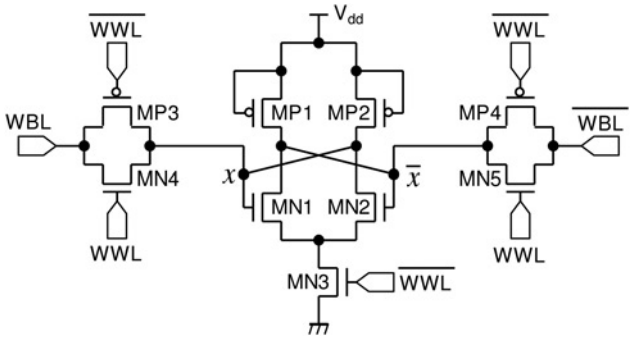

Fig. 2 *Proposed SRAM*

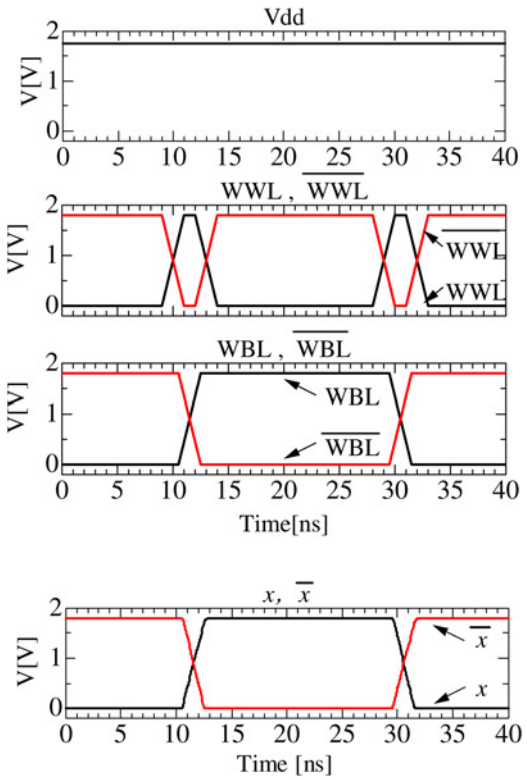

Fig. 3 *Input/output waveforms of the proposed SRAM*

does not really matter, the use of one NMOS switch is preferable from the standpoint of layout area reduction.

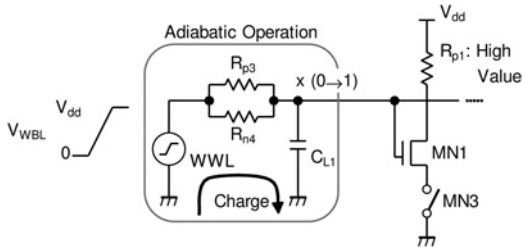

Fig. 4 *Equivalent circuit when node x changes from 0 → 1*

The write mode of the proposed circuit functions as follows: (i) when the WWL ($\overline{\text{WWL}}$) pulse is in the high (low) state, MN4, MN5, MP3 and MP4 are all turned to the ON state. Therefore, nodes x and $\bar{x}$ can be used to change the write-mode and MN3 is turned OFF in order to reduce the short-circuit current; (ii) when the adiabatic signal lines (WBL and $\overline{\text{WBL}}$) are in the on-state, data are written on x and $\bar{x}$; and (iii) when WWL and $\overline{\text{WWL}}$ are low and high, respectively, the MOS transistors MN4, MN5, MP3 and MP4 all become OFF, which switches MN3 to ON, in turn converting the cell hold state to the output data.

The energy reduction effects of the proposed SRAM are summarised as follows.

3.1 *Adiabatic operation when node x changes from 0 → 1*

Fig. 4 shows an equivalent circuit illustrating the change of node x from the 0 to the 1 state, where R_{p3} and R_{n4} are the non-equivalent resistances of MP3 and MN4, respectively, C_{L1} is the parasitic capacitance at node x and R_{p1} is the equivalent resistance of the MOS-based resistor MP1. In this circuit, adiabatic operation clearly occurs on the RC circuit consisting of $R_{p3}//R_{n4}$ and C_{L1}, and therefore the energy dissipation is $E_{\text{Pro}_{0\to1}} = \left(C_{L1}V_{\text{dd}}/\Delta T\right)^2 (R_{p3}//R_{n4})\Delta T$. On the other hand, the energy dissipation of the conventional adiabatic circuit shown in Fig. 5 [19] is given by $E_{\text{Conv}_{0\to1}} = \left(C_L V_{\text{dd}}/\Delta T\right)^2 (R_{n1})\Delta T$, where R_{n1} is the equivalent resistance of NMOS (NM1) on the write word line and C_{L1} is the parasitic capacitance. Comparing E_{Pro} and E_{Conv} shows a clear reduction of power dissipation of $E_{\text{Conv}} - E_{\text{Pro}}$.

3.2 *Adiabatic operation when node x changes from 1 → 0*

Fig. 6 shows an equivalent circuit illustrating x changing from the 1 to the 0 state, which is equivalent to the discharge mode shown in Fig. 1.

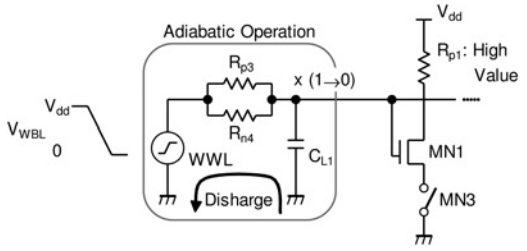

Fig. 6 *Equivalent circuit when node x changes from 1 → 0*

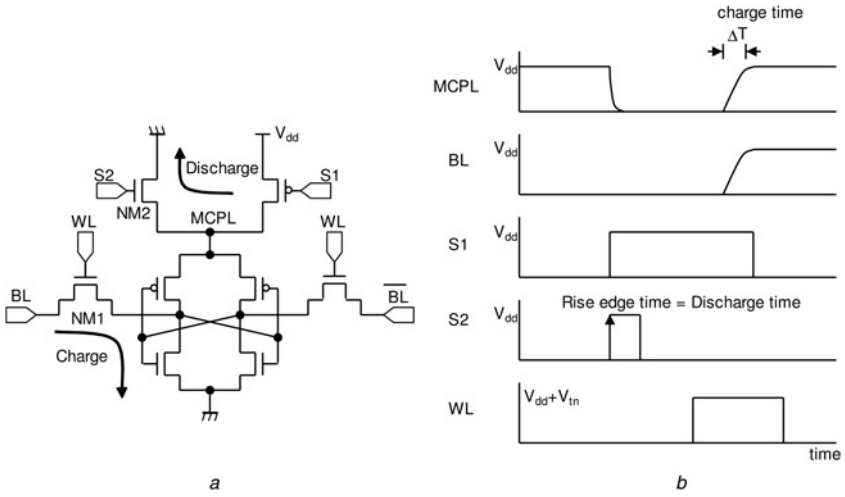

Fig. 5 *Conventional adiabatic logic [19]*
a 8TSRAM
b Timing chart of 8TSRAM

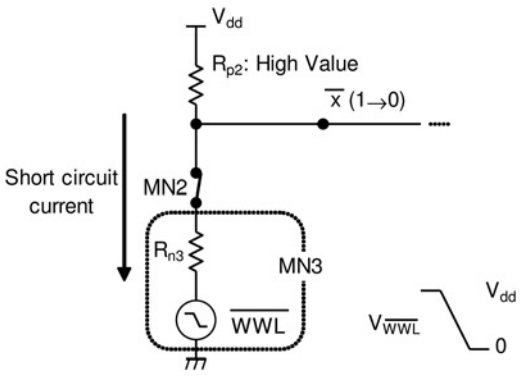

Fig. 7 *Short-circuit current model of the proposed circuit*

Although the energy dissipation of this circuit is clearly $E_{\mathrm{Pro}_{1\to 0}} = \left(C_{L1}V_{\mathrm{dd}}/\Delta T\right)^2 (R_{p3}//R_{n4})\Delta T$, the energy loss of a conventional adiabatic SRAM is nearly equal to $E_{\mathrm{Conv}_{\mathrm{loss}}} = (1/2)CV_{\mathrm{dd}}^2$, as the switching speed of NMOS switch NM2 depends on the rising clock edge, as shown in Fig. 5*b*; in other words, in discharge mode, a conventional SRAM operates like a static CMOS.

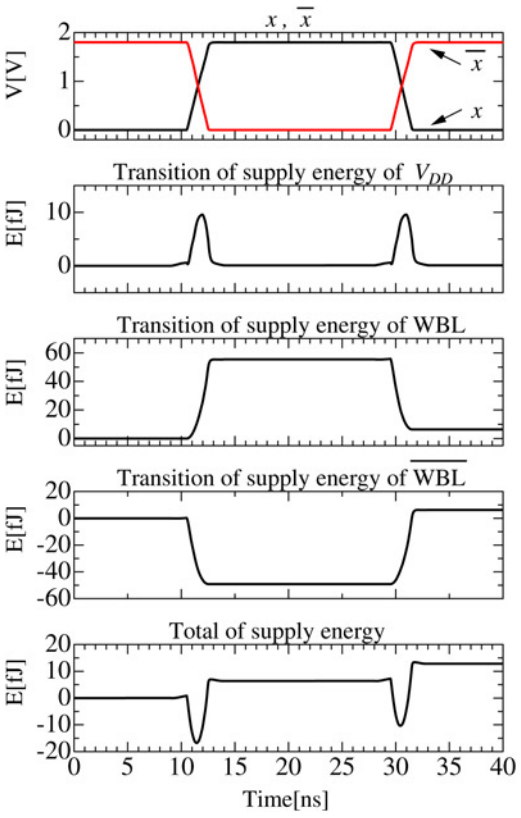

Fig. 8 *SPICE simulation of output waveforms and energy dissipation transition*

Table 1 Comparison of energy dissipation of conventional and adiabatic SRAMs

	Energy, fJ
CMOS 6T SRAM	107.08
adiabatic 8T SRAM [19]	93.58
proposed 9T SRAM	6.40

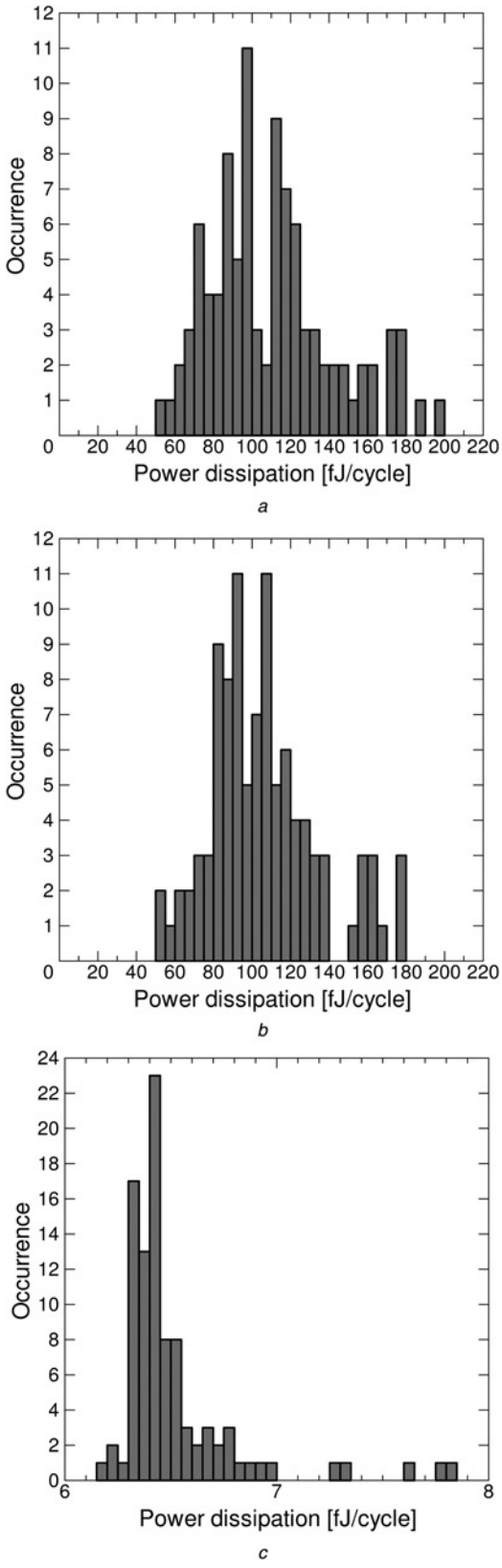

Fig. 9 *Monte Carlo simulation for process variation*
a 6T-SRAM
b Adiabatic [19].
c Proposed Adiabatic

3.3 *Short-circuit current reduction using MOS-based resistor and NMOS switch*

When MN2 is switched to ON in modes (1) or (2) described above, increasing the fall time of trapezoidal-wave $\overline{\text{WWL}}$ will cause a short-circuit current to occur owing to R_{p2}, MN2 and R_{n3}.

Since the switching speed of MN2 depends on the fall time of $\overline{\text{WWL}}$, MN2 operates as if it were in CMOS mode. To reduce this short-circuit current, either the fall time of $\overline{\text{WWL}}$ or the value of R_{p2} can be increased, as shown in Fig. 7. Although using a MOS-based resistor with a low aspect ratio (W/L) can reduce the short-circuit power, doing so increases the chip area and degrades its butterfly curve.

4 Simulation results and implementation

4.1 *SPICE simulation results*

4.1.1 Power dissipation: Both the proposed and conventional SRAMs were simulated with 0.18 µm CMOS process technology using the following parameters and simulation conditions: the aspect ratio of all transistors was $W/L = 0.60/0.18$; the supply voltage was $V_{dd} = 1.8$ V; and the WWL and WBL signal pulses were both trapezoidal waves of amplitude 1.8 V. To measure the power reduction of the SRAMs, we computed the energy dissipation E, defined as

$$E = \int_0^{T_s} \left(\sum_{i=1}^{n} (V_{p_i} I_{p_i}) \right) \mathrm{d}t \tag{2}$$

where $T_s (= 1/f_s)$ is the period of the input signal, V_p is the supply voltage, I_p is the supplied current and the index i denotes the supply sources used. Based on this formulation of E, net energy is flowing into the MOS transistors from the power line.

Fig. 8 shows the output waveform and energy dissipation for each device. From the figure, it is seen that the output of the proposed device represents accurate hold data after writing '1' and '0' and that the energy dissipation of the proposed device is smallest, particularly at the data write time.

The energy dissipation values are summarised in Table 1. These results show that the energy consumption of the proposed circuit is drastically reduced relative to that of a conventional static CMOS 6T-SRAM and an adiabatic 8T-SRAM [19].

4.1.2 Process variation: Since channel length, doping concentration and gate-oxide thickness can cause variations in device characteristics, the stability of the three designs with respect to process variation was investigated further. All three designs were simulated using a commercially available 0.18 µm standard CMOS process and subjected to SPICE-based Monte Carlo simulations of 100 samples with the SRAMs in write mode (as shown in Fig. 8). In these simulations, it was assumed that the fluctuations in threshold voltage, doping concentration and gate-oxide thickness followed normal distributions and a sigma variation of 10% was considered for each parameter. The resulting power consumptions

Table 2 Comparison of adiabatic SRAM families

	[15]	[16]	[19]	[20]	proposed
number of Tr	6	6	8	8	9
area, µm^2	$34\lambda \times 47\lambda$	n.a.	$28\lambda \times 36\lambda$	n.a.	$70\lambda \times 135\lambda$
energy dissipation	1.55 pJ/cycle	47 fJ/cycle	93.6 fJ/cycle	45 fJ/cycle	6.4 fJ/cycle
process	1.2 µm	0.35 µm	0.18 µm	90 nm	0.18 µm
write/read time	10 ns/10 ns	n.a./n.a.	2 ns/n.a.	9 ns/0.42 ns	2 ns/2 ns

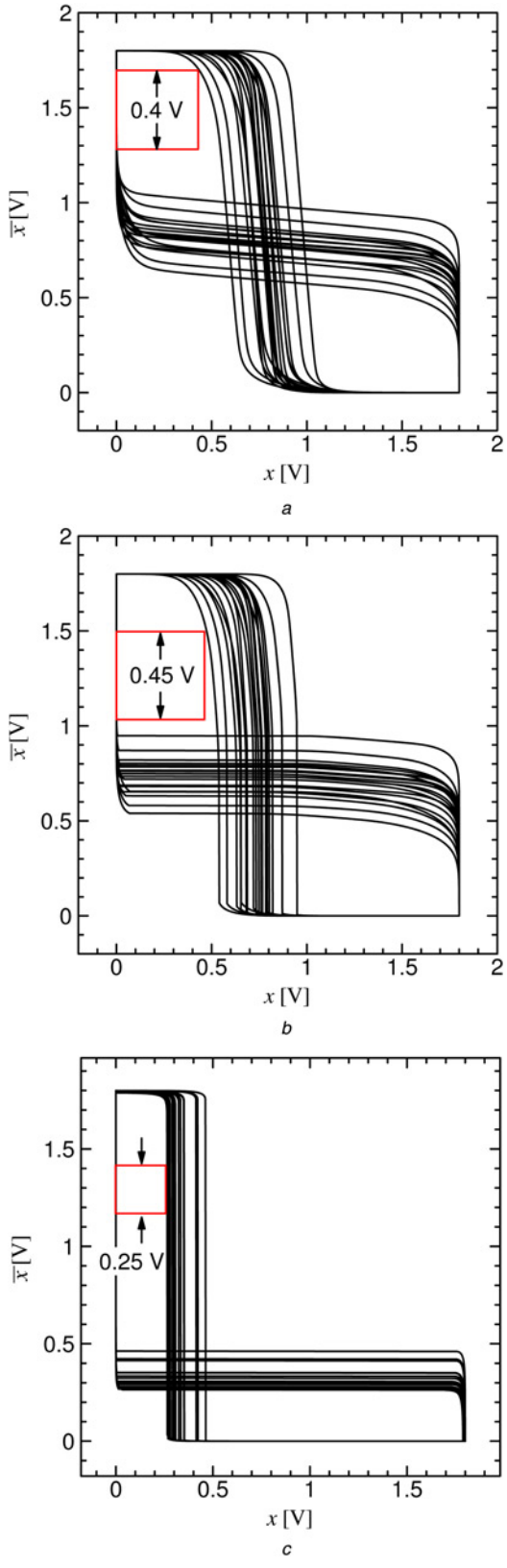

Fig. 10 *SRAM butterfly curves used for measuring SNM values*
a 6T-SRAM
b Adiabatic [19]
c Proposed Adiabatic

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of the 6T, adiabatic 8T [19] and the proposed memory cells are plotted in Fig. 9, with the following results: (a) the conventional static 6T design has a 70-sample (70%) distribution of between 70 and 130 fJ/cycle, (b) the adiabatic 8T design from [19] has a 70-sample distribution of 80 to 125 fJ/cycle, (c) the 82-sample distribution of the proposed SRAM is between 6.2 and 6.8 fJ/cycle, from which it can be concluded that (d) the effect of process variation on the proposed SRAM is smaller than that on the conventional SRAMs.

4.1.3 Static noise margin: Static noise margin (SNM) is a widely used stability criterion, with the butterfly SNM approach being the most popular for characterising the read stability of an SRAM cell. Fig. 10 shows Monte Carlo simulations of butterfly curves for different SRAM cells. From the figure, it is seen that the proposed architecture exhibits a noise margin 54% lower than that of a conventional cell. In future work, we will attempt to expand the noise margin of the proposed circuit.

4.1.4 Supply voltage scaling: Reducing the supply voltage reduces the dynamic power quadratically and the leakage power linearly. Accordingly, supply voltage scaling has remained a major focus in low-power design; however, a reduction in supply voltage may lead to increased memory failures, including read-, hold- or write-failure. Fig. 11 shows the supply voltage scaling results produced by the proposed SRAM, from which it is seen that its supply voltage can be reduced to 0.8 V.

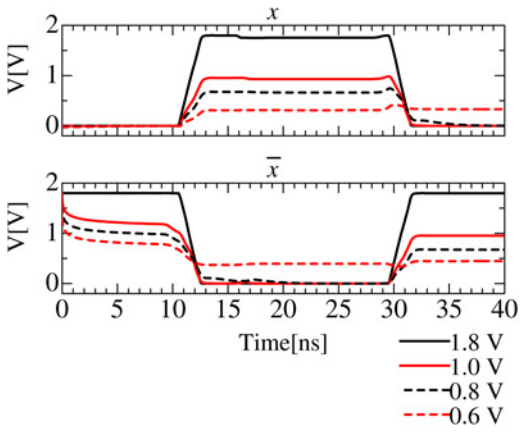

Fig. 11 *Supply voltage scaling results of the proposed SRAM*

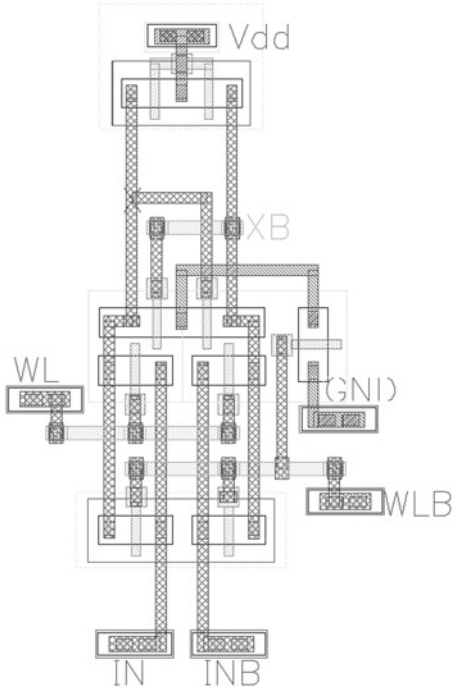

Fig. 12 *CAD layout of the proposed SRAM cell*

4.2 LSI implementation

The layout of a proposed adiabatic 9T SRAM cell with cell dimensions in $\lambda = 0.09$ is shown in Fig. 12. The cell has dimensions $70\lambda \times 135\lambda$ and is implemented in a 0.18 µm CMOS process. From Table 2, which summarises performance comparisons of adiabatic SRAM families, the following can be concluded: (i) the proposed SRAM has a smaller energy dissipation than any conventional SRAM; however (ii) the layout area of the proposed SRAM is four times larger than those of previous adiabatic SRAMs. In the near future, we will have to consider how the layout size of the proposed adiabatic SRAM can be reduced.

5 Conclusion

In this paper, a 9T adiabatic SRAM structure was presented. The proposed SRAM uses two trapezoidal waveforms for adiabatic operation and can reduce the short-circuit current. Our simulation results show that while the energy dissipation of the proposed circuit is improved over that of SRAMs using conventional adiabatic logic by a factor of seven, its architecture has a 54% lower noise margin and layout area that is increased by a factor of four.

6 References

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