Improved dual sided doped memristor: modelling and applications

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Abstract: Memristor as a novel and emerging electronic device having vast range of applications suffer from poor frequency response and saturation length. In this paper, the authors present a novel and an innovative device structure for the memristor with two active layers and its non-linear ionic drift model for an improved frequency response and saturation length. The authors investigated and compared the *I–V* characteristics for the proposed model with the conventional memristors and found better results in each case (different window functions) for the proposed dual sided doped memristor. For circuit level simulation, they developed a SPICE model of the proposed memristor and designed some logic gates based on hybrid complementary metal oxide semiconductor memristive logic (memristor ratioed logic). The proposed memristor yields improved results in terms of noise margin, delay time and dynamic hazards than that of the conventional memristors (single active layer memristors).

1 Introduction

The memristor as a fourth passive fundamental circuit element was first theoretically predicted by Chua [1] in 1971 based on the conceptual symmetry with other passive fundamental elements, such as, resistor, inductor and capacitor. This concept leads to definition of memristor as a circuit element that establishes a relationship between charge (q) and flux (ϕ). The memristive behaviour existed for many years, but the phenomenon was not properly deciphered till 2008, when William [2] and his team at HP Lab demonstrated the physical memristor whose behaviour showed a good agreement with the behaviour predicted by Chua.

The memristor is formally defined as a two terminal passive circuit element, in which the magnetic flux (ϕ) between the terminals is a function of the amount of electric charge q that has been passed through the device, which is explicitly expressed by the equation $d\phi = Mdq$, where M is called the memristance of the device [2]. As an emerging device, memristor exhibits very interesting properties such as non-volatility, good scalability, low power and non-linearity; hence, it has a great potential to lead the futuristic circuits and system architectures. Memristor has found applications in many fields, such as non-volatile memory design [3], neuromorphic computing [4], signal processing [5], control system [6] and analogue circuits [7–9].

To demonstrate and understand the working mechanism of memristor, various realistic physical and mathematical models have been proposed in the recent past [2, 10, 11]. These models either employ an active layer with an excess of oxygen ions or oxygen ion deficient layer created by non-stoichiometric defects. As a result of which, the formation of a less resistive region on one side of the active layer and comparatively high-resistive region on the other side. Major challenges that inhibit the conventional memristor performance for futuristic applications include low operating frequency or switching speed, fast device length saturation and poor R_{off} to R_{on} ratio [2, 12]. To address these limitations, a dual sided doped (two active layer) memristor was proposed in [13]. A linear mathematical model in MATLAB was developed to understand its operation and electrical characteristics. Since linear model has certain limitations, and it does not capture the realistic behaviour of the memristor, a non-linear model and its SPICE model was presented in [14].

In this paper, a novel memristor structure with two active layers (dual sided doping) instead of single active layer (single sided doped) and its non-linear ionic drift model is proposed. Employing two active layers in the proposed memristor significantly enhances the electrical properties because of drifting in both active layers. We developed the SPICE model of the proposed memristor that takes non-linear kinetics of the dopants into account, which particularly of great importance when the physical dimensions shrinking to the nano-scale range. We have compared the $I-V$ characteristics of the proposed memristor using different window functions with the conventional memristor. In addition to this, we have also designed some logic circuits based on hybrid complementary metal oxide semiconductor (CMOS) memristive logic [memristor ratioed logic (MRL)] with the proposed memristor model and found improved results in terms of noise margin, delay time and dynamic hazards than that of the conventional (single active layer) memristor.

In comparison with conventional memristor, the proposed memristor has a better (~3×) saturation frequency (maximum frequency which can be withstand by the memristor, after which memristor behaves like a resistor) that will be a key feature for analogue applications. The larger the device length saturation (~2×), the maximum the length of the device after which it loses its memristive property, a feature that offers less fabrication complexity and improved R_{off} to R_{on} ratio which will provide more immunity to noise.

2 Conventional memristor model

Fig. 1 shows the conceptual view of a conventional memristor and its equivalent electrical circuit from HP Lab [2]. A conventional memristor comprises of a thin TiO_2 layer sandwiched between two nano-wire platinum electrodes having certain length 'D' and its internal state variable 'w' represents the length of the doped region. On the application of external bias voltage (V), the state variable 'w' gets modulated because of charge dopant drifting; hence, the device's total resistivity changes. If the doped region 'w' extends to full length 'D' that is, $w/D = 1$, because of external bias voltage the total resistivity of the device will be dominated by low resistive region and corresponding resistance is called R_{on}. Similarly, on the application of opposite polarity of the bias voltage (V), the undoped region extends to full length of the device, and hence the resistivity of the device is dominated by higher resistive region which leads to off state resistance, R_{off}. A realistic charge controlled memristor model that exhibits this

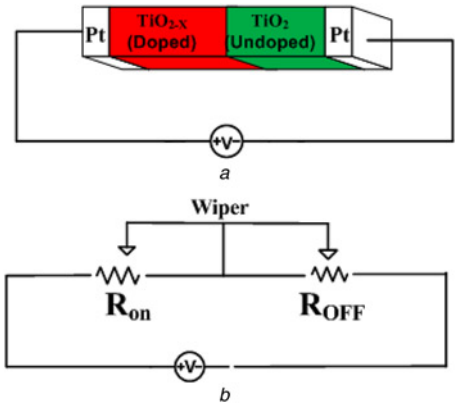

Fig. 1 *Conventional memristor*
a Physical structure of a conventional memristor
b Its equivalent electrical circuit

behaviour is presented by HP Lab [2] is as follows

$$R(w) = R_{\text{on}} \times \frac{w}{D} + R_{\text{off}}\left[1 - \frac{w}{D}\right] \tag{1}$$

$$M[q] = R_{\text{off}}\left[1 - \left[\frac{1}{D^2} \times q(t) \times \mu_v \times R_{\text{on}}\right]\right] \tag{2}$$

where $M[q]$ is the overall memristance of the memristor, R_{off} and R_{on} are the OFF and ON state resistances, μ is the mobility of oxygen ions and 'D' is the device length. From (1) it can be observed that the net memristance of the memristor depends on the charge that passed through the memristor, device length and mobility of oxygen ions.

3 Proposed memristor

The proposed dual sided doped memristor with two active layers can be created by the non-stoichiometric defects in the pure TiO_2 sandwiched in two metal nano-wire electrodes made up of Pt/Al, as shown in Fig. 2*a*. In the top layer, metal excess defects because of anion vacancies have been created; as a result, negative ions were missing from the lattice site, leaving holes which are occupied by the nearby electrons to maintain the neutrality. In this layer, the oxygen concentration is less than that of pure TiO_2, that is, TiO_{2-x}, which reduces the resistivity and increases conductivity of the layer. Similarly, metal deficient defects, because of cation vacancies, have been created at the bottom layer which results into excess of oxygen ions that is, TiO_{2+x}; hence, excess of negative ions also enhance the conductive property of the pure TiO_2 layer [15]. The two active layers TiO_{2-x} and TiO_{2+x} have been separated by a pure TiO_2 layer of high resistivity, as shown in Fig. 2*a*. The total length of memristor is 'D' and depth of doped regions TiO_{2-x} and TiO_{2+x} be 'w_1' and 'w_2', respectively. The equivalent electrical circuit of the proposed device consists of three resistors connected in series represents the resistances offered by three layers TiO_{2-x}, TiO_2 and TiO_{2+x} as indicated by R_{on1}, R_{off} and R_{on2}, respectively, as shown in Fig. 2*b*.

With the application of external forward (top electrode is positive with respect to bottom electrode) bias voltage, the oxygen ions (O^{2+} and O^{2-}) approaches towards centre, thus the active state region will increase and the undoped region decreases. This leads to switch 'ON' the memristor (i.e. the overall resistance is predominant by the 'ON' state resistance). In case of reverse biasing (opposite polarity), the oxygen ions (O^{2+} and O^{2-}) move away from the centre and the boundary will shift in opposite directions; hence, overall resistance (memristance) will be predominant by the 'OFF' state resistance. When the applied external voltage is turned off, there is no further drifting of oxygen ions; as a result, both boundaries were frozen out; hence, memristor remembers the last voltage applied to it. According to Chua [1] and Strukov *et al.* [2], the charge controlled memristance of a memristor can be defined as

$$M(q) = \frac{\mathrm{d}\phi}{\mathrm{d}q} = \frac{(\mathrm{d}\phi/\mathrm{d}t)}{(\mathrm{d}q/\mathrm{d}t)} = \frac{v(t)}{i(t)} \tag{3}$$

where $v(t)$ is the applied voltage and $i(t)$ is the current passing through the memristor. From the equivalent electrical circuit shown in Fig. 2*b*, the instantaneous value of the memristance $M(w)$ can be defined as

$$M(w_1,\ w_2) = R_{\text{on1}} \times \frac{|w_1|}{(D/2)} + R_{\text{on2}} \times \frac{|w_2|}{(D/2)} + R_{\text{off}}\left[1 - \frac{|w_1| + |w_2|}{D}\right] \tag{4}$$

where $M(w)$ is the overall memristance of the proposed memristor, R_{on1} is the ON state resistance for region-1 (top active layer), R_{on2} is the ON state resistance for region-2 (bottom active layer) and R_{off} is the OFF state resistance for region-3. Assume that the state variables $x_1 = (w_1/D/2)$ and $x_2 = (w_2/D/2)$ are the normalised width of the doped regions. Hence, (4) becomes

$$M(x_1,\ x_2) = R_{\text{on1}} \times |x_1| + R_{\text{on2}} \times |x_2| + R_{\text{off}} \times \left[1 - \frac{(|x_1| + |x_2|)}{2}\right] \tag{5}$$

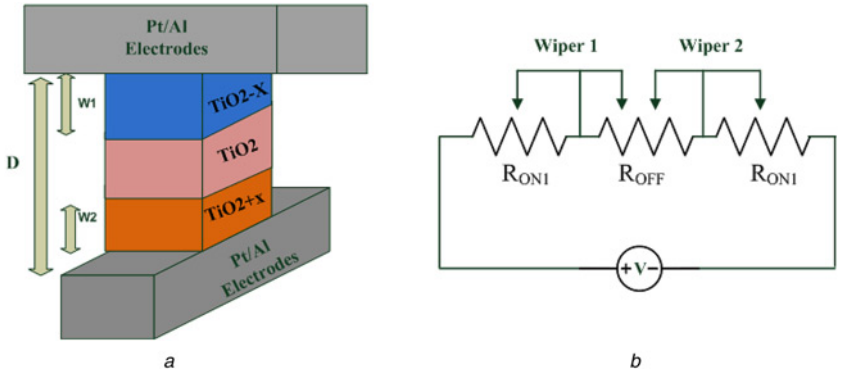

Fig. 2 *Proposed memristor*
a Three-dimensional view of the proposed dual sided doped memristor
b Its equivalent electrical circuit

If we assume the uniform electric field across the device, the width of the doped region depends on the amount of charge that has been passed through the device. Thus, the time derivative of w is a function of current which can be described as

$$\frac{\mathrm{d}w(t)}{\mathrm{d}t} = \mu \times E = \mu \times \frac{R_{\mathrm{ON}}}{D} \times i(t) \tag{6}$$

where $\mathrm{d}w/\mathrm{d}t$ is the speed at which the boundary drifts between the doped and undoped regions, μ is the average mobility of the dopants in presence of current $i(t)$ and R_{ON} is the ON state resistance of the memristor.

Equation (6) leads to a linear ionic dopant drift model of the memristor. The linear model has less complexity, because it assumes that the memristor is ohmic and dopant drift is linear under the electric field. However, this model has several drawbacks as in case of saturation, the width of the active layers will exceed maximum permissible limits; hence, the resistance (memristance) offered by the active layers fall below the specified limits of R_{on1} and R_{on2}. Similarly, in case of depletion (reverse biased), the width of active layers will take negative values which will give erroneous results. In addition, the linear model does not capture the highly non-linear effects of the large electric field inside the memristor [16, 17]. When the generated electric field is small enough, the linear dopant drift model can be used to approximate the dynamics of a memristor. However, the model is invalidated at boundaries $w < 0$ or $w > D$. This is because of the influence of a non-uniform electric field that significantly suppresses the drift of the dopants at the boundaries.

To accurately model the non-linear behaviour of the memristor at comparatively large electric field, which is very common in nano-sized devices, and confine the state variables within the specified boundary, a non-linear mathematical model which incorporates a non-linear window function $f(x)$ to the drift equation that confines the state variable 'x' between their defined boundaries is proposed. Therefore, the state equation of the memristor with non-linear window function $f(x)$ can be written as

$$\frac{\mathrm{d}x(t)}{\mathrm{d}t} = K \times i(t) \times f(x) \tag{7}$$

where K is a constant, $i(t)$ is the current and $f(x)$ is a non-linear window function. The window function compelled the state variable 'x' to become zero at the boundary. For the proposed memristor model, we use two window functions, $f(x_1)$ for region-1 and $f(x_2)$ for region-2. The window functions model the non-linear dopant kinetics in the active layers and return a scalar value based on the coordinate of the device's width w. These window functions also take into account the boundary conditions of the top and bottom electrodes of the device and are capable of imposing non-linear drift over the entire active region of the device. The width of active layers 'w_1' and 'w_2' drifted from $-D/2$ to zero and from zero to $+D/2$, respectively. In terms of normalised width or state variables x_1 and x_2, the state variable 'x_1' will drift from -1 to zero and the state variable 'x_2' will drift from zero to $+1$, as shown in Fig. 3. In the literature, several window functions have been proposed [2, 9, 12] in the recent past to accurately

Fig. 3 *Lateral view of the proposed memristor state variables x_1 and x_2 and their boundary conditions*

model the non-linear dopant kinetics of a memristor. One of the most common and widely adopted window functions for the conventional memristor is as follows [9]

$$f(x) = 1 - (2 \times x + 1)^{2P} \text{ for } 0 < x < D \tag{8}$$

where P is a controlling parameter, which controls the extent of non-linearity in the window function. For higher values of P more non-linearity is introduced in the device. Since the proposed memristor comprises of two active layers, therefore the non-linear effects of both active layers need to be considered allowing charged ions drifting in either direction. The modified state equation (7) for both active layers state variables and their corresponding window functions are as follows

$$\frac{\mathrm{d}x_1}{\mathrm{d}t} = K_1 \times i(t) \times f(x_1) \tag{9}$$

$$\frac{\mathrm{d}x_2}{\mathrm{d}t} = K_2 \times i(t) \times f(x_2) \tag{10}$$

where

$$f(x_1) = 1 - (2 \times x_1 + 1)^{2P} \text{ for } -1 < x_1 < 0 \tag{11}$$

$$f(x_2) = 1 - (2 \times x_2 - 1)^{2P} \text{ for } 0 < x_2 < 1 \tag{12}$$

These window functions ensure zero drifting at the boundaries and maximum drifting rate at the centre, as one can observe in Fig. 4. The major drawback of Joglekar window [9] function is that it suffers from 'terminal state problem'. When the state variables hit any of the boundaries ($w = 0$ or D), the state of the device cannot be further adjusted, in other words, state gets stuck at the boundaries. Hence, the window function proposed by Joglekar exhibits a serious problem for modelling of practical devices. To overcome this model inaccuracy, a different window function is proposed by Biolek *et al.* [12] that allows the memristor to come back from the terminal state problem. The Biolek window function for a conventional memristor is

$$f(x) = 1 - (x - \mathrm{stp}(-i))^{(2P)} \tag{13}$$

where

$$\mathrm{stp}(i) = \begin{cases} 1, & \text{if } i \geq 0 \\ 0, & \text{if } i < 0 \end{cases}$$

where i is the memristor current. A positive current corresponds to increasing width of the doped region and negative current is associated with the decreasing width of the doped region. The depleted (off state) or saturated (on state) device can be brought out of the terminal states when the current reverses its direction. This has been achieved by the steep trough at the extreme boundaries. The Strukov proposed another window function in [2] to develop HSPICE macromodel of memristor. According to the Strukov window function

$$f(x) = x - x^2 \tag{14}$$

the boundary condition at the off state when $x = 0$ is resolved since $f(0) = 0$, whereas it also imposes non-linearity over the bulk of the device. However, this particular window lacks in flexibility, whereas the terminal state problem remains prevalent.

Fig. 4 shows the window function $f(x_1)$ and $f(x_2)$ for regions 1 and 2, respectively, for the proposed model of memristor. It can be observed that both window functions resolve boundary

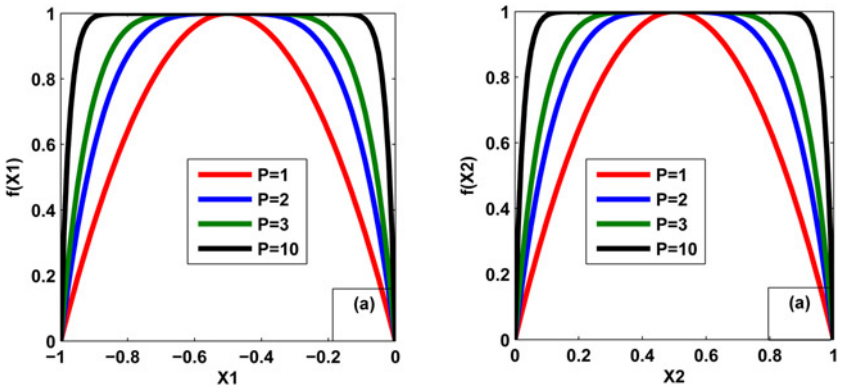

Fig. 4 *Window functions for*
a Region 1
b Region 2

conditions and impose the non-linear drifting over the entire length of the device. Furthermore, the drifting speed of active regions will be maximum at the centre of the region and continuously slows down at both ends. By modulating the value of control parameters (P) it has been observed that for a larger value of P, function becomes more linear.

4 SPICE modelling

To extract electrical characteristics and circuit level behaviour of the memristor, the SPICE model would be an appropriate way to describe real device operation [18]. Moreover, using the model as a sub-circuit, one can guarantee a reasonably high flexibility, scalability and accuracy features [19]. We developed the SPICE model for the proposed memristor based on the mathematical equations derived in the previous section. Fig. 5 shows the schematic representation of mathematical equations (9) and (10) and port equation (5). From the state equations (9) and (10), the derivatives of state variables are the product of three terms, the window functions [$f(x_1)$ and $f(x_2)$], the constant terms (represented by K_1, K_2) and the current $i(t)$. On integration, (9) and (10) give the values of state variables x_1 and x_2, respectively, which update the window functions and modulate the net memristance of the memristor according to port equation (5). The memory effect of memristor is modelled by the feedback controlled integrators. As per boundary conditions, it stores the effects of passing currents and control the memristor resistance by modulating the wiper position. The non-linear drift and influence of the boundary conditions are modelled by the feedback via non-linear window functions $f(x_1)$ and $f(x_2)$. To incorporate the state variables effect in SPICE model after integration, the port equation (5) is modified as

$$M(x_1,\ x_2) = R_{\text{off}} - x_1\left(\frac{R_{\text{off}}}{2} - R_{\text{on1}}\right) + x_2\left(\frac{R_{\text{off}}}{2} - R_{\text{on2}}\right) \quad (15)$$

$$M(x_1,\ x_2) = R_{\text{off}} - x_1 \times \Delta R_{\text{on1}} + x_2 \times \Delta R_{\text{on2}} \quad (16)$$

The SPICE equivalent circuit diagram of mathematical model developed in the previous section is shown in Fig. 6. The relation

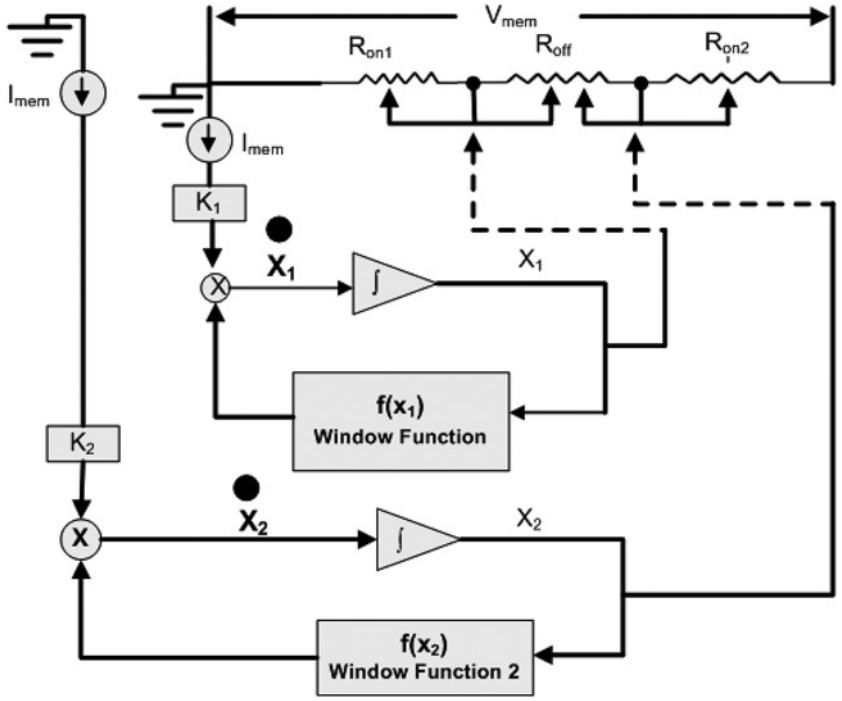

Fig. 5 *Mathematical representation of the proposed memristor for SPICE modelling*

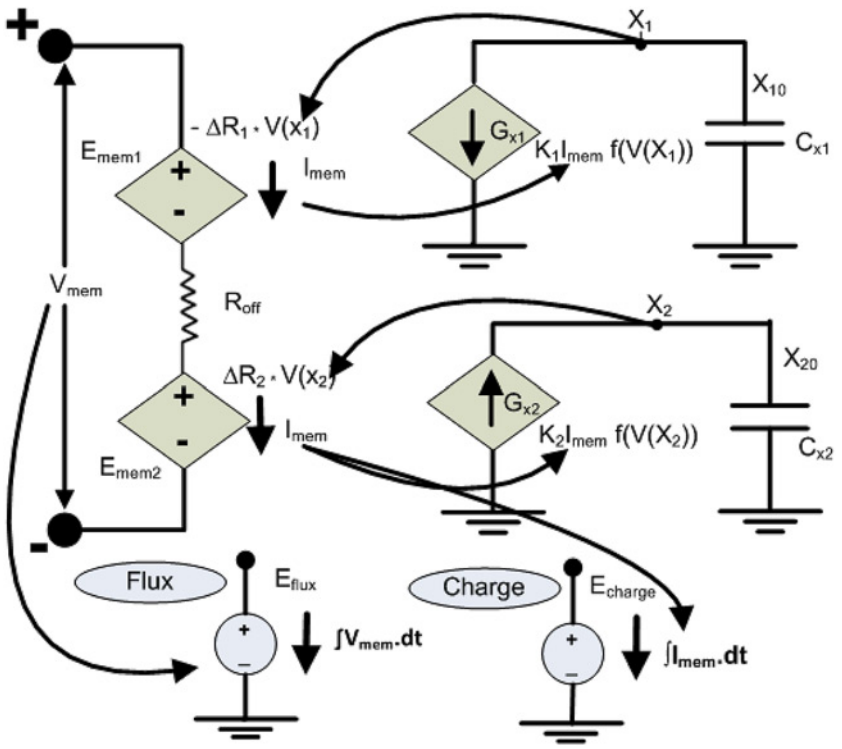

Fig. 6 *SPICE equivalent circuit diagram of mathematical representation shown in Fig. 5*

between the memristor voltage (or flux) and current (or charge) is established on the basis of modified port equation (16). In Fig. 6 the input voltage is given by V_{mem} and I_{mem} is the modelled current passing through the memristor. Equation (16) depicts that there is a resistance R_{off} in series with two voltage dependent voltage sources E_{mem1} and E_{mem2} whose terminal voltage depends on the factor '$x_1 \times \Delta R_{on1}$' and '$x_2 \times \Delta R_{on2}$', respectively. These voltage sources represent both active layers of the proposed memristor. The normalised widths of active layers x_1 and x_2 are the result of integrals of (9) and (10); hence, they are modelled by the voltage across capacitors C_{x1} and C_{x2}, where X_{10} and X_{20} are the initial conditions of the capacitors C_{x1} and C_{x2} that represent the initial values of the normalised width in active regions 1 and 2, respectively. The feedback loops in Fig. 5 are modelled as the voltage dependent current sources G_{x1} and G_{x2}, whose values depend on the voltage across the capacitors. The flux and charge relationship can be established by calculating the time integral of voltage V_{mem} for flux and time integral of current I_{mem} will yield the charge, as shown in Fig. 6. For SPICE implementation, we use a sub-circuit described as a net-list with all the components, as shown in Fig. 6, such as ON resistances R_{on1} and R_{on2}, OFF resistance R_{off}, device length (D), mobilities in active regions 1 and 2 as μ_{v1} and μ_{v2} and parametric constant P. In this paper, for numerical SPICE simulations, following parameters are passed: $D = 10$ nm, $V = 0.5\sin(2*pi*f*t)$, $f = 1$ Hz, $t = 5$ s, $\mu_{v1} = \mu_{v2} = 10$ fm^2/Vs, $R_{off} = 180$ KΩ, $R_{on1} = R_{on2} = 50$ Ω, $P = 10$ and $R_{init1} = R_{init2} = 17.5$ Ω.

To validate the functioning and modelling of the proposed memristor, we have performed SPICE simulations and compared the results with conventional memristor for different window functions. The $I - V$ characteristics exhibiting the hysteresis behaviour is an important property of a memristor. Therefore, under iso-parameters, we first simulated the hysteresis behaviour of both memristors for sinusoidal input using different window functions. This process can also be referred to as calibration of the proposed SPICE model with the existing models. Fig. 7*a* shows the $I - V$ characteristics of the conventional and proposed memristors using Joglekar window function. From the simulation results, as shown in Fig. 7*a*, it can be observed that the response of the proposed memristor shows better hysteresis compared to the conventional memristor [12]. For quantitative analysis, we have measured the current ratio (I_{max}/I_{min}) from the hysteresis curve of positive lobe assuming that the device is symmetric for both memristors under different window functions. A higher current ratio will provide better distinguishability of logic states and can be a potential memristor for

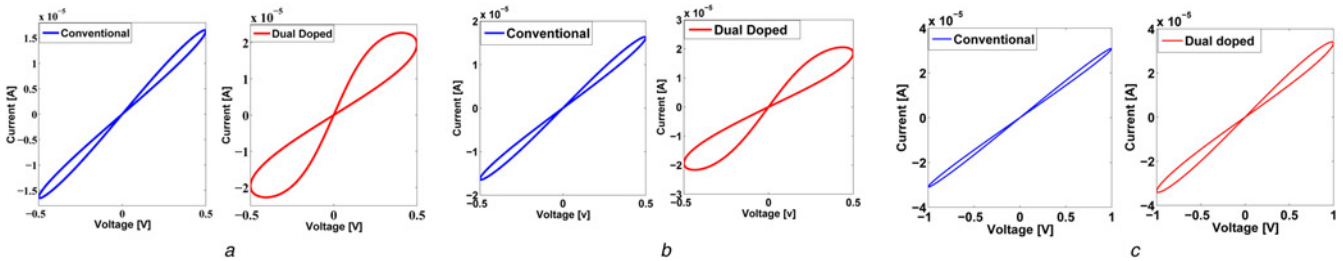

Fig. 7 *I–V characteristics (hysteresis curves) of conventional and dual sided doped memristor for sinusoidal input and different window functions*
a Joglekar window function
b Biolek window function
c Strukov window function

Table 1 Current ratio (I_{max}/I_{min}) for different window functions

Window functions	I_{max}/I_{min}(conventional)	I_{max}/I_{min}(proposed)
Joglekar	0.4189	1.3
Biolek	0.237	0.485
Strukov	78.81	86.83

memory as well as digital logic applications. From Table 1, it can seen that the proposed memristor for Joglekar window function offers a significant 3× improvement in current ratio or logic distinguishability.

Similarly, $I-V$ characteristics comparison of the conventional and proposed memristors using the Biolek and Strukov window functions are shown in Figs. 7*b* and *c*. For both window functions, proposed (dual sided doped) memristor exhibits better hysteresis as compared with conventional memristor. However, Strukov window function has its own limitations and shows poor hysteresis curves in both memristors. The Biolek window function also exhibits good hysteresis curve and offers 2× improvement in current ratio or logic distinguishability as compared with conventional memristor, can be seen in Table 1. Therefore, the proposed memristor and its SPICE modelling offers good agreement with the existing models and shows significant improvement in the $I-V$ characteristics and current ratio or logic distinguishability.

5 Digital applications

Digital applications of memristor open numerous opportunities and challenges, although several approaches have been proposed in literatures for the use of memristive devices as logic gates [20–22]. In this paper, we described the MRL proposed in [21]. In this logic style, the logic is represented as a voltage, consistent with the CMOS logic style. The memristive devices are used only for computation purposes and not for storing logical states. Similar to the standard CMOS logic style, the topology of the circuit determines the logical function. To implement an OR and AND logic gates with MRL style, we use two memristors connected in series with opposite polarity, as shown in Fig. 8. The output is taken from the common terminal of the memristive devices and the signals on the other terminal of each memristive devices are the inputs for the logic gates. Owing to the polarity of the memristors in OR and AND logic gates, when the current is supplied at any input terminal the memristor resistances change and the change in resistance would be positive for OR gate and negative for AND gate. In other words, for OR gate the resistance will decrease and in case of AND gate the corresponding resistance will be increased on applying the signals at input terminals.

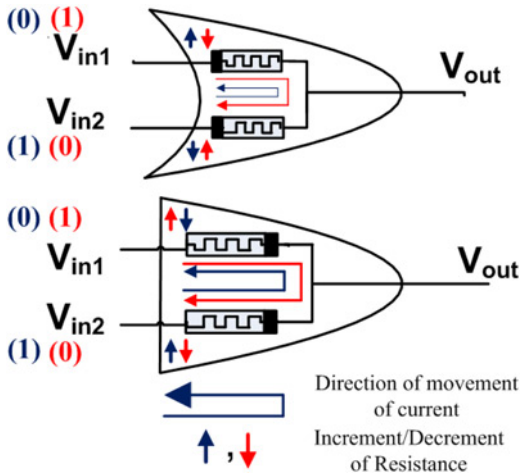

Fig. 8 *Schematic diagrams of OR and AND gates using memristors*

Both OR and AND logic gates react similarly for identical set of inputs. Hence, for identical inputs there is no voltage drop across the memristors and no current will flow in the circuit. So that the output voltage will exactly follow the input voltage. When both inputs are at logic zero, the output will be zero and when both inputs are at logic one, the output will be in high logical state. In case of different input states, that is one input high and another is in low state or vice-versa, the current will flow from high-voltage state (logical one) to low-voltage state (logical zero), and this will modulate the resistance of the memristors, as shown in Fig. 8. For example, let us consider the inputs are at logic '1' and '0' states. In case of an OR gate, the resistance connected to the logic '1' (M_1) will be decreased and the resistance connected to the logic '0' (M_2) will increase, as shown in Fig. 9*a*. Similarly, if the same inputs are applied to the AND gate, the resistance of the memristor which is connected to logic '1' will increase and the resistance of the memristor which is connected to the logic zero will decrease, as shown in Fig. 9*b*. At the end of the computation process both resistances of memristive devices will attain to their minimum and maximum values, which will be approximated as R_{on} and R_{off}, respectively. The output voltage of the logic gate is computed by the potential division across the two resistances of the memristor. The output voltage for an OR gate (assuming $R_{off} \gg R_{on}$), when dissimilar inputs are given can be computed by

$$V_{out,\,OR} = \frac{R_{off}}{R_{off}+R_{on}} \times V_{high} \simeq V_{high} \tag{17}$$

Similarly, the output voltage for an AND gate is given by

$$V_{out,\,AND} = \frac{R_{on}}{R_{off}+R_{on}} \times V_{high} \simeq 0 \tag{18}$$

For the output voltage calculations, it is assumed that the initial resistance of both memristive devices has no effect on the output. However, initial resistances only affect the delay when dissimilar inputs are applied. The delay is also dependent on the voltage level and relatively low voltage increases the delay. Figs. 10*a* and *b* show the dynamic behaviour of AND gate using conventional and proposed model of memristors, respectively. The transient response for different input combinations of memristive AND gate shows the dynamic hazards when input changes from logic level '0' to '1' or '1' to '0'. The SPICE simulation shows that for a given input voltage swing from 0 to 4 V, the output rail to rail voltage for an AND gate with conventional memristor is recorded as 3.42 V and that of the proposed model is 3.96 V. Hence, there should be an improvement of rail to rail voltage from 85.5 to 99%, which will improve the noise margin. A higher value of noise margin will indicate that the device is less susceptible to noise, and hence ensures greater reliability in comparison with previous logic gates based on conventional memristor.

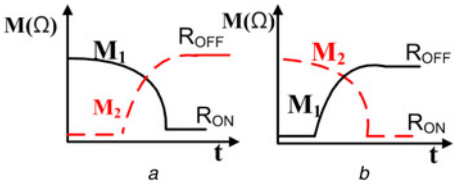

Fig. 9 *Change in resistance of the memristive devices under dissimilar inputs for*
a OR gate
b AND gate

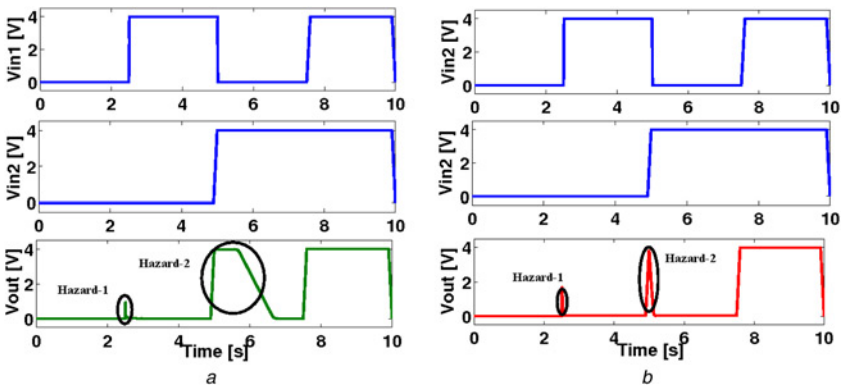

Fig. 10 *Dynamic behaviour of AND gate with hazard-1 and hazard-2*
a Conventional
b Proposed memristor

In digital systems, logic hazards are the manifestation of a problem in which changes in the input variables do not change the output correctly because of some form of delay caused by logic gates. Dynamic hazards for a logic gate occur when the output voltage level does not remain in correct logic value, even if the input voltage change does not call for the change in output. One indicative of dynamic hazards is the duration for which output gives incorrect (ambiguous) output logic level. For the AND gate logic, if the input combinations change such that the output is at zero and it should remain at logic zero, but the output shows a positive spike of an ambiguous logic level, this behaviour of logic gate is named as hazard 1 (as shown in Figs. 10*a* and *b*). For example, if input changes from level (0, 0) to (0, 1), the AND gate output should be zero for both cases, whereas output is showing a small positive spike. Similarly, if the input combinations change such that the output is at zero and it should remain at logic zero, but before settling to logic level zero the output changes to logic level one for a short period of time and then it settles at logic level zero; this behaviour of logic gate where output shows incorrect logic level before settling to the correct logic level is termed as hazard 2 (as shown in Figs. 10*a* and *b*). For example, if input changes from level (0, 1) to (1, 0), the AND gate output should be zero for both cases, whereas output is showing a logic level one for some duration.

The duration for hazard 1 for the AND gate logic using conventional memristors is 0.16 s, whereas that of the proposed memristors duration is 0.08 s. There is significant reduction of 50% in the duration of hazard 1 for the proposed memristors over the conventional one. The duration for hazard 2 for the AND gate logic using conventional memristors is 1.83 s, whereas that of the proposed memristors is 0.25 s. In other words, duration of hazard 2 using proposed memristors is reduced by a factor of ∼7× compared with the conventional memristors. It leads to the improvement in switching behaviour and dynamic power saving for the proposed memristors logic AND gate. The estimated performance parameters for memristive AND gate have also been summarised in Table 2.

Figs. 11*a* and *b* show the dynamic behaviour of an OR gate using conventional and proposed model of memristors, respectively. It can be observed that the proposed model of memristors provides better rail to rail voltage (3.98 V in comparison with 3.96 V of conventional memristor) and hence better noise margin. Corresponding to hazard 1 and hazard 2 occurring in AND gate, OR gate logic exhibits only hazard 1 when input combination changes such that the output should remain at logic 1, but it goes low to some ambiguous logic level for a short duration. The duration for hazard 1 for OR gate logic is 1.76 s for the conventional memristor-based OR gate, whereas it is 0.24 s for the proposed memristors. There is a significant reduction in the duration of hazard 1 for an OR gate

Table 2 Performance parameters for memristive AND gate

Parameters	Conventional	Proposed
R–*R* voltage, (V)	3.4210	3.9605
hazard-1, (s)	1.83	0.25
hazard-2, (s)	0.16	0.08

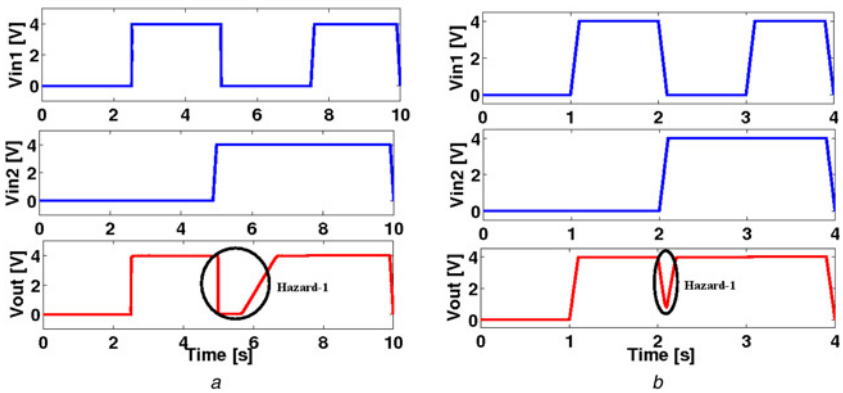

Fig. 11 *Dynamic behaviour of OR gate with hazard-1 and hazard-2*
a Conventional
b Proposed memristor

Table 3 Performance parameters for memristive OR gate

Parameters	Conventional	Proposed
R–R voltage, (V)	3.96	3.98
hazard-1, (s)	1.76	0.24
hazard-2, (s)	—	—

by a factor of ∼7× for the proposed memristors. Hence, an OR gate logic also shows the improvement in switching behaviour as a result saving in dynamic power for the proposed memristors. The estimated performance parameters for memristive OR gate have been tabulated in Table 3.

6 Conclusion

We have proposed a dual sided doped memristor having two active layers and developed its SPICE model. Two active layers in the proposed memristor significantly improve electrical properties, such as pinched-hysteresis and saturation frequency, compared to conventional single active layer memristors. The developed SPICE model incorporates non-linear mechanism using different window functions and exhibits excellent agreement with existing single active layer memristors. In addition to that, a comparative study was carried out for the digital logic gates of single sided and dual sided doped memristors. From the simulation results, we observed that the proposed model has greater noise margin; hence, better reliability, less propagation delay which lead to faster switching and improved dynamic hazards in comparison with that of the conventional memristors. These improved characteristics may provide greater flexibility to design circuits using the proposed memristor.

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