

Minimum jitter-based adaptive decision feedback equaliser for giga-bit-per-second serial links

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Abstract: This study presents a minimum jitter-based adaptive decision feedback equaliser (DFE) for giga-bit-per-second (Gbps) serial links. The adaptation in search for the optimal tap coefficients of DFE is carried out with the objective to minimise data jitter at the edge of data eyes. Jitter minimisation is achieved by adjusting the slope of the DFE that counteracts that of the channel. The effectiveness of the proposed adaptive DFE is evaluated by embedding the DFE in a 2 Gbps serial link. The data link is analysed using Spectre from Cadence Design Systems with BSIM4 device models. Simulation results demonstrate that the proposed adaptive DFE is capable of opening closed data eyes with 83% vertical opening, 68% horizontal opening and 16% data jitter over 1 m FR4 channel while consuming 15.45 mW.

1 Introduction

The explosive growth of data processed by digital systems demands that data be transmitted over wire channels at giga-bit-per-second (Gbps). Increasing the number of parallel links undoubtedly improves effective channel bandwidth, its effectiveness, however, is severely undermined by high routing cost and deteriorating data skew [1]. Inter-chip and point-to-point on-chip data links over long interconnects are most achieved using serial links where data and clock are transmitted simultaneously via a single channel. The data rate of serial links is limited by inter-symbol interference (ISI) arising from channel imperfections including finite bandwidth, reflection and cross-talk. ISI manifests itself as both pre-cursors and post-cursors that span beyond the temporal boundary of one symbol time with latter typically dominating. To remove post-cursors, the most widely used method is decision feedback equalisation (DFE) introduced by Austin in 1967 [2]. Fig. 1 illustrates the operation of a 3-tap DFE. The slicer slices v_s at the main cursor and the result of the slicer passes through three delay stages of unit-interval (UI) delay. The output of the j th delay stage is multiplied by weight factor c_j such that $v_{in,j} = c_j v_{k-j}$ where $v_{in,j}$ is the j th post-cursor and v_{k-j} is the j th past decision of the slicer is satisfied. The temporally distributed feedback signal $v_f = v_{in,1}u(k-1) + v_{in,2}u(k-2) + v_{in,3}u(k-3)$ where $u(k-r)=1$ if $k=r$ and 0 otherwise is subtracted from v_{in} such that $v_s[k]=0$ at $k=1, 2, 3$. As a result, the first three post-cursors of v_s are removed ideally. The uncertainty of the characteristics of channels requires that weight factor c_j be set in accordance of the characteristics of the channels such that a complete removal of the post-cursors can be achieved [3]. In [4], the optimal tap coefficients are obtained by minimising the power of the difference (error) between the output and input of the slicer, that is, the least mean square (LMS) of the error. The j th optimal tap coefficient is obtained using iterative operation $c_{j,k+1} = c_{j,k} + h\varepsilon_k v_{k-j}$ where $j = 1, 2, \dots, N$, N is the number of the taps of DFE, $c_{j,k+1}$ and $c_{j,k}$ are the coefficients of tap- j in steps $k+1$ and k , respectively, and h is the step size used to adjust the tap coefficients in each iteration step. LMS-based DFE is difficult to implement because of the need for ε_k and v_{k-j} , which can only be obtained using analogue-to-digital converters. Sign-sign LMS (SS-LMS)-based DFE that only needs the signs of ε and v_{k-j} and obtains the optimal tap coefficients using iterative algorithm $c_{j,k+1} = c_{j,k} + h \text{sign}[\varepsilon_k] \text{sign}[v_{k-j}]$ where $\text{sign}[x] = 1$ if $x \geq 0$ and -1 otherwise is proven to be an efficient and yet effective alternative of LMS-based DFE [5].

Since when data eye, that is, the waveform of the input of the slicer, is fully open, the difference between the output and input of the slicer is minimised. This observation suggests that the eye-opening of received data can also be used to guide the search for optimal DFE tap coefficients. As eye-opening is directly related to bit error rate (BER), for example, the larger the eye-opening, the better the BER, eye-opening-monitor (EOM)-based DFE provides an explicit link between DFE operation and BER. Both one-dimensional (1D) [6–10] and 2D EOMs [11–14] have been reported. A common drawback of EOM-based DFE is the lack of a tight constraint on data jitter, arising from duty-cycle distortion, switching noise and ISI, and having a detrimental effect on both the vertical and horizontal openings of data eyes. For example, 1D EOMs only focus on the vertical opening at the centre of data eye and do not have any constraint on data jitter. Although 2D EOMs do have a constraint on data jitter, it is lower-bound by the vertical eye-opening at the centre of the data eye, as illustrated

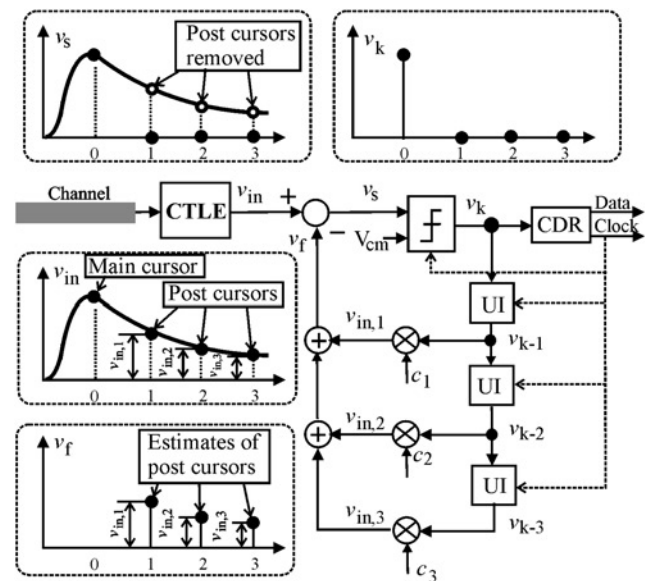


Fig. 1 3-tap DFE. Continuous-time linear equaliser is used to boost data symbols prior to slicing
This step is necessary to ensure that v_s is large enough such that the decision made by the slicer is most likely correct

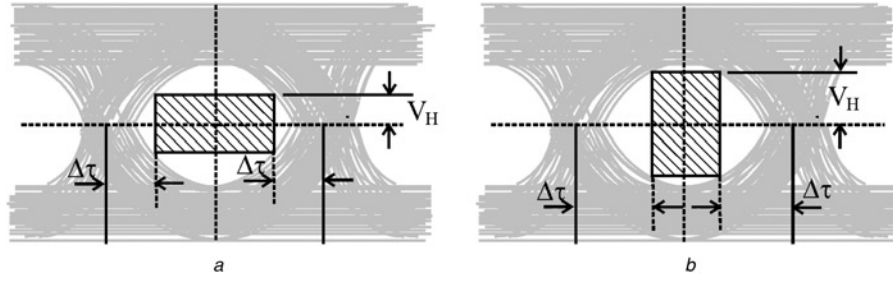


Fig. 2 Jitter constraint is lower bound by the vertical eye-opening at the centre of data eye
It is seen that the smaller the vertical opening V_H , the tighter the jitter constraint
a smaller vertical eye-opening, better jitter constraint
b Larger vertical eye-opening, poorer jitter constraint

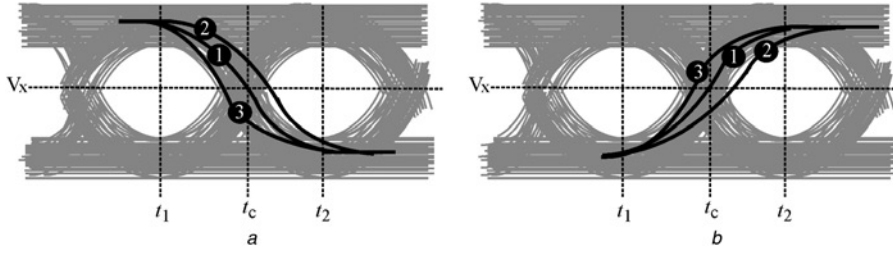


Fig. 3 Jitter-based error detection
a High-to-low transitions
b Low-to-high transitions

graphically in Fig. 2. It is highly desirable from a clock recovery point of view to minimise data jitter without sacrificing eye-opening. In [15], jitter information at the edges of data eyes is obtained by employing a set of temporally spaced samplers that sample the transition edge of the eyes at uniformly incremented time instants. Although effective, this approach is power hungry especially when the number of samplers is large. The dual-mode adaptive DFE proposed in [16] consists of a data DFE for maximising the vertical opening of data eyes and a jitter DFE for minimising the jitter at the edges of data eyes.

This paper presents a jitter-based adaptive DFE for Gbps serial links. The adaptation in search for the optimal tap coefficients of DFE is carried out with the objective to minimise data jitter at the edge of data eyes. Jitter minimisation is achieved by adjusting the slope of the DFE that counteracts that of the channel. The rest of

this paper is organised as follows: Section 2 details the principle and implementation of the proposed maximum jitter adaptive DFE and simulation results that validates the effectiveness of the DFE. This paper is concluded in Section 3.

2 Jitter-based adaptive DFE

2.1 Algorithm

The detection of whether the minimum data jitter at the edges of received data is achieved or not is performed by comparing the voltage of received data with their common-mode voltage V_x at t_1 , t_c and t_2 where $t_1 = t_c - T_s/2$, $t_2 = t_c + T_s/2$, t_c is threshold-crossing time instant and T_s is the symbol time, as shown in Fig. 3:

- (1) If $V_s(t_1) > V_x$ and $V_s(t_2) < V_x$, it is a high-to-low transition (Fig. 3a).
 - If $V_s(t_1) > V_x$ and $V_s(t_c) = V_x$ (Trace 1), the desirable trace is obtained and no error is flagged.
 - $V_s(t_1) > V_x$ and $V_s(t_c) > V_x$ (Trace 2), the slope of the rising edge is too small. An error is flagged.
 - If $V_s(t_1) > V_x$ and $V_s(t_c) < V_x$ (Trace 3), the slope of the rising edge is too large. An error is flagged.
- (2) If $V_s(t_1) < V_x$ and $V_s(t_2) > V_x$, it is a low-to-high transition (Fig. 3b).
 - If $V_s(t_1) < V_x$ and $V_s(t_c) = V_x$ (Trace 1), the desirable trace is obtained. No error is flagged.
 - If $V_s(t_1) < V_x$ and $V_s(t_c) < V_x$ (Trace 2), the slope of the rising edge is too small. An error is flagged.
 - $V_s(t_1) < V_x$ and $V_s(t_c) > V_x$ (Trace 3), the slope of the rising edge is too large. An error is flagged.

The preceding analysis reveals that the error signal indicating whether the slope of the transition is too small or too large can be generated using elementary logic. The tap coefficients of DFE can therefore be updated using an iterative algorithm similar to SS-LMS: $c_{j,k+1} = c_{j,k} + h\varepsilon_k \text{sign}[v_{k-j}]$ where ε_k is the error in step k . The adaptive engine (AE) shown in Fig. 4 first determines the

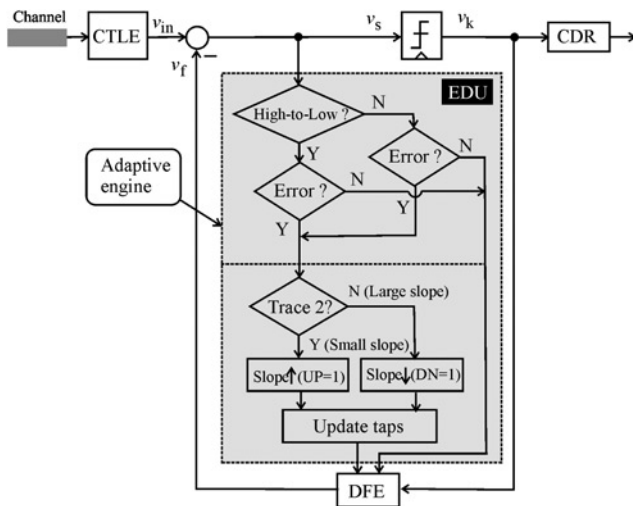


Fig. 4 AE of maximum jitter adaptive DFE

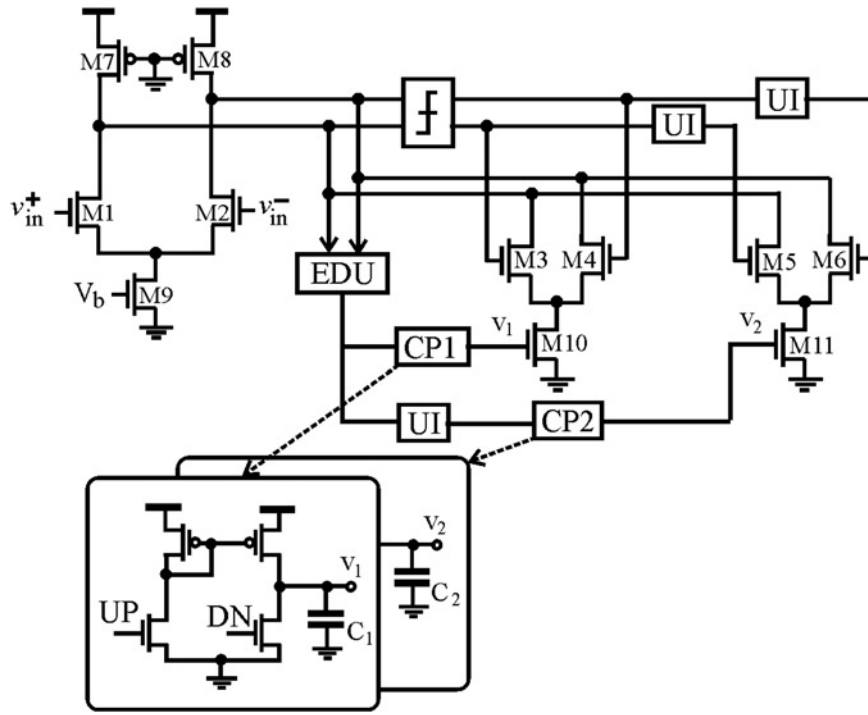


Fig. 5 Configuration of jitter-based adaptive DFE

type of the transition, it then rules whether the slope of the transition is too large or too small. If it is too large, DFE counteracts it by discharging the capacitors subsequently v_1 and v_2 . This in turn lowers the tap coefficients and weakens DFE equalisation. Otherwise, it increases the tap coefficients and strengthens DFE equalisation.

The amount of the adjustment of v_1 and v_2 subsequently that of tap coefficients is set with the following considerations: if the adjustment is too small, the equalisation action of the DFE will be too weak to be effective. On the other hand, if the adjustment is too large, the equalisation action of the DFE will be too strong, resulting in undesirable oscillation subsequently a long adaption process. The value of the capacitors must also be chosen with care. If the capacitances are too large, the output voltage will not change fast enough to provide an appropriate voltage to DFE, resulting in a slow adaptation process. On the other hand, if the capacitances are too small, a large voltage fluctuation will exist, which will in turn have a negative effect on the search for the

optimal coefficients of DFE. The voltage incremental step for tuning the coefficient of tap-1 is set to be five times that for tuning the coefficient of tap-2. This is achieved by setting $C_1 = 1$ pF and $C_2 = 5$ pF. Note that although $C_2 = 5C_1$ and the same error ϵ_k is used for tap-1 and tap-2, the iterative adjustments of tap-1 and that of tap-2 are independent of each other. This is because $c_{1,k+1} = c_{1,k} + h\epsilon_k \text{ sign}[v_{k-1}]$ and $c_{2,k+1} = c_{2,k} + h\epsilon_k \text{ sign}[v_{k-2}]$. The difference of v_{k-1} and v_{k-2} ensures that c_1 and c_2 are adjusted independently.

2.2 Implementation

The configuration of the proposed jitter adaptive DFE with two taps is shown in Fig. 5. The DFE consists of a differential amplifier to boost received signal prior to slicing, a slicer implemented using a three-stage clocked comparator capable of minimising duty-cycle distortion and kick-back [17–19], several clocked delay units, two

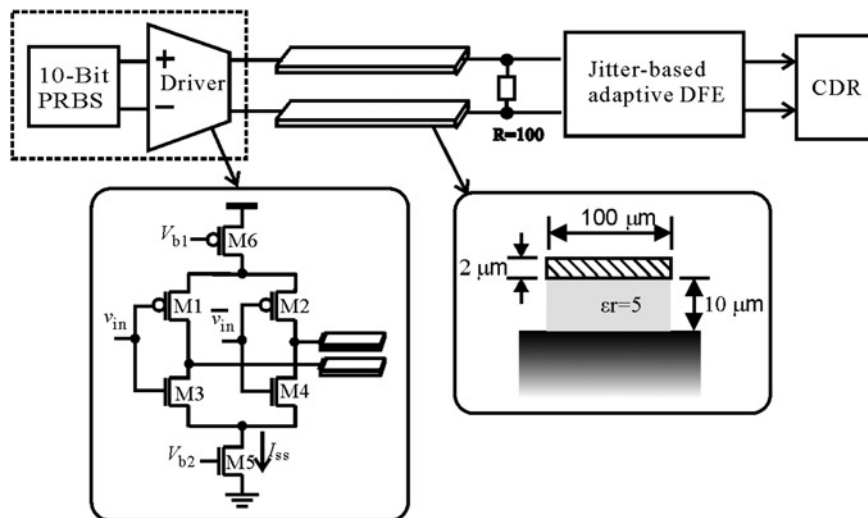


Fig. 6 Test bench

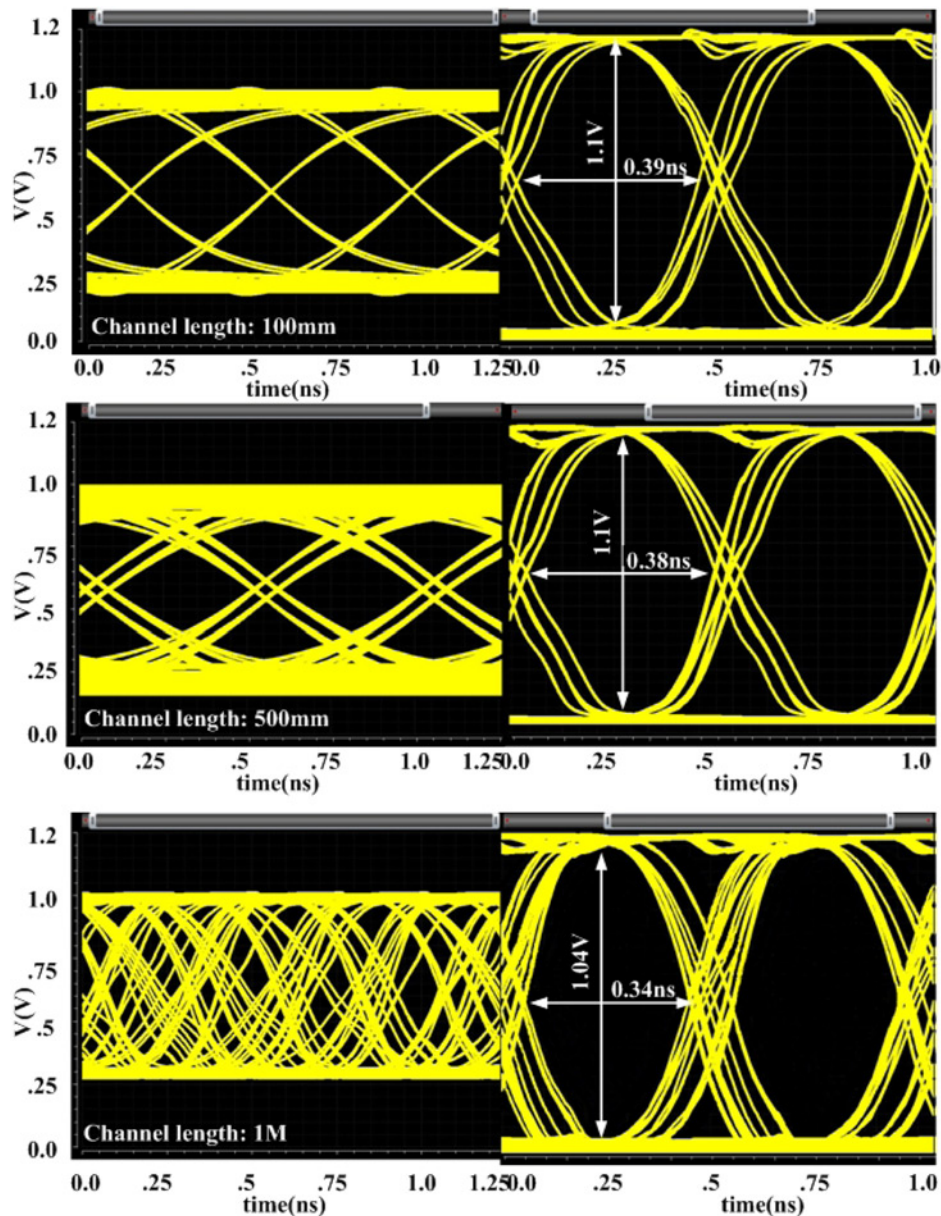


Fig. 7 Simulated eye diagram
Left: without DFE, and right: with DFE

current-steering tap generators with tap coefficients set by the tail currents, an error detect unit (EDU) consisting of three comparators and some logic gates, and two charge pumps that adjust the bias voltages of the tail current sources of the tap generators. Tap-1 takes the output of the slicer directly, whereas tap-2 has explicit delay units. The implementation of tap-1 is the same as that in [20]. Together with the delay of the second tap generator, the output of tap-2 has the delay of two unit intervals. It should be emphasised that the error signal from the EDU to the second tap generator needs to be delayed by one UI because of the temporal displacement of tap-1 and tap-2.

2.3 Simulation results

The proposed DFE is embedded in a 2 Gbps serial link shown in Fig. 6. The low-voltage differential-signalling driver conveys a 2 mA current to the channel that is terminated with a 100 Ω resistor at the far end of the channel. The data conveyed to the channel is a 10 bit pseudo-random bit sequence of full voltage swing. The

serial link is analysed using Spectre from Cadence Design Systems with BSIM4 device models.

Fig. 7 shows the simulated eye diagram of the signal at the input of the slicer without and with the proposed DFE for various channel lengths. It is seen that when the DFE is absent, the eye-opening is reduced with the increase in channel length and the eye is completely closed when channel length is 1 m. When the proposed DFE is activated, the data eye is open nicely. The vertical eye-opening for channel length 0.1, 0.5 and 1 m is found to be 1.1, 1.1 and 1.0 V, respectively. The horizontal eye-opening for channel lengths 0.1, 0.5 and 1 m is found to be 0.39, 0.83 and 0.34 ns, respectively. With 0.5 ns symbol time, the data jitter for channel length 0.1, 0.5 and 1 m is found to be 55, 60 and 80 ps, respectively.

Fig. 8 shows the adaptation process with channel length 60 mm. It is observed v_1 and v_2 rise rapidly and reach their steady-state values in ~ 20 ns. The fluctuations of v_1 and v_2 in their steady-state agree well with the bang-bang nature of the proposed DFE. If one wants to remove the fluctuations of v_1 and v_2 , a jitter dead zone can be introduced, as shown in Fig. 9. Traces 1 and 2 set the lower and

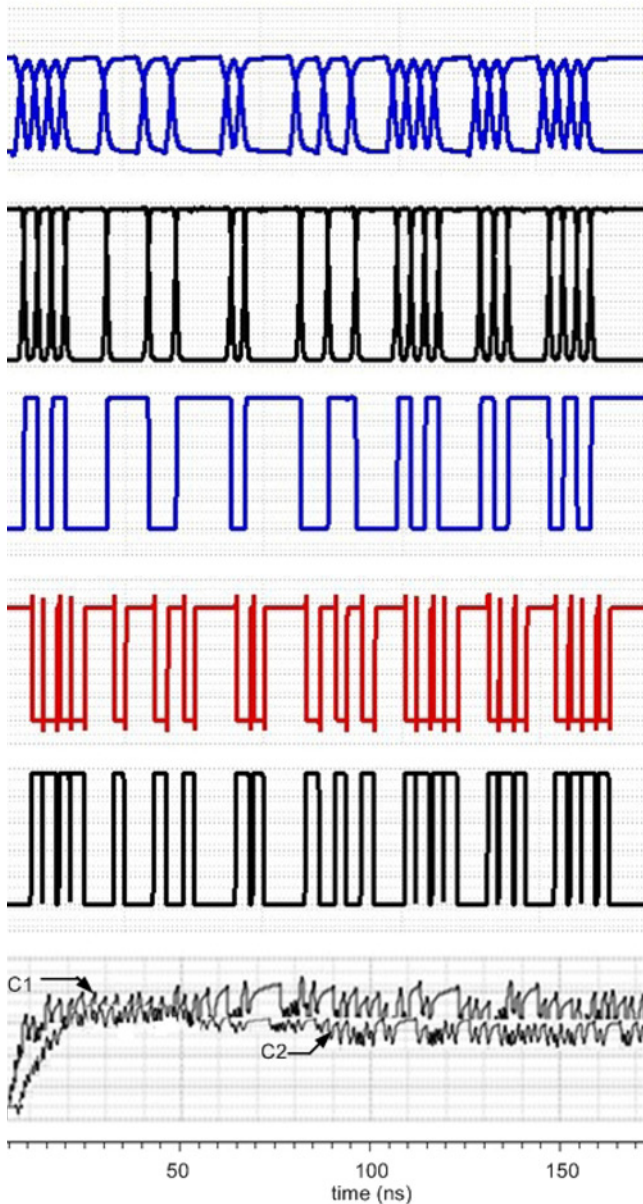


Fig. 8 Top figure: waveform of unequalised data symbols (channel length: 60 mm), second figure: waveform of equalised data symbols, third figure: output of slicer, fourth figure: error signal (low-to-high transition), fifth figure: error signal (high-to-low transition) and last figure: v_1 and v_2 of tap generators

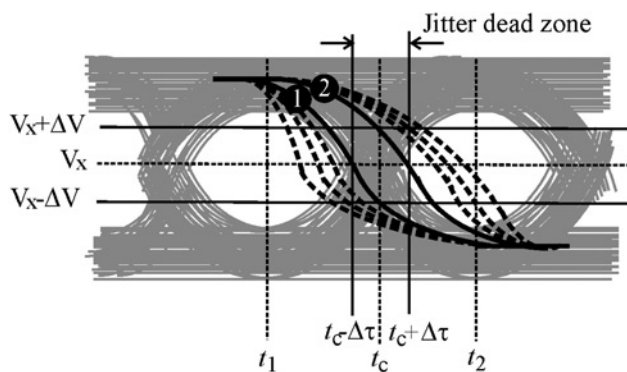


Fig. 9 Jitter dead zone

Table 1 Performance of the proposed jitter adaptive DFE (1 m channel length)

Tech.	IBM 130 nm
Supply voltage	1.2 V
Data rate	2 Gbps
Power of charge pumps	3.41 mW
Power of EDUs	6.33 mW
Power of DFE core (pre-amp., tap generators, delay units, ...)	5.71 mW
Total power	15.45 mW
Vertical eye-opening	1.0 V (83%)
Horizontal eye-opening	0.34 ns (68%)
Jitter	80 ps (16%)

upper boundaries. The corresponding voltages at t_c are $V_x - \Delta V$ and $V_x + \Delta V$, respectively. The corresponding jitter dead zone is given by $[t_c - \Delta\tau, t_c + \Delta\tau]$. Traces that fall into the dead zone will not flag an error. As a result, no action will be taken by DFE and v_1 , v_2 will remain unchanged. Traces that fall outside the dead zone (dotted traces) will flag an error, which will in turn activate DFE and adjust v_1 and v_2 accordingly. Table 1 tabulates the performance of the proposed DFE at 1 m channel length.

3 Conclusions

A minimum jitter-based adaptive DFE for Gbps serial links was presented. The adaptation in search for the optimal tap coefficients of DFE is carried out with the objective to minimise data jitter at the edge of data eyes. Jitter minimisation is achieved by adjusting the slope of the DFE that counteracts that of the channel. The effectiveness of the proposed adaptive DFE is evaluated by embedding the DFE in a 2 Gbps serial link. The data link is analysed using Spectre from Cadence Design Systems with BSIM4 device models. Simulation results demonstrate that the proposed adaptive DFE is capable of providing 83% vertical eye-opening, 68% horizontal eye-opening and 16% data jitter over 1 m FR4 channel while consuming only 15.45 mW. Although the example used to validate the proposed DFE contains only two DFE taps, the underlining principle is applicable to DFE with an arbitrary number of taps. The method presented here cannot change the number of DFE taps adaptively. If one wants to have the number of taps also to be adaptive to the characteristics of channels, an algorithm that pre-determines the number of taps based on the characteristics of the channel is needed.

4 Acknowledgments

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